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DESIGN OF LOW POWER ENCODING TECHNIQUES AND IT'S POWER ANALYSIS

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ABSTRACT

The power dissipation of links of network on chip increases as the technology going to reduce. This power dissipation is even larger than other elements of communication subsystem like router and network interface. Here, in this paper we represent gray code technique. The proposed system gives reduction in dynamic power dissipation by reducing coupling switching activity and switching activity when compared to previous systems. Also, the proposed scheme does not need any type of modification of the routers and link architecture. Using this, power dissipation and energy consumption will be reducedwithout any significant performancedegradation.

KEYWORDS

Data encoding; coupling switching activity; network-on-chip (NoC); low power, power analysis.

1. INTRODUCTION

As semiconductor technology scales to nanometer technology, power requirement becomes a critical factor in digital system. Network on chip is a communication system on integrated circuit between IP cores in a system on a chip (SOC). NoCtechnology is applied method for on-chip communication and brings improvement over conventional bus and crossbar interconnections. The network on chip (NoC) design paradigm is recognized as the most promising way to solve the scalability and variability problems that defines the ultra deep submicron meter era. As the design complexity increases, the total length of the interconnection wires increases which results in long transmission delay and higher powerconsumption.

In this paper, the main focusis on reduction of power dissipation caused by network links. In fact, the power dissipated by the network links is as large as that dissipated by network interfaces and routers and it will increase in near future nodes as technology scales. In particular, we present different designs of encoders which operates at flit level and workson end-to-end basis, which makes it easier to decrease both the switching activity and the coupling switching activity on links of the routing paths followed by the packets. We focus on data encoding schemes as a possible way to reduce dissipation of power by the links of network. The basic idea is to just encode the data before their injection in the network in such a way that it will reduce the switching activity of the links. Silicon area, reduction in power and energy are the parameters which are taken into consideration for analysis. The results show that by using this proposed encoding schemes power and energy can be saved.

2. RELATED WORK

The LDPC code is based on a set of individual or more crucial LDPC codes. Each one of the primary codes is a systematic linear block code. The primary code contains different code rates and packet sizes. Each LDPC code in the set of LDPC codes is distinctive by a matrix **H** of size m-by-n, where n is the length of the code and m is the amount of uniformity check bits in the code. The amount of orderly bits is$k=n-m$.

Majority-logic decoding is an easy

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and efficient method intended for decoding definite module of block codes, particularly intended for decoding definite module of repeated codes. Majority logic decoding is a technique to decode repetition codes. Based on the statement that the largest number of occurrences of a sign was the transmitted sign. It will amplify the power consumption. Syndrome vector is oldest expertise, which is used to identify the error in the code word. One of the examples of syndrome decoder is hamming code.

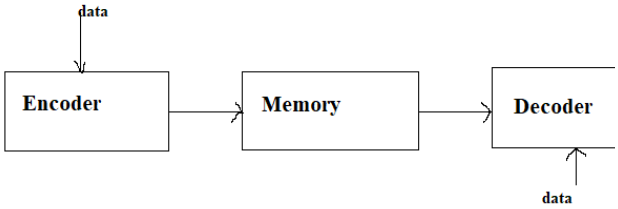

Fig2.1 Sample Memory System Schematic

These data encoding schemes which are discussed in the exceeding sections be replaced with these encoding schemes as an alternative of the encoder in the LDPC block. They had presented data encoding techniques which are used in the place of encoders in LDPC, which reduces the power consumption by eliminating the transitions as discussed before. Here we analyzed the Power consumption for these three schemes and compared their power and areaperformances.

3. PROPOSED METHOD

The basic idea of the proposed technique is the packets are transferred through the network after that the bits are encoded. This technique is more helping to reduce the switching activity and coupling switching activity in the links traversed by the packets. This self-switching activity and coupling switching activity are responsible for the link power dissipation. Here we refer to end-to-end scheme. Based on the end to end scheme we are having a better advantage. The advantage is a pipeline nature of the wormhole switching technique. Since the same sequence of all the packets passes through all the links of the routing path. The NI may provide the same power saving for all the links. The advanced scheme, an encoder and decoder block are added to the NI. The gray input is applied for all the three scheme encoders. The gray coding technique is used for the error correction application. The encoder encodes all the leaving bits of the packets other than header bit such that the power dissipated by the inter router and point-to point link is minimized.

The proposed data encoding schemes have been assessed by means of a cycle-accurate NoC simulator based on Noxim. The power estimation models of Noxim include NIs, routers, and links. The link power dissipation was computed using where the terms T0→1, T1, and T2 were computed based on the information obtained from the cycle accurate simulation. The following parameters were used in the simulations. The NoCwas clocked at 700 MHz while the baseline NI with minimum buffering and supporting open core protocol 2 and advanced high-performance bus protocols dissipated 5.3 mW. The average power dissipated by the wormhole-based router was 5.7 mW. Based on a 65-nm UMC technology, a total capacitance of 592 fF/mm was assumed for an inter-router wire. About 80% of this capacitance was due to the crosstalk. We assumed 2-mm 32-bit links and a packet size of 16 bytes (eight flits). Using the detailed simulations, when the flits traversed the NoC links, the corresponding self and coupling switching activities were calculated and used along with the self- and coupling capacitance of 0.237 and 0.947 nf, respectively, to calculate the power (Vdd = 0.9V and Fck = 700 MHz).

The encoder and the decoder were designed in Verilog HDL described at the RTL level, synthesized with synopsis design compiler and mapped onto an UMC 65-nm technology library. In our study, the area and power of the proposed encoding scheme I (H), scheme II (HF), and scheme III (OEF) are compared against SC and SCS, the BI

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coding, the coupling driven BI (CDBI) coding, and the forbidden pattern condition (FPC) codes. The area and power overheads of the NI compared to the baseline NI are shown in Fig.1. For each encoder type E, we consider four different implementations, denoted by E4, E8, E16, and E32 where in En, the link is partitioned in 32/nn-bit sub links. We apply the encoding scheme E in parallel to each sub link. In the case of FPC, 4-bit sub links are used in this paper. The results of Fig. 1 reveal that the power overhead for all the encoding schemes is below 10%. Except for the cases of OEF 32 and OEF16, the area overhead is below 15%. As we will see later, in many cases, the link power saving achieved in the encoding is well above the overhead.

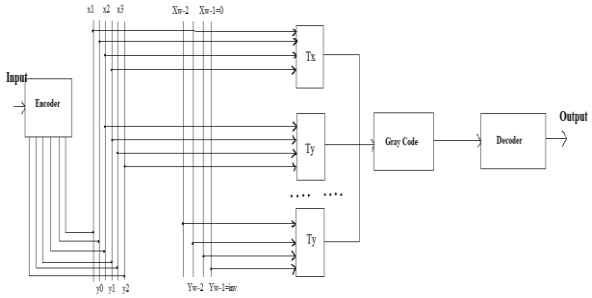

Fig 3.1 Block Diagram for proposed system

We are giving the input to the encoder. Encoder is used to encode the data or message which is in the form of physical or analog. By encoding the data, we get the output in the form of binary numbers (0 or 1). In fig 5.1 x1, y0, x2, y1, x3, y2 are the data lines it takes the data from encoder in the form of binary numbers. Tx, Ty, are the transition blocks, these blocks are used to check the switching activity present in the data. By comparing the present data (x1) with the previous data (y0) we can find the switching activity. Based on the transition block (switching activity) we are applying the data encoding techniques to reduce the switching activity and power consumption in the device.

Gray code:

The **reflected binary code** (**RBC**), also known just as **reflected binary** (**RB**) or **Gray code** after Frank Gray, is an ordering of the binary numeral system such that two successive values differ in only one bit (binary digit). The reflected binary code was originally designed to prevent spurious output from electromechanical switches. Today, Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.

Gray code is a coded binary representation of decimal digit which has a change in 1-bit position for consecutive digits.

The binary-reflected Gray code list for *n* bits can be generated recursivelyfrom the list for $n - 1$ bits by reflecting the list (i.e. listing the entries in reverse order), prefixing the entries in the original list with a binary 0, prefixing the entries in the reflected list with a binary 1, and then concatenating the original list with the reversed list.

Decimal Digit	Binary Digit	Gray code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

Table:3.2 Gray code to Binary & Binary to Gray

4. RESULT EXISTENCE METHOD

Clock Frequency	Dynamic Power	Quiescent Power	Total Power
100	0.016	0.081	0.097
200	0.032	0.081	0.113
300	0.048	0.081	0.129
400	0.064	0.081	0.145
500	0.080	0.081	0.162

Table 4.1 Result of Existence Method

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PROPOSED METHOD

Clock Frequency	Dynamic Power	Quiescent Power	Total Power
100	0.006	0.081	0.080
200	0.012	0.081	0.091
300	0.020	0.081	0.099
400	0.030	0.081	0.103
500	0.048	0.081	0.115

Table 4.2 Result of Proposed Method

5. CONCLUSION

In this project we have presented a set of new data encoding schemes aimed at reducing the power dissipated by the links of a NoC. In fact, links are responsible for a significant fraction of the overall power dissipated by the communication system. In addition, their contribution is expected to increase in future technology nodes. As compared to the previous encoding schemes proposed in the literature, the rationale behind the proposed schemes is to minimize not only the switching activity, but also (and in particular) the coupling switching activity which is mainly responsible for link power dissipation in the deep sub-micro-meter technology regime. The proposed encoding schemes are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. The encoders implementing the proposed schemes have been assessed in terms of power dissipation and silicon area. The impacts on the performance, power, and energy metrics have been studied using a cycle- and bit-accurate NoC simulator under both synthetic and real traffic scenarios.

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