



International Journal for Innovative Engineering and Management Research

A Peer Reviewed Open Access International Journal

www.ijiemr.org

COPY RIGHT



ELSEVIER
SSRN

2019IJIEMR. Personal use of this material is permitted. Permission from IJIEMR must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. No Reprint should be done to this paper, all copy right is authenticated to Paper Authors

IJIEMR Transactions, online available on 3rd Apr 2019. Link

[:http://www.ijiemr.org/downloads.php?vol=Volume-08&issue=ISSUE-04](http://www.ijiemr.org/downloads.php?vol=Volume-08&issue=ISSUE-04)

Title: **16x16 VEDIC MULTIPLIER USING REVERSIBLE LOGIC GATES**

Volume 08, Issue 04, Pages: 72–79.

Paper Authors

**A.SATHI BABU, P.N.B.SWAMY, V.L.NAVEENA, V.RAMYA KALYANI,
S.RISHITHA, T.CHAITANYA**

NRIIT



USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per **UGC Guidelines** We Are Providing A Electronic Bar Code



16x16 VEDIC MULTIPLIER USING REVERSIBLE LOGIC GATES

¹A.SATHI BABU, ²P.N.B.SWAMY, ³V.L.NAVEENA, ⁴V.RAMYA KALYANI, ⁵S.RISHITHA, ⁶T.CHAITANYA

^{1,2}Assistant professor, Dept. of ECE,NRIIT
^{3,4,5,6}Student, Dept. of ECE,NRIIT

Abstract— Multiplier design is always a challenging task; how many ever novel designs are proposed, the user needs demands much more optimized ones. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation is drastically reduced by the use of Reversible logic. The reversible Urdhva Tiryakbhayam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. In this paper we aim to enhance the performance of the previous design. The Total Reversible Logic Implementation Cost (TRLIC) is used as an aid to evaluate the proposed design. This multiplier can be efficiently adopted in designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications.

Keywords— Quantum Computing, Reversible Logic Gate, Urdhva Tiryakbhayam, Optimized Design, TRLIC.

I. INTRODUCTION

Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved.

With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. Vedic mathematics can be aptly employed here to

perform multiplication. Another important area which any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a tradeoff between the power dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. Thus during the design of any reversible circuit the delay is the only criteria that has to be taken care of. In a reversible Urdhva Tiryakbhayam Multiplier had been proposed. This paper is an extension of the previous work which tries to optimize the circuit proposed in. The paper is organized as follows: The section II gives the basics of reversible logic along with the literature review. Section III explains the Urdhva Tiryakbhayam algorithm. The section IV describes the modifications of the previous design in order to evolve the optimized design. section V compares the proposed design with the other non Vedic multipliers as well as the previous Vedic multiplier design and draws a conclusion claiming the versatility of Reversible Urdhva Tiryakbhayam multiplier.

II. REVERSIBLE LOGIC

A. Literature Survey and Significance of reversible logic Conventional combinational logic circuits are known to dissipate heat for every bit of information that is lost. This is also evident from the second law of thermodynamics which states that any irreversible process leads to loss of energy. Landauer showed that any gate that is irreversible, necessarily dissipates energy, and each irreversible bit generates $kT \ln 2$ joules of heat where k is Boltzmann's constant (1.38×10^{-23} joules/Kelvin) and T is temperature in Kelvin. Lowering the threshold voltage and management of the power supply are widely applied practices to decrease the energy consumption in any logical operation. However these technologies of lowering the energy consumption will hit a barrier of kT . In

order to alleviate this, techniques such as reducing the temperature of computer and constructing a thermodynamically reversible computer can be used Frank analyzed that the second option was a better choice. When the temperature of the system reduces to absolute zero, the energy reduces two orders of magnitude but using reversible computing there can be further more reduction that Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT 2013) matches with the theoretical value. The cardinal feature of reversible computing is that electric charge on the storage cell

consisting of transistors is not permitted to flow away during transistor switching. This can be reused through reversible computing and hence decrease energy dissipation. Bennett in 1973 showed that an irreversible computer can always be made reversible. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost.

B. Reversible Logic Gates

A Reversible Logic gate is an n -input n -output logic function in which there is a one-to-one correspondence between the inputs and the outputs. This not only helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Because of this bijective mapping the output vectors are merely permutations of the input vectors. Some of the basic reversible logic gates in the literature those are useful in designing the Reversible Urdhva Tiryakbhayam Multiplier are the Feynman Gate—the only 2×2 gate, that is used for fan-out purposes as well as for complementing. It has a quantum cost of one. Peres Gate—a 3×3 gate that is used to produce AND operation as well as EX-OR operation. It has a quantum cost of four. New

Fault Tolerant gate (NFT) – is also a 3x3 gate with a quantum cost five. HNG gate which is a 4x4 gate that can be effectively used as a full adder and provides minimum quantum cost implementation. It has a quantum cost of six. BVPPG is a 5x5 gate with a quantum cost of ten. All the mentioned gates are shown in the figure 1.

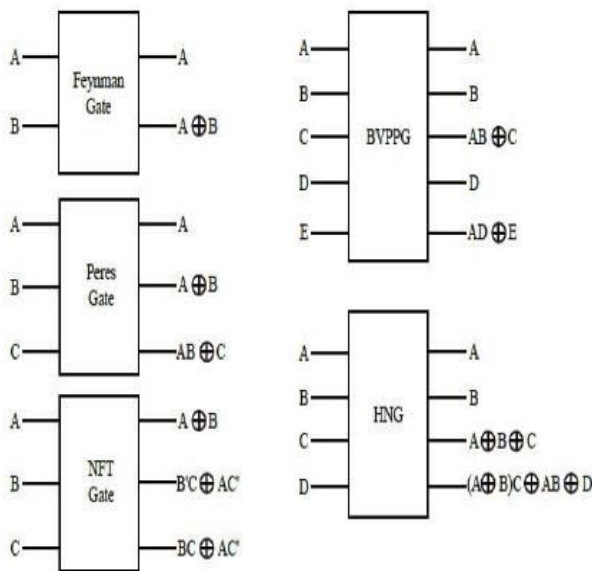


FIGURE 1: REVERSIBLE LOGIC GATES

FIGURE 1: REVERSIBLE LOGIC GATES

C. Optimization parameters for reversible logic circuits

The important parameters which play a major role in the design of an optimized reversible logic circuit are as listed:

- Constants (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- Garbage (GO): This refers to the number of outputs which are not used in the synthesis of a given function. These are very essential, without which reversibility cannot be achieved.
- Gate count (NG): The number of reversible gates used to realize the function.

□□ Flexibility: This refers to the universality of a reversible logic gate in realizing more functions.

□□ Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1x1 or 2x2) required to realize the circuit

□□ Gate levels: This refers to the number of levels in the circuit which are required to realize the given logic functions.

□□ Total Reversible Logic Implementation Cost (TRLIC) : Let, in a reversible logic circuit there are NG reversible logic gates, CI constant inputs, GO number of garbage outputs, and have a quantum cost QC. Then the TRLIC is given as

$$TRLIC = \sum(NG + CI + GO + QC) \dots 1$$

III. URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM

Urdhva Tiryakbhayam (UT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhayam. Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in computation of the product does not increase proportionately. Because of this fact the time of computation is independent of clock frequency of the processor. Hence one can limit the clock frequency to a lower value. Also, since processors using lower clock frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms like the above mentioned. The

Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers. Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT 2013).

scaled up by optimizing each individual unit in terms of quantum cost, garbage outputs etc.

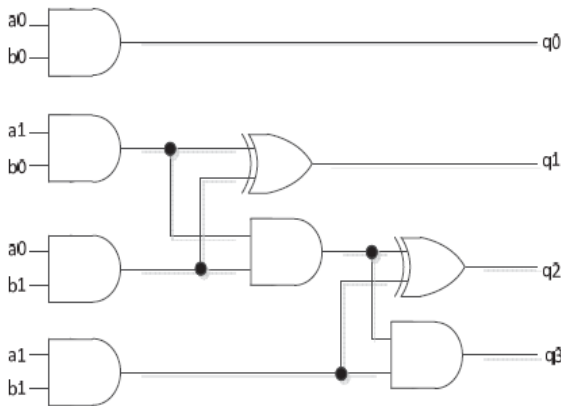


FIGURE 3: CONVENTIONAL 2X2 URDHVA TIRYAKBHAYAM MULTIPLIER [8]

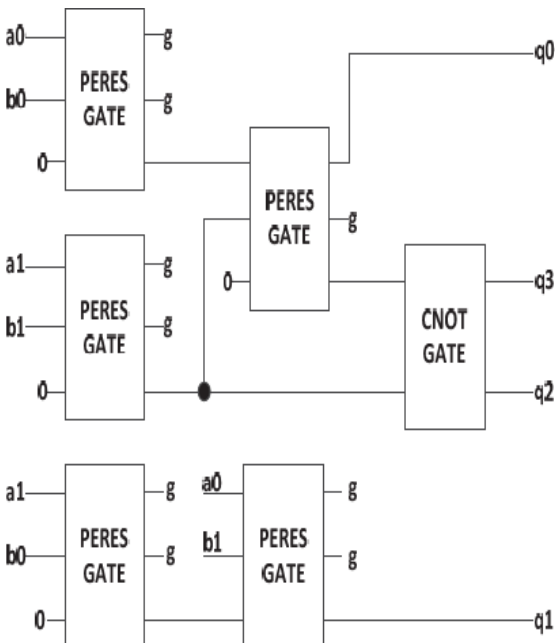


FIGURE 4: REVERSIBLE 2X2 UT MULTIPLIER IN [12]

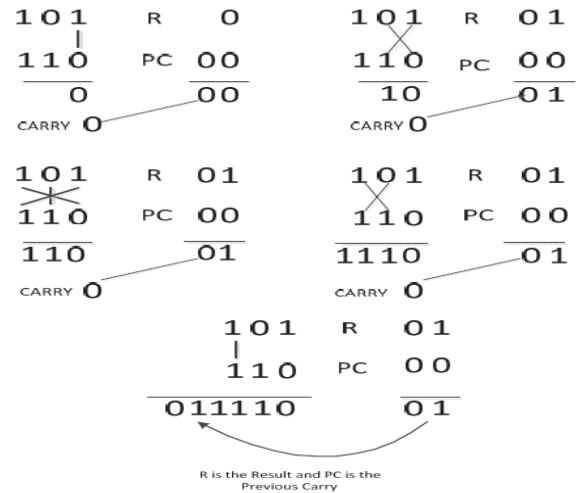


FIGURE 2: URDHVA TIRYAKBHAYAM PROCEDURE FOR MULTIPLICATION

The Algorithm: Multiplication of 101 by 110.

1. We will take the right-hand digits and multiply them together. This will give us LSB digit of the answer.
2. Multiply LSB digit of the top number by the second bit of the bottom number and the LSB of the bottom number by the second bit of the top number. Once we have those values, add them together.
3. Multiply the LSB digit of bottom number with the MSB digit of the top one, LSB digit of top number with the MSB digit of bottom and then multiply the second bit of both, and then add them all together.
4. This step is similar to the second step, just move one place to the left. We will multiply the second digit of one number by the MSB of the other number.
5. Finally, simply multiply the LSB of both number together to get the final product. The conventional logic design implementation of a 2x2 Urdhva Tiryakbhayam multiplier using the irreversible logic gates is shown in the Figure 3. In the four expressions for the output bits are derived from this figure and is used to obtain the reversible implementation as shown in Figure .

4. The circuit uses five Peres gates and one Feynman gate. This design has a total quantum cost of 21, number of garbage outputs as 11 and number of constant inputs 4. The gate count fan is 6. This design does not take into consideration the outs. The overall performance of the UT multiplier is scaled up by optimizing each individual unit in terms of quantum cost, garbage outputs etc.

A. Improved 2x2 Urdhva Tiryakbhayam multiplier

The design expressions can be logically modified so as to optimize the design. The new design makes use of one BVPPG, three Peres gates and a single Feynman gate. The design also takes into account the fan outs. One of the major design constraints of reversible logic is the fan out, other being loops not permitted. This means that the reversible logic circuit with multiple numbers of same inputs is not advisable. One way out is to use a separate fan out generator or to build a circuit that inherently takes care of fan outs using the reversible logic gates used in the design. This design has a quantum cost of 23, number of garbage outputs as 5, number of gates 5 and the number of constant inputs is 5. The second design also considers the fan out using BVPPG, three Peres gates and one NFT gate as shown in the figure.

5. Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT 2013). The quantum cost of the circuit is 24; number of garbage outputs as 4, number of gates 5 and the number of constant inputs is 5. I1, I2, I3 (Fig 5 and 6) and I4 (Fig 6) are the intermediate outputs that are used for fan-out purposes.

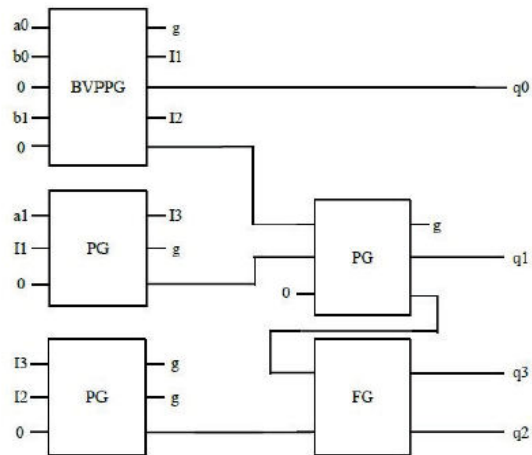


FIGURE 5: PROPOSED MODIFIED DESIGN 1

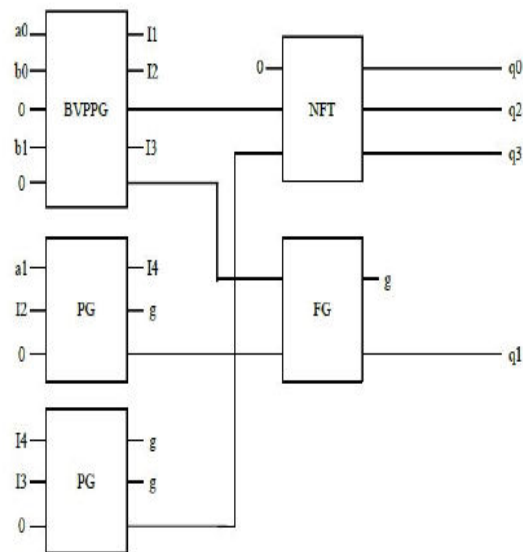


FIGURE 6: PROPOSED MODIFIED DESIGN 2

B. Design of 4x4 Urdhva Tiryakbhayam multiplier

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure.

6. It consists of four 2X2 multipliers each of which procures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as

input to the four bit ripple carry adder. The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in turn 5 bits each which need to be summed up. This is done by a five bit ripple carry adder which generates a six bit output. These six bits from the upper bits of the final result..

C. Modification in the design of ripple carry adder

The design shown in consists of only HNG gates. The number of HNG gates is 4 if the ripple carry adder is used in the second stage or five if the ripple carry adder is used in the last stage of the 4X4 Urdhva Tiryakbhayam Multiplier. the ripple carry adder can be modified as under. Since for any ripple carry adder the input carry for the first full adder is zero, this implicitly means the first adder is a half adder. Thus a Peres gate can efficiently replace a HNG. This cut down the quantum cost by two for any ripple carry adder and the garbage output by one. The Constant inputs and the gate count remain unchanged

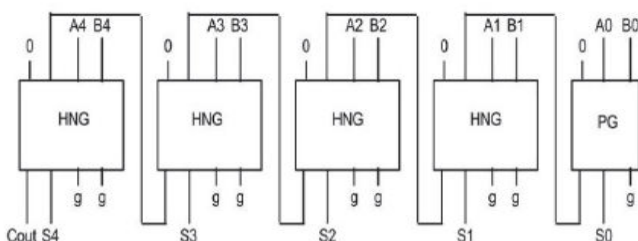


FIGURE 7: PROPOSED MODIFIED 5 BIT RIPPLE CARRY ADDER DESIGN

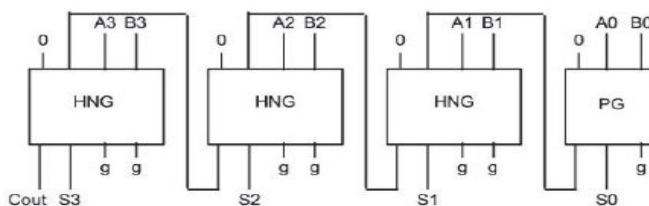


FIGURE 8: PROPOSED MODIFIED 4 BIT RIPPLE CARRY ADDER DESIGN

The 4x4 UT multiplier structure is as shown in figure 9.

. The 4x4 UT multiplier structure is as shown in figure 9. The design of the reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i and MODELSIM. The simulation results are as shown in figures 10 and 11 respectively. The following are the important design constraints for any reversible logic circuits.

1. Reversible logic circuits should have minimum quantum cost.
2. The design can be optimized so as to produce minimum number of garbage outputs.
3. The reversible logic circuits must use minimum number of constant inputs.
4. The reversible logic circuits must use a minimum number of reversible gates.

Since TRLIC is the sum of all these design commendable to have a least value of TRL design of Reversible UT Multiplier is compass 11 different prominent multiplier design in terms of Quantum cost, garbage outputs, number of constant inputs and also in terms This also includes a comparison with our own and the optimization is clearly evident full Comparison as shown in figure9.

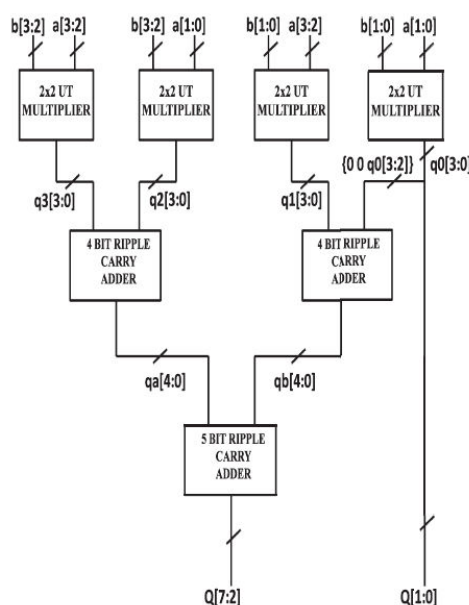
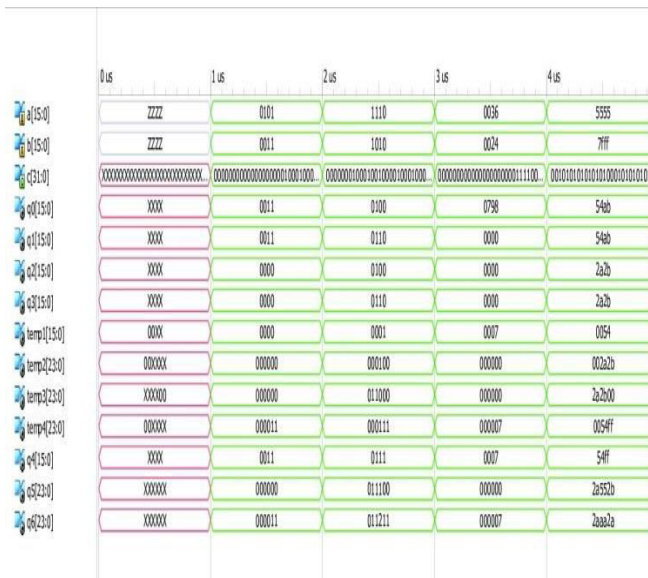


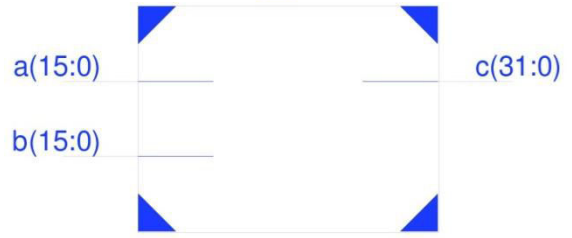
FIGURE 9: BLOCK DIAGRAM OF 4X4 UT MULTIPLIER

The proposed design of 16x16 UT multi mentioned takes care of the fan-outs also. slight increase in the quantum cost of the 2x2 is 23. First HNG gate by a Peres G output by one due to the same quantum cost has increased garbage outputs and gate count. The focus of this paper is main speed multiplier which is done using reversible logic gates. They to yield an optimized design literature. The efficiency of characterized in terms of parameter number of constant inputs, g gates utilized to realize the lower value of these parameters more called TRLIC had been as sum of all cost metrics of the cost is a parameter that direct quantum circuit. Also lower the quantum cost, hence lower Besides imbibing the design generated within the circuit, the TRLIC as compared to the , The further optimization total logical costs is under the work. The quantum perfectly reflects the delay of the TRLIC implicitly means lower is the delay and vice versa. criterion that fan-out must be he proposed designs also reduce ,he previously proposed design n of the circuit in terms of the progress and is taken as future proceedings.

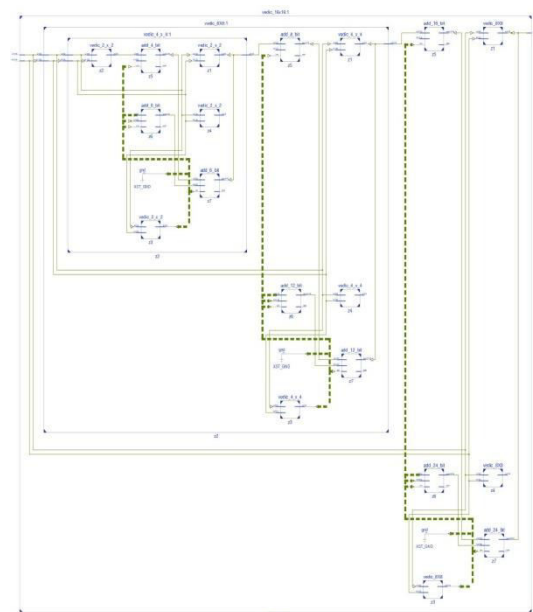
IV RESULTS AND OUTPUTS



vedic_16x16



vedic_16x16



REFERENCES

- [1] Swami Bharati Krsna Tirtha, Vedic Mathematics. Delhi: Motilal Banarsidass publishers 1965
- [2] Vedic Mathematics: <http://www.hinduism.co.za/vedic.html>.
- [3] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp.183-191, 1961.
- [4] C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.
- [5] R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11-20, 1985.



- [6] A. Peres, Reversible logic and quantum computers, *Phys. Rev. A* 32 (1985) 3266–3276.
- [7] E. Fredkin and T. Toffoli, "Conservative Logic", *Int'l J. Theoretical Physics* Vol 21, pp.219-253, 1982.
- [8] G Ganesh Kumar and V Charishma, Design of high speed vedic multiplier using vedic mathematics techniques, *Int'l J. of Scientific and Research Publications*, Vol. 2 Issue 3 March 2012.
- [9] Rakshith Saligram and Rakshith T.R. "Design of Reversible Multipliers for linear filtering Applications in DSP" *VLSICS*, 3. No (6), Dec-12
- [10] Rakshith Saligram and Rakshith T.R. "Novel Code Converter Employing Reversible Logic", *International Journal of Computer Applications (IJCA)*, August 2012.
- [11] H R Bhagyalakshmi and M K Venkatesha, "Optimized multiplier using Reversible Multi-Control Input Toffoli Gates", *VLSICS*, Vol 3. No (6), Dec.- 12.
- [12] Rakshith T R and Rakshith Saligram, Design of High Speed Low Power Multiplier using Reversible logic: a Vedic Mathematical Approach, *Intl. Conf. on Circuit, Power and Computational Technologies*.
- [13] H. R. Bhagyalakshmi, M. K. Venkatesha, "An Improved Design of a Multiplier using Reversible Logic Gates," *IJEST*, Vol. 2, No. 8, 2010.
- [14] Fateme Naderpour, Abbas Vafaei "Reversible Multipliers: Decreasing the Depth of the Circuit" *ICECE 2008*, 20-22 December 2008.
- [15] Maryam Ehsanpour, Payman Moallem, Abbas Vafaei, "Design of a Novel Reversible multiplier Circuit Using Modified Full Adder", 2010 International Conference On Computer Design And Applications, 1389, (ICCD 2010).
- [16] M. Haghparast, S. Jafarali Jassbi, K. Navi and O. Hashemipour, "Design of a Novel Reversible Multiplier Circuit Using HNG Gate. in *Nanotechnology*", *World Applied Science J.* Vol. 3 No. 6, 2008.
- [17] M.S. Islam et al., "Low cost quantum realization of reversible multiplier circuit", *Information technology journal*, Vol.8, 2009.
- [18] M. Shams, M. Haghparast and K. Navi, "Novel Reversible Multiplier Circuit in nanotechnology", *World Applied Science. Journal* Vol. 3, No. 5, pp. 806-810, 2008.
- [19] Nidhi Syal, Dr. H.P. Sinha, "Design of fault tolerant reversible multiplier", *International Journal of Soft Computing and Engineering (IJSCE)* ISSN: 2231-2307, Volume-1, Issue-6, January 2012.
- [20] H. Thapliyal and M.B. Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", *Proc. IEEE International Conference on Computer Systems and Applications*, pp. 100-103, March 2006.
- [21] Somayeh Babazadeh and Majid Haghparast, "Design of a Nano metric Fault Tolerant Reversible Multiplier Circuit", *Journal of Basic and Applied Scientific Research*.
- [22] Thapliyal, H., M.B. Srinivas and H.R. Arabnia, 2005, A Reversible Version of 4x4 Bit Array Multiplier with Minimum Gates and Garbage Outputs, *Int. Conf. Embedded System, Applications (ESA'05)*, Las Vegas, USA, pp: 106 114.
- [23] A. Khazamipur K. Radecka, "Adiabatic Implementation of Reversible Logic", *Proc. Midwest Intl. Symposium on Circuits and Systems*, pp. 291--294, 2005.