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Enhanced Reverse Carry Propagate Adder For High Speed And Energy Efficient DSP Applications

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Abstract— Digital signal processing (DSP) hardware acceleration has recently been shown to be a very promising implementation strategy. In this abstract, we provide an unique accelerator architecture based on flexible computational units that aids in the execution of a large number of operation templates accessible in DSP kernels rather than a monolithic application-specific integrated circuit design approach. Many digital signal processing applications depend on adders, including This study demonstrates a well-organized reverse carry propagate adder (RCPA). Due to the unique RCPA structure, a Carry signal is better suited for manufacturing since it propagates from the most significant bit (MSB) to the least significant bit (LSB) backwards. With delay variance, the stability of this propagation method is improved significantly. The n-bit adder architecture is similarly based on a hybrid structure in which the first half of the adder is added using a high-speed high-accuracy adder, such as Brent–Kung. We may boost the speed of the adder by employing the Brent–Kung adder, and at least half of the adder design is accomplished by using the Reverse Carry Propagate Adder (RCPA) (RCPA). Xilinx ISE 14.7 software and Verilog HDL coding are used to examine the structure of hybrid adders and compare it to that of standard approximation adders.

Index Terms— Approximate adder, Parallel Self Timed adder (PASTA), Digital signal processing (DSP), Reverse carry propagate adder (RCPA),

INTRODUCTION

Adder blocks, which are critical components of DSP systems' arithmetic units, use a lot of power and tend to generate hotspots in the die. These serve as the driving forces behind the approximation computing method used to create this kind of component. At the very least, general-purpose processors and DSP instruction sets incorporate some kind of addition. There are several operations that incorporate addition and whose underlying hardware is similar or identical to addition hardware, such as subtraction and multiplication. If an adder is in the critical path, then the design's performance is generally limited by the performance of its numerous adders or adders. A chip's remaining properties, such as power or area, are more likely to be influenced by the hardware used for addition. There are a slew of additional considerations that come into play when making the decision about which adder to utilise in an application. As signal and computer processing applications grow,

the need for high-speed processing grows as well. Many image processing and real-time signal applications rely on faster arithmetic operations to meet their performance goals.
As a result of its growing popularity, digital signal processing (DSP) has been included into a large number of commercial processors. When compared to general-purpose processors, DSPs have a wide range of architectures and features. The gain performance of these features determines the overall processor performance. Experiments on approximation adders have been done before.

Concentrate on reducing errors through reducing the frequency of errors and increasing the weight of errors. Designing digital processing units, particularly portable systems, has as its primary objectives reducing power consumption and increasing speed. For certain processing units, an increase in speed is often accompanied by an increase in power consumption. Increasing throughput at the expense of precision may also be an option for increasing both speed and power.

Approximate computing is the method used in this project. It is employed in situations where a small number of mistakes is acceptable. In a hybrid structure adder, the estimated least significant bits (LSBs) and the accurate most significant bits (MSBs) are used in distinct regions. The fault is found in the summing of the LSB and the input carry of the MSB parts. This reduces the MSB part's error weight by limiting the carry input's error weight. Due to the fact that most of the work is done in the LSB section. Using pure approximation adder structures is the second strategy to consider. The major design requirements for these adders are to decrease power consumption and delay, as well as to lower the error probability of summing.

Hybrid adders with the usage of the RCPFA (approximate reverse carry propagate full-adder) will be studied in this work. The carry input is propagated from the high significant bit to the low significant bit in the approximation adder to generate the carry out. A prediction signal may be used as an output signal in this adder type, known as a reverse carry propagate adder (RCPA). The propagation weight will be reduced by adopting reverse carry propagation. Parallel prefix adder is used to add the MSB half because it may increase the speed of operation. An approximate reverse carry propagate adder is used to add the LSB half of the signal.

LITERATURE SURVEY

The Ripple carry adder (RCA) has the poorest power and area utilizations among the precise adder topologies. Despite this, there is a significant lag time. The precision of this adder has been compromised in order to boost the adder's energy economy and speed.
An error-tolerant adder structure (EAS), a rough approximation of an RCA, has been proposed. Figure 1 depicts the EAS organisational structure.

1. In this design, the input operands are seperated into 2 parts called exact

computation part and inexact computation part. In the exact part is the MSB part, the conventional FAs with a zero input carry for the each part are used wherease the inexact part is the LSB part which consists of a carry-free addition part.

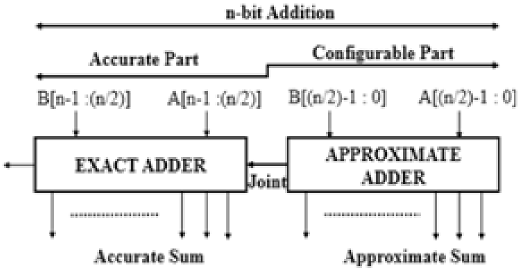


Fig.1 Error tolerant adder structure

We chose an adder that employs reverse carry propagation, in which the carry is propagated in the opposite direction of the clock, because of the added delay imposed by carry propagation.

The standard FA, a critical building block of reverse carry propagate adders, has three equally weighted inputs. For a summation, it has a single output with twice the weight of the inputs and two outputs with the same weight as the inputs. Carry propagation delay (tCP) is an important timing component in FAs since it has historically played a role in defining the critical route delay in multibit adders (and multipliers). Short-delay violations might result in a large amount of error since the fault arises on the MSBs of the summation.

This is the result of the propagation and generation of the input carry of the MSBs through less significant bit FAs. Due to this reason, if the order of the carry propagation is reversed, one can see the decrease in the amount of error due to the timing violation.

2. Reverse Carry Propagate Full-Adder Cell

Each exact FA generates its sum and carry output signals using

$$2C_{i+1} + S_i = A_i + B_i + C_i$$ ....(1)

Where Ai (Bi) is the ith bit of the input A(B), Ci(Ci + 1)is the carry in (output), and *Si* is the ith bit of the sum.

Based on this equation, the output signals in the ith bit position relay on the ith bits of the inputs *A* and *B* and the carry out of the previous position (Ci). By moving the term Ci (Ci + 1)to the left (right) of the equation, one can write as

$$S_i - C_i = A_i + B_i - 2C_{i+1} \qquad (2)$$

Considering equation (2), one can think of a full adder as a design whose operation depends on the carry out of the (i + 1)nth bit position (Ci + 1)and its input operand bits. For this structure, the sum and the carry signals having the equal weights are the outputs .

From the above discussion, we suggest a family of full adders for the RCPFA shown in Fig.

As shown in Fig. 2, these full adders have four inputs and 3 outputs. The inputs are the input operands (Ai and Bi), the carry out of the next bit position (Ci+1), and a forecast signal (Fi). The RCPFA determines the carry (Ci), summation result (Si), and the forecast signal (Fi+1) as its output signals. As mentioned earlier, the advantage by using the RCPA is that the value of the error is in the direction with respect to decrease in the bit significance. This shows that the cumulative impact factor of the error (e.g., because of the delay variation) during the carry propagation is lower for bits with higher significances.

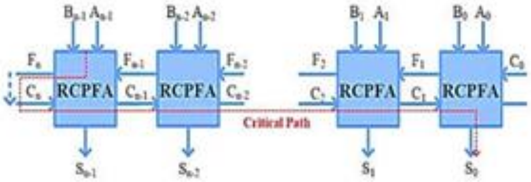
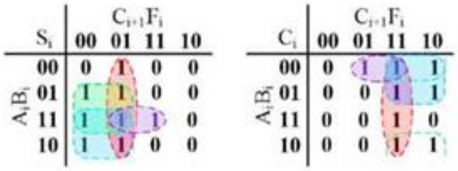


Fig .2 n-bit RCPA.

To determine a structure for RCPFA, the Karnaugh maps of the summation result (S_i) and carry (C_i) were drawn based on (2) and considering the forecast signal (F_i) as an input (Fig. 3) The Boolean equation between inputs gives rise to Si and Ci

$$S_i = C_{i+1}F_i + C_{i+1}A_i + C_{i+1}B_i + A_i B_i F_i \quad (3)$$

$$C_i = C_{i+1}F_i + C_{i+1}A_i + C_{i+1}B_i + A_i B_i F_i \quad (4)$$



S_i \ A_iB_i \ $C_{i+1}F_i$	00	01	11	10
00	0	1	0	0
01	1	1	0	0
11	1	1	1	0
10	1	1	0	0

C_i \ A_iB_i \ $C_{i+1}F_i$	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	1	0
10	0	0	1	1

Based on our design requirement we use 3 types of reverse carry propagate adders the designs of those adders is shown below. By using these proposed adders we can implement 3 types of reverse propagate adders and are it is used in the place of approximate adders which is shown on figure 1.

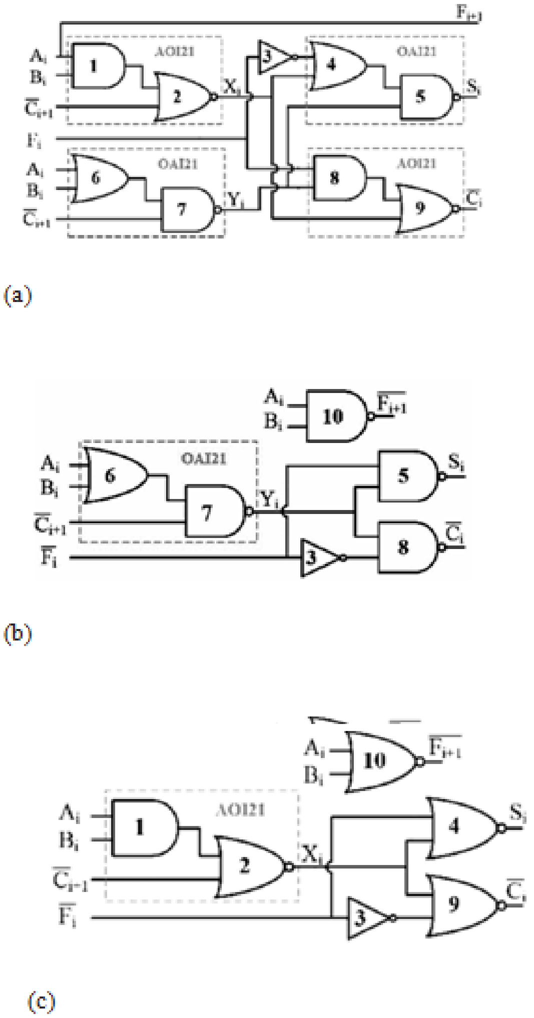


Fig.4 Internal structures of the (a) RCPFA-D1, (b) RCPFA-D2, (c) RCPFA -D3

The block diagram of an n-bit adder which is designed with the help of reverse carry propagate adder is shown in below figure

As mentioned before, the weight of the carry decreases as the carry propagates in a counter-flow manner.

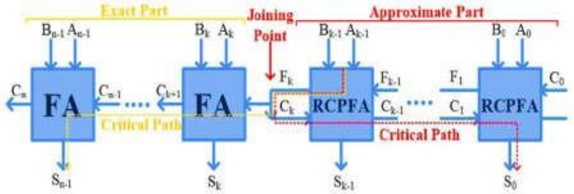


Fig.5 Architecture of an n-bit adder with RCPA This property helps having less vulnerability to the delay variation (due to process and supply voltage variations) impact for this adder when compared to other proposed approximate FAs. This is especially advantageous in the case of hybrid adders with large sizes for the approximate part which determines the critical path of the adder. The proposed RCPFAs may be used in hybrid adders whose general *n*-bit structure based on the RCPFAs is depicted in Fig. 8. Obviously, the design parameters of the adder relay on the width part of the approximate adder.

PROPOSED METHOD

Here we will propose a new adder It is called as hybrid n-bit two n/2 bit adders are combined to generate an adder with an output of the same number of bits. We will employ a PASTA adder, a parallel self-timed adder, in order to increase delay performance. Carry, or how quickly the adder reaches each bit position, affects the delay in an adder. As a result, the carry chain is the most complex part of the design of binary addition. The carry chain's latency and length rise in tandem with the incoming operand's increase in breadth. Parallel prefix adders may be used to increase speed and reduce latency.

Until all of the carry bits are calculated, simultaneous prefix adders compute a limited number of intermediate prefixes and then locate the big group prefixes. Operands A and B are added in three phases to a parallel prefix addition of width n:

1. Pre Processing
2. Carry Generation
3. Post processing

1. *Pre-processing stage:*

In first stage process we compute, The generate signals and propagate signals are utilized such that carry in of each adder is generated. A and B are inputs.

It is one of the most extensively used and popular adders. This adder is used to conduct addition operations at a high rate of performance. Parallel prefix adders are a subset of this kind. PASTA adders are less expensive, but they also simplify wiring. It's like a tree structure that does the math. The Pasta adder has both grey and black cells. ' There will be one OR gate and two AND gates in every black cell. There is only one AND gate in every grey cell. A single AND gate and an OR gate are used to create the signal gi. Pi stands for propagate and just one AND gate is required. The term "carry generate" refers to the employment of one AND gate and one OR gate in the first black cell of the equation. This information may be seen in the equations 5 and 6.

Pi = Ai Xor Bi……(5)

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Gi = Ai. Bi … … (6)

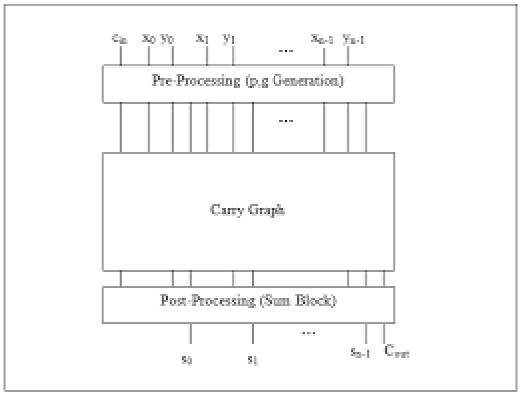

c_{in} x_0 y_0 x_1 y_1 … x_{n-1} y_{n-1}
Pre-Processing (p,g Generation)
Carry Graph
Post-Processing (Sum Block)
s_0 s_1 … s_{n-1} C_{out}

Fig.6 Block Diagram of Parallel prefix addition.

2. **Carry generation stage**:

We'll get the carries for every bit in this generating step. A parallel mode of execution is used. Carry computations in parallel are broken down into a number of smaller components. Two AND gates and one OR gate are included in the carry operator. Figures 7 and 8 show that the intermediate signals are propagate (Pi) and create (Gi).

P(i:k) = P(i:j) · P(j–1:k) … … (7)

G(i:k) = G(i:j) + (G(j–1:k) · P(i:j)) … … (8)

This carry can generated by using different cell structures such as Gray cell, Black cell and Buffer cell. By use of this cell structures we will be able to calculate final carry and is similar for all parallel prefix adders but the design of carry generation is different.

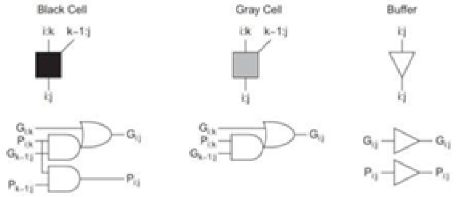


Fig.7 Black Cells, Gray Cells and Buffer cell used for carry generation stage.

ARCHITECTURE OF PASTA

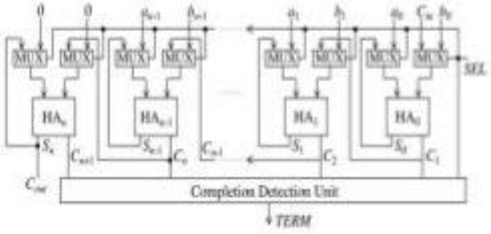


Fig.8 Architecture of PASTA adder

1. ***Post Processing:***

The sum is generated either by the use of simple XOR gates or by the use of conditional sum adders. In conditional sum adders, for each bit position, It generates two tentative sums and the correct one will be selected when the relevant carry for that bit arrives.

Proposed Adder architecture is shown in below figure:

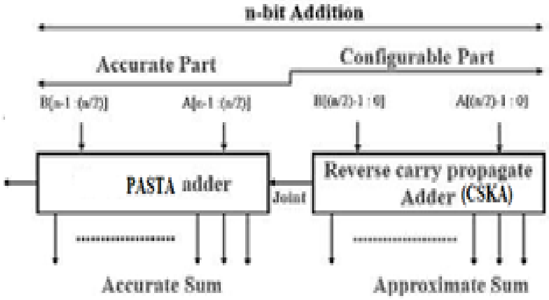
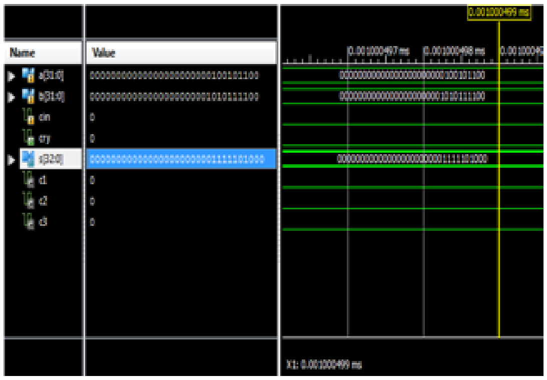


Fig.9 Modified Hybrid adder Architecture.

RESULT

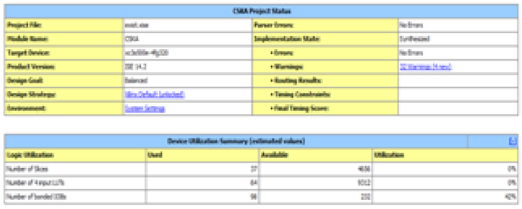
By implementing the adder by using two sub adders like PASTA adder and reverse carry propagate adder we can have better in terms of delay and energy. Here in this paper we present 32- bit adders with the design of reverse carry propagate adders. The results are presented in the below table

S.No	32 bit adder	Existing Method	Proposed Method
1	Area	95	112
2	Delay	21.765	15.296
3	power	5.521	4.485



```
Name      Value
a[31:0]   00000000000000000000000100101100
b[31:0]   00000000000000000000001010111100
cin       0
cry       0
s[32:0]   000000000000000000000001111101000
c1        0
c2        0
c3        0
```

. Fig.10. Simulation Results



CSRA Project Status			
Project File:	xxxt.xise	Parser Errors:	No Errors
Module Name:	CSRA	Implementation State:	Synthesized
Target Device:	xc3s500e-4fg320	• Errors:	No Errors
Product Version:	ISE 14.2	• Warnings:	32 Warnings (4 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	37	4656	0%
Number of 4 input LUTs	64	9312	0%
Number of bonded IOBs	98	232	42%

Fig.11. Synthesis Report

CONCLUSION

Using two different kinds of adders, we were able to create an n-bit adder with a hybrid architecture. It is more important to employ approximation in addition's lower half since it is less significant than addition's upper half, where it is more crucial. The pasta adder we utilised in this project is a parallel prefix adder, and the RCPA we built in this work is the approximation adder. We can save energy and improve latency by using this design.

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