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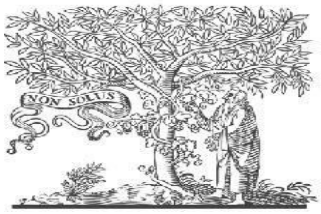

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A DC/DC VOLTAGE BOOST-UP CONVERTER USING ZERO VOLTAGE SWITCHING TECHNIQUES

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Abstract— this paper proposes a ZVS dc/dc converter with voltage boost. It offers an ongoing input and high voltage gain. Furthermore, the software feature of the proposed converter decreases active power switch loss and improves the conversion efficiency. A regulation over the current change rates of diodes by the use of the leakage induction of a coupled inductor can also mitigate the reverse recovery issue of the output rectifiers.

Index Conditions—Boost converter, soft switching, and high voltage gain.

INTRODUCTION

The demand for high voltage dc/dc converters has recently risen. Strengthening research in renewable and green sources of energy such as solar panels and fuel cells [1]–[5] has been the product of the energy shortages and air pollution. In addition, battery sources and super condensers were used to create power systems. Sadly, these sources have relatively small output voltages. The step-up power conversion in these systems is therefore important [6], [7]. In addition to stepping up, demands for different applications have increased as well as low power waves, high performance, rapid dynamics, low weight, and high power density. A high-step dc/dc converter [8], [9] is an essential function of the input current ripple. In particular, reducing the ripple input current is extremely important for fuel cell systems, as the high ripple current both shortens the fuel cell life and reduces its performance[10]–[14]. Present-fed converters are therefore widely used because they can reduce the current tension [15].

An input-start-up voltage converter (CCM) also takes advantage of its advantages, including a continuous input current and an easy structure for applications that need a stepping up voltage feature and a constant input current. But due to its parasite components, it has a small voltage gain. In addition, the output diode reverse recovery problem degrades the efficiency of the device. The reverse recovery phenomenon of the boost converter output diode is triggered when the switch is activated. The switch is provided with a high current change rate and a high reversing current peak. The parasite inductance in the current loop induces a parasite stress ringing and then increases

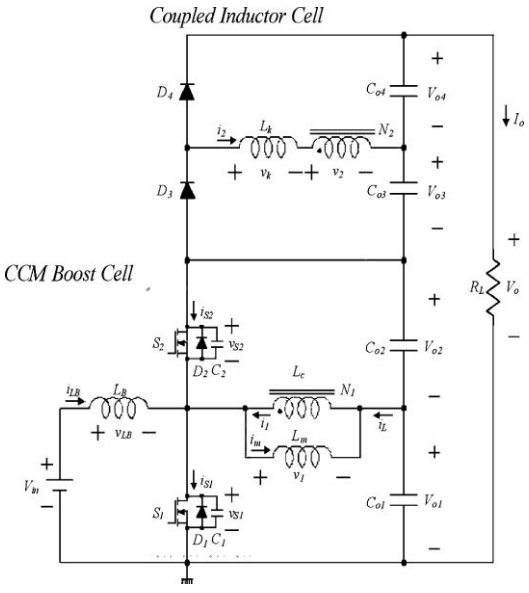

Fig. 1. Proposed dc/dc converter circuit diagram.

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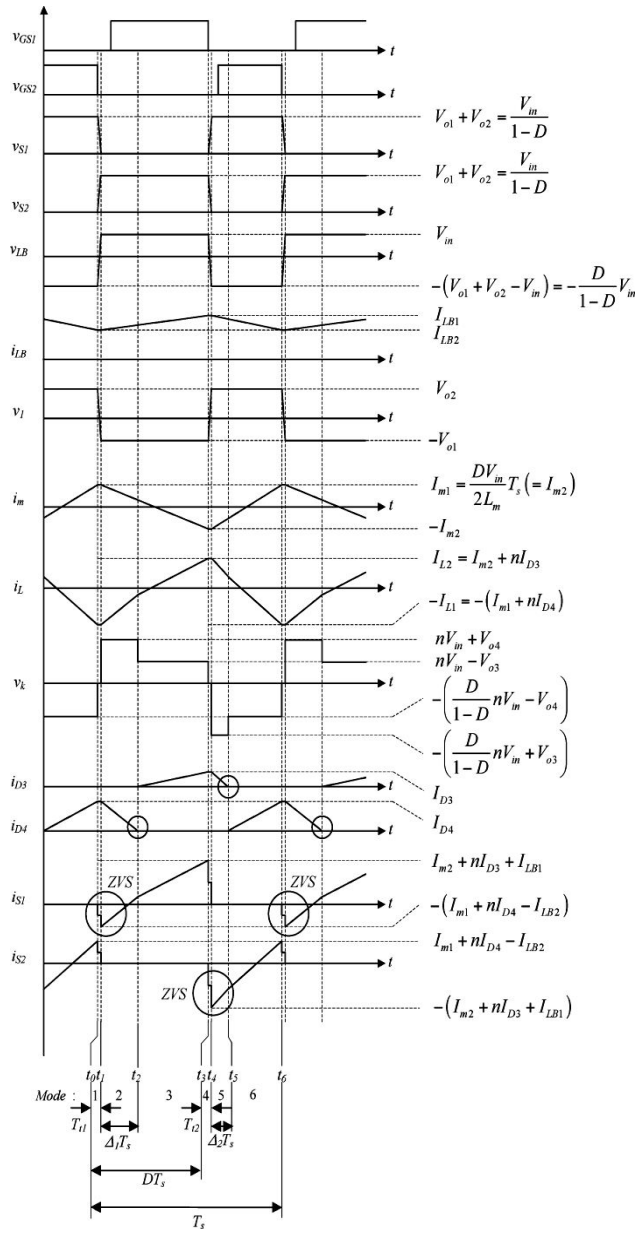
The switch and the output diode have voltage stresses. This leads considerably to increased electromagnetic interference and loss of switching. Another important consideration for dc/dc converters with high voltage gains is the reverse recovery issue for the output diodes [16] [17]. Various topologies have been introduced in order to solve these issues. The boost converters with coupled drives are given in [18] and [19] in order to increase the voltage gain. Their voltage gains are improved, but their characteristic loses a continuous input current and performance degrades because the power switches are turned hard. Present step-ups are suggested in [20] and [21] for a continuous input current. They deliver high voltage gain and shielded galvanic. The additional snubber is therefore important to minimize switch voltage. A soft switching technique in dc/dc converters [22]–[27] is required in order to increase the effectiveness and density of the power conversion.

A high voltage soft-switch dc/dc converter shown in the figure. 1, it is being implied. A CCM Boost cell gives the input current continuously. The coupling inductor cell output is mounted at the top of the cell boost output in order to maximize its voltage gain. The high voltage gain of the coupled inductor, therefore, is accomplished without high turns and the voltage of the controls are limited to the CCM boost cell's output voltage. The operation of the power switches by a Zero Voltage Switch (ZVS) decreases the switching loss during the transition and improves overall performance.



FFig. 2. Proposed converter's main waveforms.

II. ANALYSIS OF THE PROPOSED CONVERTER

The photo. 1 depicts the circuit diagram of a high-voltage high-voltage soft-changing converter. The Fig shows its main waveforms. 2. Asymmetrical operation of switches S1 and S2 is carried out and the operating ratio D is based on switch S1. Intrinsic diodes of S1 and S2, D1 and D2 are body diodes. Parasite output capacitances of S1 and S2 are C1 and C2 capacitors. A CCM boost cell is included in the proposed transformer. The components are LB,

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S1, S2, Co1 and Co2, respectively. A continuous current is given by the CCM boost cell. The boost-course iLB increases linearly from its minimum ILB2 value to its maximum ILB1 value when the shutter S1 has been activated. The current iLB decreases linearly from ILB1 to ILB2 when the switch S1 is switched off and the switch S2 is activated. The voltages Vo1 and Vo2 can therefore easily be extracted as output capacitor

$$Vo1 = Vin \qquad (1)$$

$$Vo2 = \frac{D}{1-D} V_{in} \qquad (2)$$

A coupling inductor Lc is inserted to achieve ZVS of S1 and S2 with high voltage gains. The coupled inductor Lc is modeled as Lm, Lk, and the ideal transformative with a turn ratio of 1: n (n=N2/N1). The inductive mains are used to generate Lc (Lk). The voltage doubler is made of D1, D2 diodes and Co3, Co4 and N2 secondary winding of the attached Lc inductor, at the top of the booster cell output, in order to increase voltage increase. The coupling inductor current iL ranges from its lowest IL1 to its highest IL2. The proposed converter operation can be divided into six modes in one Ts conversion cycle. The photo. 3 Displays the modes of service. The S2 and the D4 diode are powered before t0. Before t0.

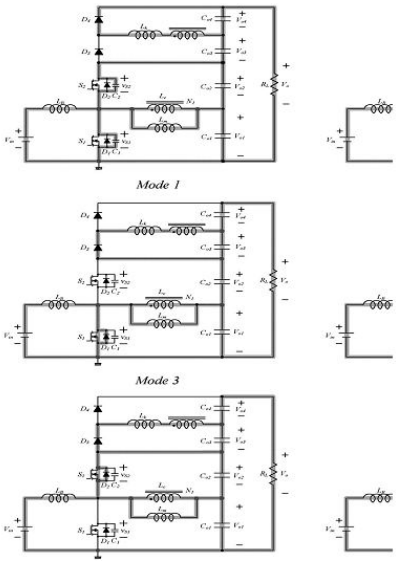

Fig. 3. Operating modes.

Mode 1 [t0, t1]: At *t*0 , Turn off the S2 switch. Then the new iLB raise and the current iL coupling begins loading C2 and loading C1. The voltage vS1 over S1 therefore begins to decrease with the voltage vS2 over S2 beginning to increase. Switches can be regarded with the Transition Interval Tt1 as

$$Tt1 = \frac{(C_1 + C_2)V_{in}}{(1 - D)(I_{L1} \,.\, I_{LB2})} \qquad (3)$$

Since the switches' output capacitances C1 and C2 are very small it is possible to ignore the transition interval Tt1. Consequently, during mode 1, constant values can be seen for inductors iLB and iL.

Mode 2 [t1, t2]: At t1, on the lower switch S1 the voltage vS1 is set to zero and on the lower diode D1. The door is then moved to the S1 turn. Since the power flows through the low D1 diode and the vS1 voltage is zero prior to switching the S1 switch, S1 turns zero. Since the voltage around the LB boosting inductor is vin, ILB2 increases the boosting inductor current linearly. Since v1 is −Vin and vk is Vo4 + nVin, the current is magnetizable in v1. The main current is i1. The secondary current is i2.

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$$i_m(t) = i_{m1} - \frac{V_{in}}{L_m}(t - t_1) \quad (4)$$

$$i_2(t) = -I_{D4} + \frac{V_{04} + nV_{in}}{L_k}(t - t_1) \quad (5)$$

$$i_1(t) = ni_2(t) = nI_{D4} + n\frac{V_{04} + nV_{in}}{L_k}(t - t_1) \quad (6)$$

$$i_L(t) = -i_m(t) + i_1(t) = -i_{m1} - nI_{D4} + \frac{V_{in}}{L_m}(t - t_1) + n\frac{V_{04} + nV_{in}}{L_k}(t - t_1) \quad (7)$$

Mode 3 [t2, t3]: At t2, i2 changes its direction from the secondary current. The current iD4 diode decreases to zero and the D4 diode is disabled. The D3 diode is switched on and its current is gradually rising. Since the current rate of D4 change is regulated by the coupling inductor leakage, it alleviates its problem with reverse recovery. As v1 is −Vin and vk is nVin − Vo4, i1 the current, i1 the current and i2 the current inductor are listed.

$$i_m(t) = i_m(t_2) - \frac{V_{in}}{L_m}(t - t_2) \quad (8)$$

$$i_2(t) = \frac{nV_{in} - V_{03}}{L_k}(t - t_2) \quad (9)$$

$$i_1(t) = ni_2(t) = n\frac{nV_{in} - V_{03}}{L_k}(t - t_2) \quad (10)$$

$$i_L(t) = -i_m(t) + i_1(t) = -i_m(t_2) + \frac{V_{in}}{L_m}(t - t_2) + n\frac{nV_{in} - V_{03}}{L_k}(t - t_2) \quad (11)$$

Mode 4 [t3, t4]: At t3, you disable the lower switch S1. Then the current iLB boost and the current iL coupling inductor start loading C1 and loading C2. The Voltages vS1 and vS2 therefore continue to increase and decrease in a way similar to mode 1. Switches can be seen as the phase interval Tt2.

$$T_{t2} = \frac{(C_1 + C_2)V_{in}}{(1 - D)(I_{L2} - I_{LB1})} \quad (12)$$

Tt2 is trivial, too. Therefore, iLB and iL inductor currents during Tt2 can be regarded as having constant values.

Mode 5 [t4, t5]: At t4, the voltage vS2 through the top of the button S2 is zero and the diode D2 is triggered. The door signal is then added to the S2 switch. The voltage vS2 is zero until the switch S2 is switched on, which means that the current has already fled the diode D3 and S2's zero voltage switch on. The voltage over the booster inducer LB −(Vin/(1 − D) − Vin) is therefore decreased by the booster inductor current linear from ILB1. The current inductive current im, primary current i1, secondary current i2, and the current inductor iL is given since v1 is DVin/(1 - D) and vk is −Vo3 − nDVin/(1 − D).

$$i_m(t) = -i_{m2} + \frac{DV_{in}}{L_m(1 - D)}(t - t_4) \quad (13)$$

$$i_2(t) = I_{D3} - \frac{V_{03} + (D/1 - D)nV_{in}}{L_k}(t - t_4) \quad (14)$$

$$i_1(t) = ni_2(t) = \text{n } I_{D3} - n\frac{V_{03} + (D/1 - D)nV_{in}}{L_k}(t - t_4) \quad (15)$$

$$i_L(t) = i_{m2} + ni_{D3} - \left(\frac{DV_{in}}{L_m(1 - D)} + nn\frac{V_{03} + (D/1 - D)nV_{in}}{L_k}\right)(t - t_4) \quad (16)$$

Mode 6 [t5, t6]: At t5, i2 changes the direction of the secondary current. The iD3 diode is reduced to zero and the D3 diode is disabled. The problem with D3 reverse recovery is also minimized by Lc's leakage induction. The diode D4 is then activated, with its current rising linearly. Since v1 is DVin/(1 − D) and

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vk is Vo4 − nDVin/(1 − D), the current im, the primary current i1 is i2, and iL is i1.

$$i_m(t) = -i_m(t_5) + \frac{DV_{in}}{L_m(1-D)}(t - t_5)$$

(17)

$$i_2(t) = -\frac{(D/1-D)nV_{in} - V_{04}}{L_k}(t - t_5)$$

(18)

$$i_1(t) = ni_2(t) = -n\frac{(D/1-D)nV_{in} - V_{04}}{L_k}(t - t_5)$$

(19)

$$i_L(t) = -i_m(t_5)$$

$$-\left(\frac{DV_{in}}{L_m(1-D)} + nn\frac{V_{03} + (D/1-D)nV_{in}}{L_k}\right)(t - t_5)$$

(20)

The average values of *vLB* and *v*1, *Vo*1 can be considered to be *V*in. Referring to the voltage waveforms *vLB* in Fig. 2, the volt–second balance law gives

$$V\text{in}DTs - (Vo1 + Vo2 - V\text{in})(1 - D)Ts = 0. \quad (21)$$

From modes 3 and 5, the current *I*D3 can be written as follows:

$$I_{D3} = \frac{nV_{in} - V_{03}}{L_k}(D - \Delta_1)T_s$$

$$= \frac{V_{03} + \left(D/1 - D\right)nV_{in}}{L_k}\Delta_2 T_s$$

(22)

from where, the output voltage *Vo*3 can be obtained by

$$V_{03} = \frac{D - \Delta_1 - (D/1-D)\Delta_2}{D - \Delta_1 + \Delta_2}nV_{in} \quad (23)$$

From modes 2 and 6, the current *I*D4 can be written as follows:

$$I_{D4} = \frac{nV_{in} + V_{04}}{L_k}(\Delta_1)T_s$$

$$= \frac{-V_{04} + (D/1-D)nV_{in}}{L_k}((1-D) - \Delta_2)T_s$$

(24)

From where, the output voltage *Vo*4 can be obtained by

$$V_{04} = \frac{D - \Delta_1 - (D/1-D)\Delta_2}{1 - D + \Delta_1 - \Delta_2}nV_{in} \quad (25)$$

Since the average value of the current *i*2 is zero, the following relation can be obtained:

$$(D - \Delta 1 + \Delta 2)\, I\text{D3} = (1 - D + \Delta 1 - \Delta 2)\, I\text{D4}. \quad (26)$$

From (22), (24), (25), and (26), the relation between Δ1 and
Δ2 is obtained by

$$\frac{\Delta_1}{\Delta_2} = \frac{D}{1-D} \quad (27)$$

Since the average value of the current *im* is zero, its peak
Values *Im*1 and *Im*2 have the following values:

$$Im1 = Im2 = \frac{DV_{in}T_s}{2L_m} \quad (28)$$

The output current *Io* in Fig. 1 can be represented by

$$Io = (D - \Delta 1 + \Delta 2)\frac{I_{D3}}{2} = (1 - D + \Delta 1 - \Delta 2)\frac{I_{D4}}{2}. \quad (29)$$

From (22), (27), and (29), Δ1 and Δ2 are obtained by

$$\Delta 1 = \alpha D \quad (30)$$

$$\Delta 2 = \alpha\,(1 - D) \quad (31)$$

where

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$$\alpha = \frac{1}{2}\left(1 - \sqrt{1 - \frac{8L_k I_0}{nDV_{in}T_s}}\right)$$

III. CHARACTERISTIC AND DESIGN PARAMETERS

A. Input Current Ripple

The input current ripple ΔILB can be written as

$$\Delta ILB = ILB1 - ILB2 = \frac{DV_{in}T_s}{L_B}. \quad (32)$$

To reduce the input current ripple ΔILB below a specific value I^*, the inductor LB should satisfy the following condition:

$$LB > \frac{DV_{in}T_s}{I^*} \quad (33)$$

B. Voltage Gain

From (1), (2), (23), (25), (27), (30), and (31), the voltage gain of the proposed converter is obtained by

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} + \frac{nD(1-\alpha)}{(D-\alpha(2D-1))(1-D+\alpha(2D-1))}$$

(34)

$$\frac{V_o}{V_{in}} = \frac{1+n}{1-D} \quad (35)$$

C. ZVS Condition

The ZVS condition for S2 is given by

$$Im2 + nID3 + ILB1 > 0 \quad (36)$$

From where, it can be seen that the ZVS of S2 is easily obtained. For ZVS of S1, the following condition should be satisfied:

$$Im1 + nID4 > ILB2. \quad (37)$$

On the assumption that α is small, $ID4$ and $ILB2$ can be simplified as follows:

$$I_{D4} = \frac{2I_o}{1-D} \quad (38)$$

$$I_{LB2} = \frac{(n+1)I_o}{1-D} - \frac{\Delta I_{LB}}{2} \quad (39)$$

From (38) and (39), the inequality (37) can be rewritten by

$$I_{m1} + \frac{2nI_o}{1-D} > \frac{\Delta I_{LB}}{2} + \frac{(n+1)I_o}{1-D} - \frac{\Delta I_{LB}}{2} \quad (40)$$

Provided the positive values of Im1, Io, and DILB, inequality (40) still satisfies n>1. The ZVS conditions for S1 and S2 can be observed from (36) and (40) onwards. In addition, dead times should be found for two S1 and S2 switches. Before the current that runs through the anti-parallel diode changes direction, the gate signal should be applied to the switch. The leachage inductance Lk, that is, is adequate to hold the current in the direction of two switches, S1 and S2, during dead times. The minimum leakage value may be calculated by this condition inductance. From (30), the leakage inductance Lk should satisfy the following condition:

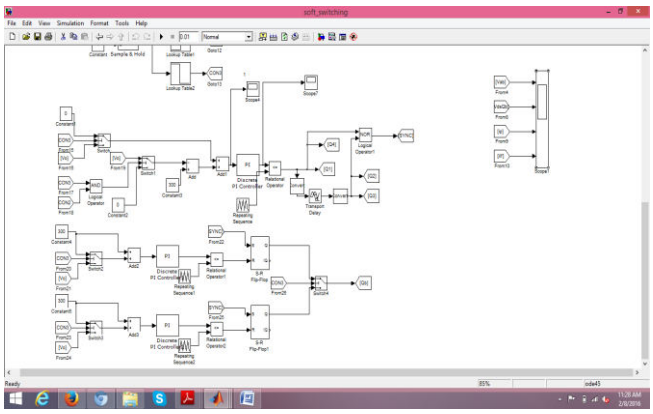
$$L_k > \frac{nV_{in}DT_s}{8I_o}\left[1 - \left(1 - \frac{2\Delta 1^*}{D}\right)^2\right]$$

(41)

Where $\Delta * 1$ is a predetermined minimum value of$\Delta 1$. The leakage inductance of the coupled inductor also alleviates the reverse recovery problem of output diode. Large leakage inductance can remove the reverse-recovery problem but it reduces the voltage gain as shown in Fig. 4(b).

III. Simulation Results

Simulink Model



Control diagram

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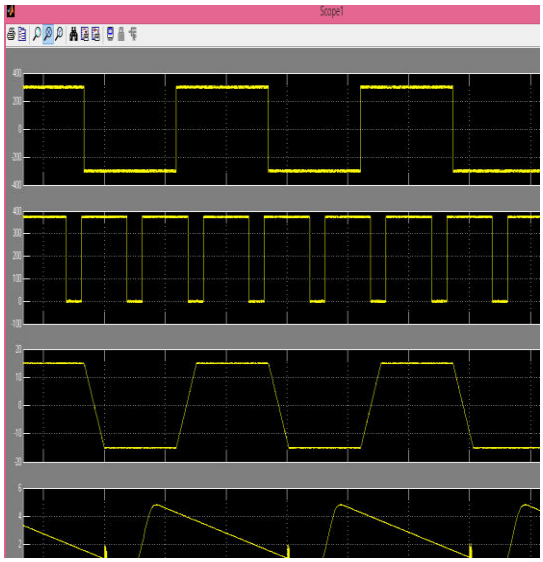
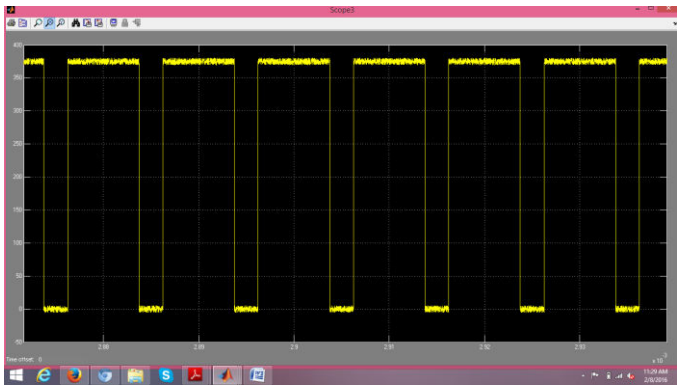
Simulink Results



1.Vab 2.VdsQb 3.ip 4.ilf

Control diagram



Upper mosfet Source to drain voltage

IV. CONCLUSION

A soft-switching dc/dc converter with high voltage gain has been proposed in this paper. The proposed converter can minimize the voltage stresses of the switching devices and lower the turn ratio of the coupled inductor. It provides a continuous input current, and the ripple components of the input current can be controlled by using the inductance of the CCM boost cell. Soft switching of power switches and the alleviated reverse-recovery problem of the output rectifiers improve the overall efficiency.

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