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A THREE PHASE MULTILEVEL INVERTER WITH REDUCED NUMBER OF DEVICES FOR INDUCTION MOTOR DRIVE

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ABSTRACT- Multilevel inverter offer high power capability, associated with lower output harmonics and lower commutation losses. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. This paper proposes a multilevel inverter with reduced number of switches for induction motor drive application, multilevel inverter with reduced number of switches. The inverter is capable of producing levels of output-voltage levels from the dc supply voltage. This paper proposes a new multilevel inverter topology using reduced number of auxiliary switches. The new topology produces a significant reduction in the number of power devices and switches required to implement a multilevel output using the induction motor applications. The inverter is capable of producing levels of output-voltage levels from the dc supply voltage. This paper proposes a new multilevel inverter topology using reduced number of auxiliary switches. Reduction in overall part count as compared to the classical topologies has been an important objective in the recently introduced topologies. In this paper, some of the recently proposed multilevel inverter topologies with reduced power switch count are reviewed and analyzed. The paper will serve as an introduction and an update to these topologies, both in terms of the qualitative and quantitative parameters. Multilevel inverters are used in high voltage AC motor drive, distributive generation, high voltage direct transmission as well as SVC applications. The concept of an MLI to achieve higher power is to use power semiconductor switches along with several lower voltage dc levels to perform the power conversion by synthesizing a staircase voltage levels. And also Extension of this paper is Single phase topology is extended to three phase topology and fed with an induction motor drive.

KEYWORDS: Even power distribution, fundamental switching frequency operation, multilevel inverters (MLI), reduced device count, source configuration.

I. INTRODUCTION

In the industries, the applications like mills, laminators, conveyors, fans and pumps etc require high power and medium voltage. Such a high power applications the multilevel inverter (MLI) [2-3] topology is extending the usage because of its own advantages. The conventional square wave inverter produces more harmonics and in multilevel inverter the output voltage wave shape is nearly sinusoidal with number of levels. The advantages of multilevel inverter are listed below.

1. The stress of the motor is reduced and protects the motor against damage.
2. Multilevel inverters draw the current from source with less distortion.
3. These can operate at high as well as lower frequencies.

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4. The total harmonic distortion (THD) is less in the output voltage wave form without using any filter.

Owing to these advantages different types of multilevel inverters are introduced in to the market such as diode clamped type, flying capacitor type and cascaded multilevel inverter. The diode clamped and flying capacitor type multilevel inverters need more number of diodes and capacitors. So, most commonly used topology is the cascade H-Bridge inverter topology. The number of levels can be increased by increasing the number of H-Bridges by using the formula number of levels= 2n+1. Here, n is the number of H-Bridges. In CHB also there are two configurations like symmetrical and asymmetrical. When the magnitude of dc voltage source is same in each bridge, then that configuration is called symmetrical and if the magnitude of dc voltage source is not equal it is called as asymmetrical configuration. For the same number of bridges, the asymmetrical configuration gives more levels as compared to symmetrical configuration. The series-parallel connection of voltage sources in each bridge is also developed to get the more voltage levels.In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, static VAR compensators and renewable energy systems. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters. This paper presents an optimized configuration of a3-phase MLI with minimum number of switches. To overcome the disadvantages this paper proposes anew multilevel inverter topology with reduced switches compared to conventional MLIs. Finally the induction motor fed by the proposed MLI is presented in this paper.

Multilevel DC to AC Conversion and Classical Topologies

The multilevel approach for dc to ac conversion offers many advantages such as [5]–[10]:

1) The staircase waveform not only exhibits a better harmonic profile but also reduces the *dv/dt* stresses. Thus, the filter requirements can be greatly brought down (or even eliminated), while electromagnetic compatibility problems can be reduced.

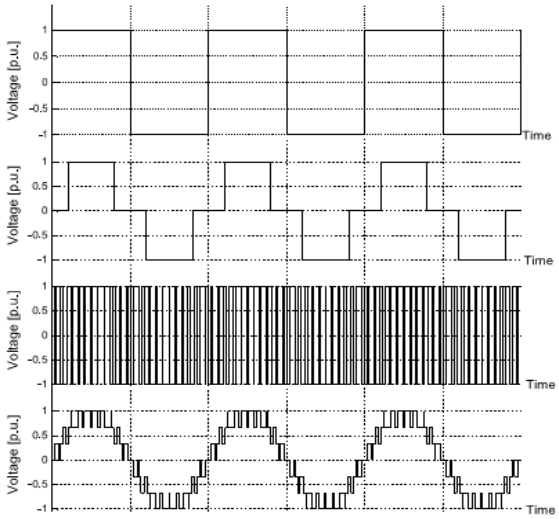

Fig.1. Typical inverter waveforms: (a) Square wave. (b) Quasi-square wave. (c) Two-level PWM waveform. (d) Multilevel PWM waveform.

2) The voltage stresses on the semiconductor devices are much lesser as compared to the overall operating voltage. Thus, a high-voltage waveform can be obtained with comparatively low-voltage rated switches.

3) MLIs produce much smaller common mode voltage and thus, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.

4) Many multilevel topologies offer the possibility to obtain a given voltage level with multiple switching combinations. These redundant states can be utilized to program a fault tolerant operation.

5) MLIs can draw input current with low distortion.

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6) Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system and can be controlled for equal load sharing amongst the input sources.Over the past few decades, MLIs have attracted wide interest both in the research community and in the industry, as they are becoming a viable technology for many applications. In the mid 1970s, the first patent describing a converter topology capable of producing multilevel voltage from various dc voltage sources was published by Baker and Bannister . The topology consists of single-phase inverters connected in series as depicted in Fig.2, and it is known as series-connected H-bridge inverter, or cascaded H-bridge (CHB) inverter.

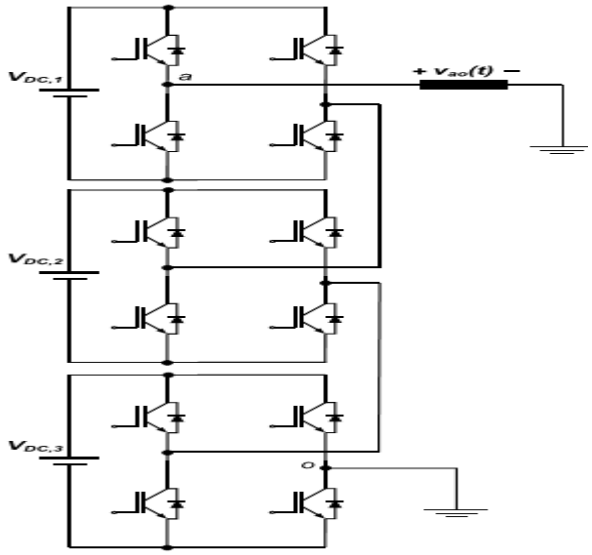

Fig.2. CHB structure for MLIs.

In another patent by Baker [12] in 1980, a modified multilevel topology was introduced, for which three-level and five-level versions are illustrated in Fig.4.3 (a) and (b), respectively. In contrast to the CHB inverters, this converter can produce multilevel voltage from a single dc source with extra diodes connected to the neutral point. This topology is now widely referred to as the neutral point clamped (NPC) inverter and/or diode clamped topology. In 1980, Nabae et al. [13] demonstrated the implementation of NPC inverter using a PWM scheme. In the 1980s, much of the research was focused only on three-level inverters. The so-called flying capacitor (FC) was introduced in the 1990s by Meynard and Foch [14] and Lavieville et al. [15]. The topology of the FC inverter is depicted in Fig.4 (a) for three-level and in Fig.4.4 (b) for five-level applications. Much of the literature published in past few decades have shown intense focus in studying the diode clamped, FCs and CHB topologies with regards to their respective pros and cons [5], [16]–[34], and these topologies are now widely referred to as the "classical topologies."

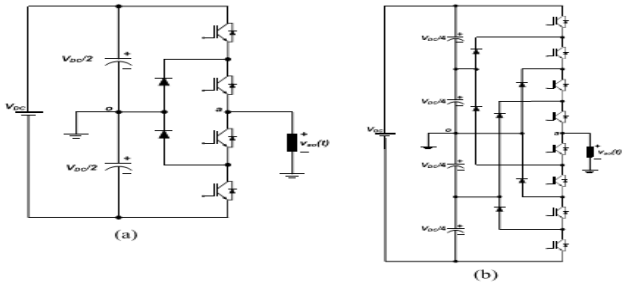

Fig.3. One leg of neutral-point /diode-clamped structure; (a) three-level; and (b) five-level.

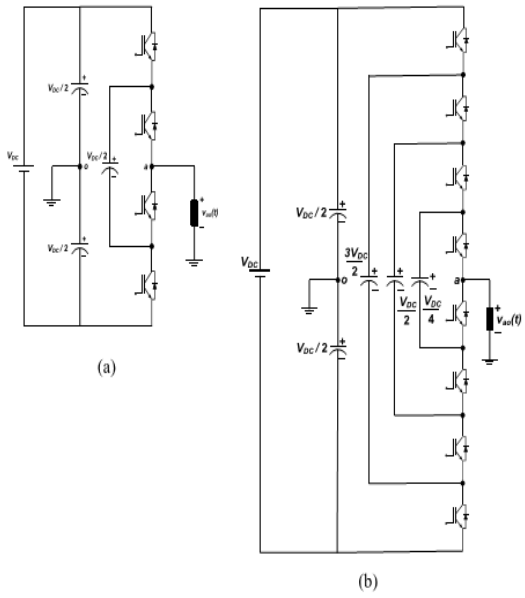

Fig.4. One leg of flying capacitor structure; (a) three-level; and (b) five-level.

Advent of New Topologies With Application-Oriented Approach

The so-called "classical topologies" have attracted maximum attention both from the academia and industry. Still, no specific topology seems to be absolutely advantageous as multilevel solutions are heavily influenced by application and cost considerations. Because of its intrinsic characteristics, a given topology can be very well adapted in some cases and totally unsuitable in some others. Therefore, the optimal solution is often recommended on case-to-case basis. Hence, along with the exploration of classical topologies, researchers continued (and still continue) to evolve newer topologies with an application oriented approach. In this subsection, some of such contributions are discussed.

Topologies with Reduced Device Count and Scope of This Paper

In view of their many advantages, MLIs are receiving much more and wider attention both in terms of topologies and control schemes. MLIs, however, exhibit an important limitation—for an increased number of output levels, they require a large number of power semiconductor switches, thereby increasing the cost, volume, and control complexity. Although low-voltage rated switches can be utilized in an MLI, each switch requires a related gate driver unit, protection circuit, and heat sink. This may cause the overall system to be more expensive, bulky, and complex. Consequently, for past few years, efforts are being directed to reduce the power switch count in MLIs and a large number of topologies have appeared in the literature. These topologies have their own merits and demerits from the point of view of application requirements. As of now, no literature is available which comprehensively reviews the aforementioned topologies, thereby stipulating their comparative advantages and limitations. This paper aims at presenting a review of MLI topologies proposed with the exclusive objective of reducing the power switch count. Analysis of these topologies has been specifically carried out in terms of: count of power semiconductor components, total voltage blocking capability requirement, possibility of even power distribution amongst the input dc sources, possibility of optimal distribution of switching frequency amongst the power switches, and possibility of employing asymmetric sources. In addition, this paper provides a list of appropriate references in relation to MLI topologies and their control. Although the development of topologies has been accompanied with advancement in modulation schemes, this paper focuses only on the topological features and their consequences.

Terminology, Assessment Parameters, and Classification of Topologies

Prior to a comparative analysis of topologies, some terms pertaining to the assessment criteria are defined. Thereafter, various criteria to assess reduced device count topologies are discussed, and a classification of the topologies is presented so that a broad outline can be drawn.

Terminology

1) Reduced Device Count Multilevel Inverter (RDC-MLI) Topologies: Topologies which are proposed/presented with an exclusive claim of reducing the number of controlled switching power semiconductor devices for a given number of phase voltage levels are referred to as RDC-MLI topologies. In this paper, nine such topologies are reviewed.

2) Total Voltage Blocking Capability: For a topology, the total sum of the voltage blocking capability requirement for all its

power switches is referred to as the "total voltage blocking capability" . For example, if a structure consists of four switches rated at V_{DC} and six switches rated at $2V_{DC}$, the total voltage blocking capability requirement would be:

$$[(4 \times V_{DC}) + (6 \times 2V_{DC}) = 16V_{DC}]$$

3) Symmetric and Asymmetric Source Configuration: When the voltages of the input dc levels to an MLI are all equal, the source configuration is known as "symmetric," otherwise "asymmetric" [59]. Two popular asymmetric source configurations are: binary and trinary. In binary configuration, values of voltage levels are in geometric progression (GP) with a factor of "2" (i.e. V_{DC}, $2V_{DC}$, $4V_{DC}$, $8V_{DC}$...), while in trinary configuration the GP factor is "3" (i.e., V_{DC}, $3V_{DC}$, $9V_{DC}$, $27V_{DC}$...). There are many other asymmetric source configurations proposed by various researchers [44]. An asymmetric source configuration is employed to synthesize more number of output levels with the same count of power switches.

4) Even Power Distribution: When the multilevel dc to ac conversion is carried out in such a way that each input source contributes equal power to the load, the "power distribution" amongst the sources is said to be "even." Some authors also refer to it as "charge balance control" or "equal load sharing" . "Even power distribution" is a feature of control aspect, only when the topology permits so. When the source configuration is symmetric, the control algorithm is designed such that the average current drawn from each source is equal, thereby making average powers equal. For a given topology, even power distribution is possible if each input source contributes toward all the output levels in one or more output cycles. For example, if a topology has three symmetric input dc sources $V_{DC, 1}$, $V_{DC, 2}$, and $V_{DC, 3}$ ($V_{DC, 1} = V_{DC, 2} = V_{DC, 3} = V_{DC}$), then even power distribution is possible if all the combinations.

5) Level-Generation and Polarity-Generation: An MLI synthesizes a stepped waveform consisting of the input dc levels and their additive and/or subtractive combinations. Thus, the voltage waveform consists of multiple "levels" with both "positive" and "negative" polarities (in positive and negative half cycles, respectively). Many a times, an MLI circuit is such that a part of it synthesizes the multiple levels with only one polarity and an H-bridge is used to convert this single polarity waveform to a bipolar one for the ac load. These parts are, respectively, referred to as "level-generation part" and "polarity-generation part" [66]. It is important to mention here that the power switches for the polarity generation part need to have a minimum voltage rating equal to the operating voltage of the MLI.

6) Fundamental Frequency Switching: The switching losses in a converter are proportional to the current, blocking voltage, and switching frequency [68]. To minimize the switching losses, it is preferred to operate higher voltage-rated power switches at a low frequency and if possible, at the power frequency (or fundamental frequency), without compromising the quality of output waveform. A power switch in a topology can operate at fundamental switching frequency if it remains ON for one complete half cycle (either positive or negative) and remains OFF for the next complete half cycle, while the desired multilevel waveform is synthesized at the load terminals. Thus, fundamental frequency switching frequency is a control feature of modulation scheme provided the topology permits so. In addition, when a topology consists of power switches with different voltage ratings, in order to properly

distribute the switching losses, the higher voltage rated switches should be operated at comparatively lower switching frequencies while those with lower voltage rating should be operated with comparatively higher switching frequencies. Thus, the switching frequency should be calculatedly "distributed" if the topology offers such a possibility. Also, if the level generation part of a topology can synthesize the zero level, then switches of polarity generation can be operated at the line frequency.

Assessment Parameters

Merit of any given topology can be primarily judged based on the application for which it has to be employed. Still, in the context of this paper, the general criteria for an overall assessment of the merit of an RDC-MLI and its comparison with the other topologies can be:

1) The number of power switches used;
2) The total blocking voltage of the converter;
3) The optimal controllability of the topology, in terms of the possibilities of charge-balance control (or "even power distribution" amongst the input sources) and appropriate distribution of switching frequencies amongst the differently voltage-rated switches;
4) Possibility of employing asymmetric sources/capacitor voltage ratios in the topology.

While parameters 1 and 2 affect reliability of the inverter, efficiency is influenced by parameters 1, 2, and 3 and application, performance, and control complexity are governed by parameter 3. Number of redundant states and consequently, programmability of fault tolerant operation, is directly influenced by 1 and 4. In addition, apart from 1 and 2, the cost of a converter also depends on the dispersion of power switching ratings (e.g., using one 400 V switch and one 800 V switch would be, in principle, more expensive than using two 600 V switches).

Categorization of RDC-MLI Topologies

In this paper, nine different RDC-MLI topologies, as proposed in [50]–[68], are evaluated. These topologies are enlisted as follows.

1) cascaded half-bridge-based multilevel dc-Link (MLDCL) inverter [50], [51];
2) T-type Inverter [52]–[54];
3) switched series/parallel sources (SSPS)-based MLI [55], [56];
4) series-connected switched sources (SCSS)-based MLI [57], [58];
5) Cascaded "bipolar switched cells" (CBSC)-based MLI [59];
6) packed-U cell (PUC) topology [60]–[64];
7) Multilevel module (MLM)-based MLI [65];
8) Reversing voltage (RV) topology [66], [67];
9) two-switch enabled level-generation (2SELG)-based MLI [68].

While a detailed analysis of these topologies is presented, it is important to appreciate that there are several similarities between the different RDC-MLI topologies which can be clearly seen if they are drawn with a similar structure, without taking into account the actual power switch configurations. For example, as shown in Fig.5 (a) and (b), it can be observed that the PUC topology is equivalent to the FC structure without dc sources. As indicated in Fig.5 (c) and (d), the T-type inverter [52]–[54] and CBSC-based MLI [59] have similar units. The 2SELG-based MLI [68] consists of repeated connection of the units used in MLM-based MLI [65] as shown in Fig.4.5 (e) and (f). Similarly, the topologies proposed in [50], [55], [57], and [66] consist of similar arrays of sources and switches connected in various fashions, as depicted in Fig.5 (g), (h),

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(i), and (j). With the help of Fig.5, it can be observed that the RDC-MLI topologies can be classified as those with H-bridge and those without H-bridge. In addition, these topologies may need isolated input dc levels or non isolated input dc levels. Thus, a broad categorization of RDC-MLI topologies is presented in Fig.6.

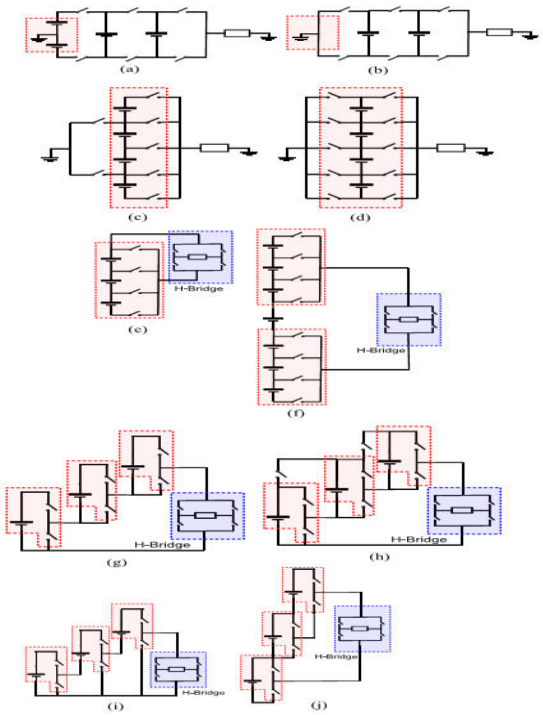

Fig.5. Similarities in the structures of various topologies.

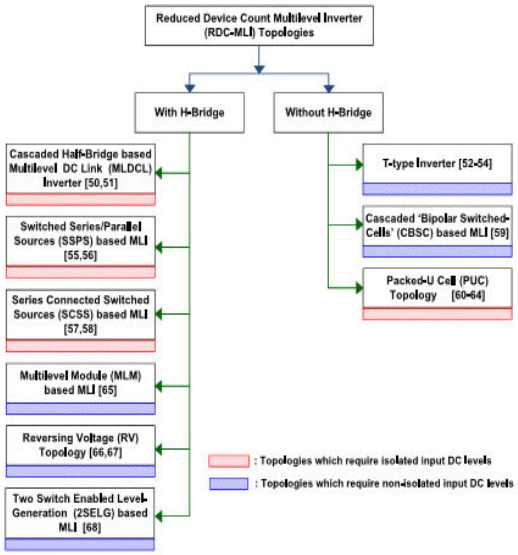

Fig.6 Categorization of RDC-MLI topologies.

II. Review of MLI Topologies with Reduced Device Count

In this section, nine RDC-MLIs are reviewed and based on the parameters mentioned; topologies with reduced device count are discussed in this section. The topologies are presented in their single-phase form for the sake of simplicity. Their overall comparison, however, is carried out in terms of three-phase implementation, because MLIs are mostly administered in three-phase configurations. In addition, the illustrations for these topologies are indicated with four input sources and various valid switching states are tabulated. For the TCSMLDCL inverter, however, seven sources are shown so that its general structure can be comprehended.

(A) Cascaded Half-Bridge-Based MLDCL Inverter

Su [50], [51] has presented a new MLI named as "Cascaded Half-Bridge-based MLDCL inverter." An MLDCL inverter with four input dc levels is shown in Fig.4.7. It comprises of cascaded half-bridge cells, with each cell having its own dc source. It has separate "level-generation" and "polarity generation" parts. The level-generation part comprises of the sources $V_{DC,j}\{j=1,2,3,4\}$and the power switches $S_j\{j= 1to8\}$. This part synthesizes a multilevel dc voltage, $v_{bus}(t)$, fed to the "polarity-generation" part, comprising of switches $Q_j\{j=1to4\}$, which in turn alternates the polarity to produce a multilevel ac waveform.

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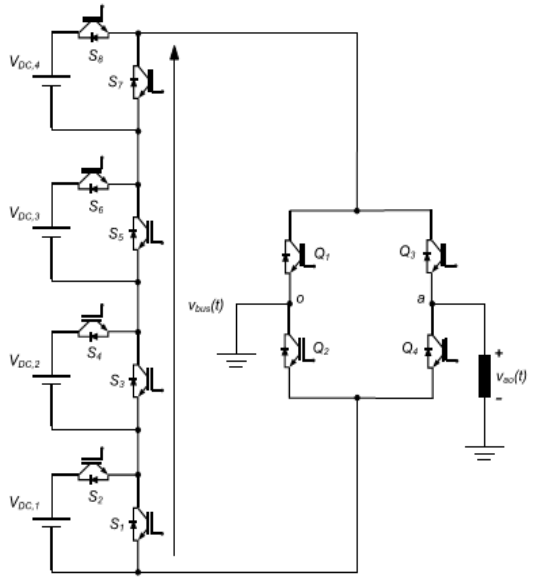

Fig.7 Cascaded half-bridge-based MLDCL inverter as proposed.

The level-generation part and two switches conduct for the polarity-generation part (switches Q_1 and Q_4 for the positive half cycle, Q_2 and Q_3 for the negative half cycle, and Q_1, Q_3/Q_2, Q_4 for the zero level). It can be observed from the topology that each power switch of polarity-generation part must possess a minimum voltage blocking capability equal to the sum of the input voltage values. Thus, these switches are rated higher as compared to the switches in the level-generation part. However, since the zero level can be synthesized using switches of the polarity-generation part, the higher rated switches $Q_j\{j=1to4\}$can be operated at fundamental switching frequency.

For a symmetric source configuration with $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$, it can be observed that the switches $S_j\{j=1to8\}$need to block a voltage of V_{DC} and need to conduct a current equal to the load current while the switches $Q_j\{j=1to4\}$need to block a voltage equal to $4V_{DC}$ and conduct a current equal to the load current. Moreover, it can be observed from Table III that since voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$, and $4V_{DC}$ can be synthesized combining all the input sources in groups of one, two, and three, respectively, equal load sharing amongst them is possible. These redundancies also provide flexibility in voltage balancing, in case capacitors are used.

Regarding asymmetric source configurations in the MLDCL topology, no comments are offered in [50] and [51]. Since subtractive combinations of the input dc levels cannot be synthesized, the trinary source configuration cannot be employed for this topology. As it can be observed from Table III, a binary source configuration with $V_{DC,1} = V_{DC}$, $v_{DC,2} = 2V_{DC}$, $V_{DC,3} = 4V_{DC}$, and $V_{DC,4} = 8V_{DC}$ is possible since the voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$, $5V_{DC}$, $6V_{DC}$,...,$15V_{DC}$ can be synthesized by utilizing the states presented.

As suggested by the author in [50] and [51], one application area in the low-power range (<100 kW) for the MLDCL inverters is in the permanent-magnet (PM) motor drives employing a PM motor of very low inductance. The level-generation part can utilize the fast-switching low-cost low-voltage MOSFETs and the polarity-generation part can use IGBTs so as to dramatically reduce the current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. The MLDCL inverter can also be applied in distributed power generation involving fuel cells and photovoltaic cells.

TABLE I

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_2, S_3, S_5, S_7
2	$V_{DC,2}$	S_1, S_4, S_5, S_7
3	$V_{DC,3}$	S_1, S_3, S_6, S_7
4	$V_{DC,4}$	S_1, S_3, S_5, S_8
5	$V_{DC,1} + V_{DC,2}$	S_2, S_4, S_5, S_7
6	$V_{DC,1} + V_{DC,3}$	S_2, S_3, S_6, S_7
7	$V_{DC,1} + V_{DC,4}$	S_2, S_3, S_5, S_8
8	$V_{DC,2} + V_{DC,3}$	S_1, S_4, S_6, S_7
9	$V_{DC,2} + V_{DC,4}$	S_1, S_4, S_5, S_8
10	$V_{DC,3} + V_{DC,4}$	S_1, S_3, S_6, S_8
11	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_2, S_4, S_6, S_7
12	$V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_1, S_4, S_6, S_8
13	$V_{DC,1} + V_{DC,3} + V_{DC,4}$	S_2, S_3, S_6, S_8
14	$V_{DC,1} + V_{DC,2} + V_{DC,4}$	S_2, S_4, S_5, S_8
15	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_2, S_4, S_6, S_8
16	0	S_1, S_3, S_5, S_7

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(B) T-Type Inverter

Cegliaet al. [52]–[54] reported a new MLI topology, herewith referred to as the "T-type inverter." The primary introduction to the topology is described in [52] with the help of a five-level single-phase inverter which results in a significant reduction in the number of power devices as compared to the conventional topologies. A single-phase structure of the topology with four input voltage sources is shown in Fig.8. It comprises of three switches $S_j\{j=1,2,3\}$which are bidirectional blocking-bidirectional-conducting while four switches $Q_j\{j=1to4\}$are unidirectional-blocking-bidirectional-conducting.Thus, this topology inadvertently requires a mix of unidirectional and bidirectional power switches. Valid switching states for the inverter are summarized, and it can be seen that the input dc values are required to be symmetric, i.e. $V_{DC,1}$ =$V_{DC,2}$ =$V_{DC,3}$ =$V_{DC,4}$ =V_{DC}. This is so because not all the additive/subtractive combinations of the input voltage levels can be synthesized at the load terminals and many times either a positive or negative combination can be synthesized but not both. For example, while a voltage level−$V_{DC,4}$ can be synthesized at the load terminals, the level+$V_{DC,4}$ cannot be synthesized. Thus, it is imperative that the input sources are symmetric. Also, lack of sufficient redundancies goes against an effective voltage balancing.

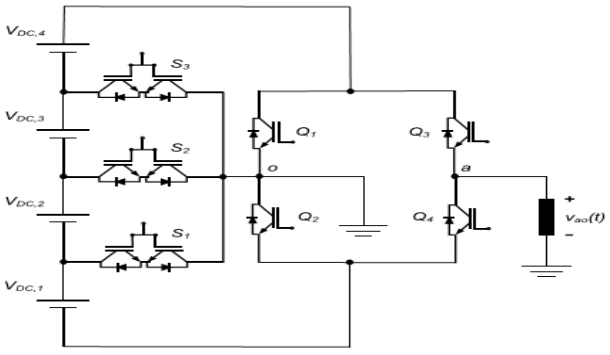

Fig.8. T-type inverter as proposed

TABLE II

State	Output voltage [$v_{ao}(t)$]	Switches in ON state
1	$-V_{DC,1}$	S_1, Q_4
2	$V_{DC,4}$	S_3, Q_3
3	$-(V_{DC,1}+V_{DC,2})$	S_2, Q_4
4	$V_{DC,3}+V_{DC,4}$	S_2, Q_3
5	$-(V_{DC,1}+V_{DC,2}+V_{DC,3})$	S_3, Q_4
6	$V_{DC,2}+V_{DC,3}+V_{DC,4}$	S_1, Q_3
7	$-(V_{DC,1}+V_{DC,2}+V_{DC,3}+V_{DC,4})$	Q_1, Q_4
8	$V_{DC,1}+V_{DC,2}+V_{DC,3}+V_{DC,4}$	Q_2, Q_3
9	0	Q_1, Q_3
10	0	Q_2, Q_4

III. INDUCTION MOTOR

An asynchronous motor type of an induction motor is an AC electric motor in which the electric current in the rotor needed to produce torque is obtained by electromagnetic induction from the magnetic field of the stator winding. An induction motor can therefore be made without electrical connections to the rotor as are found in universal, DC and synchronous motors. An asynchronous motor's rotor can be either wound type or squirrel-cage type.Three-phase squirrel-cage asynchronous motors are widely used in industrial drives because they are rugged, reliable and economical. Single-phase induction motors are used extensively for smaller loads, such as household appliances like fans. Although traditionally used in fixed-speed service, induction motors are increasingly being used with variable-frequency drives (VFDs) in variable-speed service. VFDs offer especially important energy savings opportunities for existing and prospective induction motors in variable-torque centrifugal fan, pump and compressor load applications. Squirrel cage induction motors are very widely used in both fixed-speed and variable-frequency drive (VFD)

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applications. Variable voltage and variable frequency drives are also used in variable-speed service.In both induction and synchronous motors, the AC power supplied to the motor's stator creates a magnetic field that rotates in time with the AC oscillations. Whereas a synchronous motor's rotor turns at the same rate as the stator field, an induction motor's rotor rotates at a slower speed than the stator field. The induction motor stator's magnetic field is therefore changing or rotating relative to the rotor. This induces an opposing current in the induction motor's rotor, in effect the motor's secondary winding, when the latter is short-circuited or closed through external impedance. The rotating magnetic flux induces currents in the windings of the rotor; in a manner similar to currents induced in a transformer's secondary winding(s). The currents in the rotor windings in turn create magnetic fields in the rotor that react against the stator field. Due to Lenz's Law, the direction of the magnetic field created will be such as to oppose the change in current through the rotor windings. The cause of induced current in the rotor windings is the rotating stator magnetic field, so to oppose the change in rotor-winding currents the rotor will start to rotate in the direction of the rotating stator magnetic field. The rotor accelerates until the magnitude of induced rotor current and torque balances the applied load. Since rotation at synchronous speed would result in no induced rotor current, an induction motor always operates slower than synchronous speed. The difference, or "slip," between actual and synchronous speed varies from about 0.5 to 5.0% for standard Design B torque curve induction motors. The induction machine's essential character is that it is created solely by induction instead of being separately excited as in synchronous or DC machines or being self-magnetized as in permanent magnet motors.For rotor currents to be induced the speed of the physical rotor must be lower than that of the stator's rotating magnetic field (***ns***); otherwise the magnetic field would not be moving relative to the rotor conductors and no currents would be induced. As the speed of the rotor drops below synchronous speed, the rotation rate of the magnetic field in the rotor increases, inducing more current in the windings and creating more torque. The ratio between the rotation rate of the magnetic field induced in the rotor and the rotation rate of the stator's rotating field is called slip. Under load, the speed drops and the slip increases enough to create sufficient torque to turn the load. For this reason, induction motors are sometimes referred to as asynchronous motors. An induction motor can be used as an induction generator, or it can be unrolled to form a linear induction motor which can directly generate linear motion.

Synchronous Speed:

The rotational speed of the rotating magnetic field is called as synchronous speed.

$$Ns = \frac{120 \times f}{P} \quad (RPM) \qquad (1)$$

Where, f = frequency of the supply

P = number of poles

Slip: Rotor tries to catch up the synchronous speed of the stator field, and hence it rotates. But in practice, rotor never succeeds in catching up. If rotor catches up the stator speed, there won't be any relative speed between the stator flux and the rotor, hence no induced rotor current and no torque production to maintain the rotation. However, this won't stop the motor, the rotor will slow down due to lost of torque, and the torque will again be exerted due to relative

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speed. That is why the rotor rotates at speed which is always less the synchronous speed.

The difference between the synchronous speed (Ns) and actual speed (N) of the rotor is called as slip.

$$\% \text{ slip } s = \frac{Ns - N}{Ns} \times 100 \quad (2)$$

IV. MATLAB/SIMULINK RESULTS

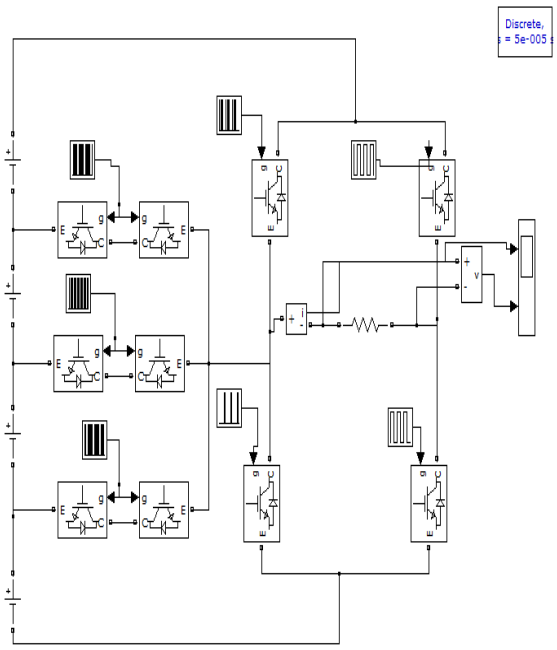

Fig.9. Simulink model of 9 level T-Type MLI

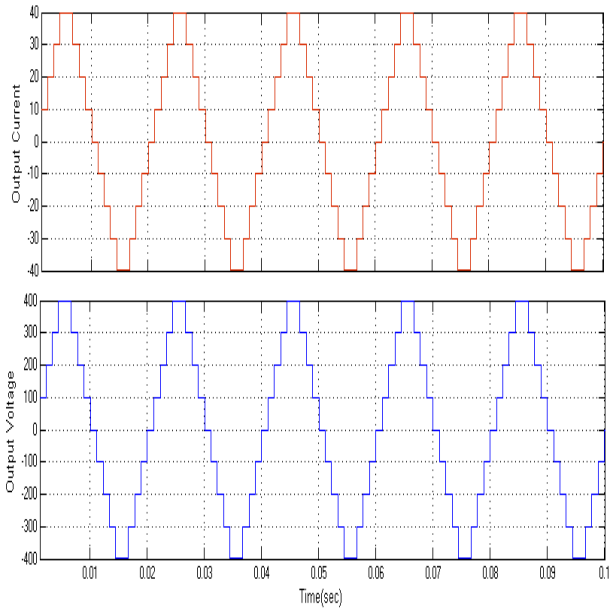

Fig.10. Output Current and Voltages of 9 Level T-Type MLI

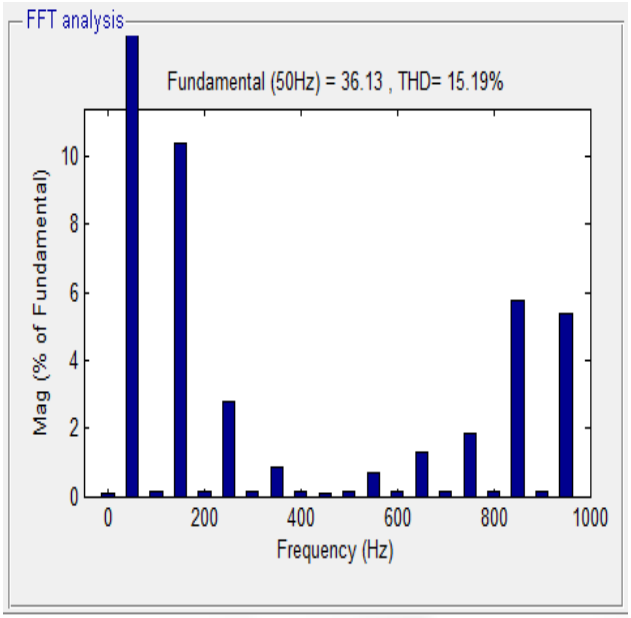

Fig.11. THD of 9 Level T-Type MLI

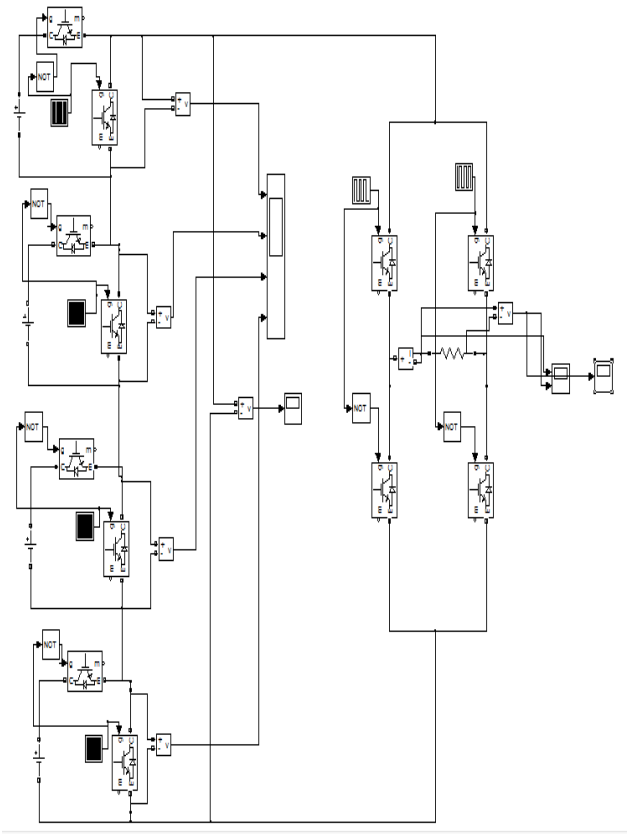

Fig.12. Simulink model of 31 level MLI.

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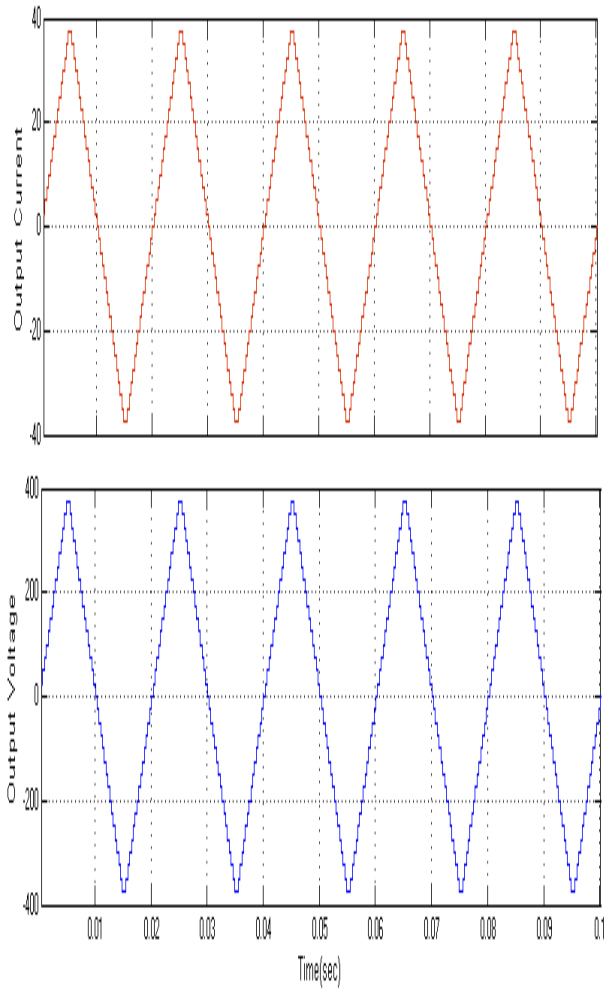

Fig.13. output voltage and currents of 31 Level MLI

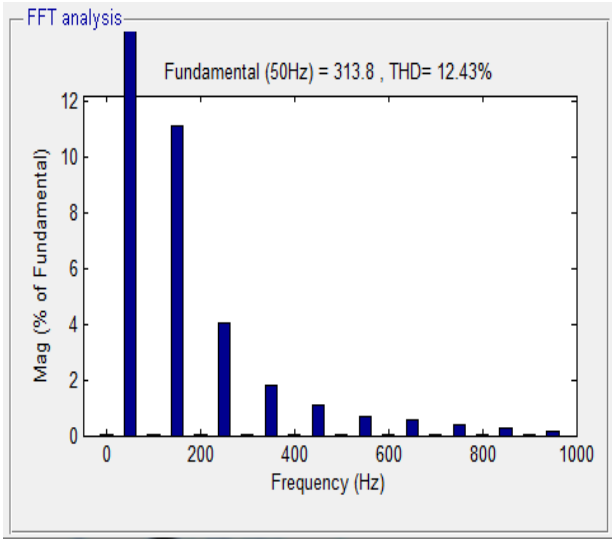

Fig.14. THD of 31 Level MLI

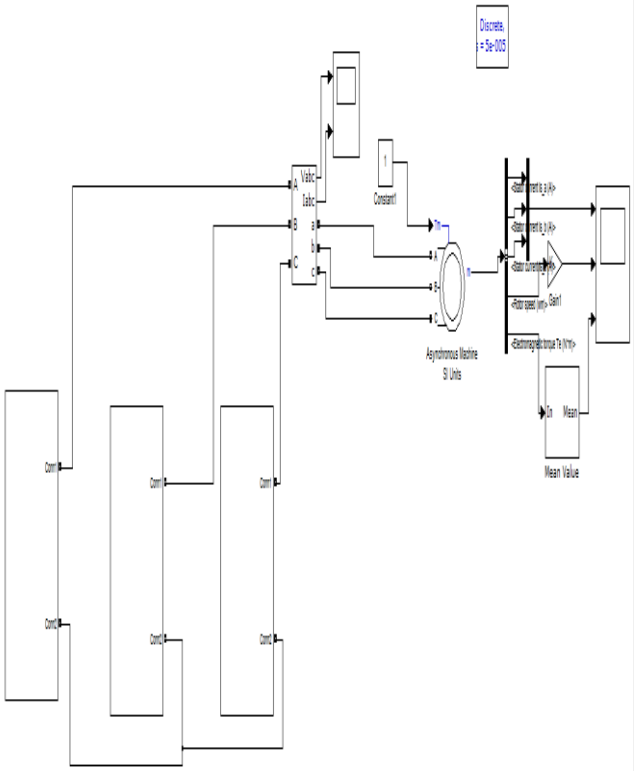

Fig.15. Simulink model of 31 level inverter fed Induction Motor.

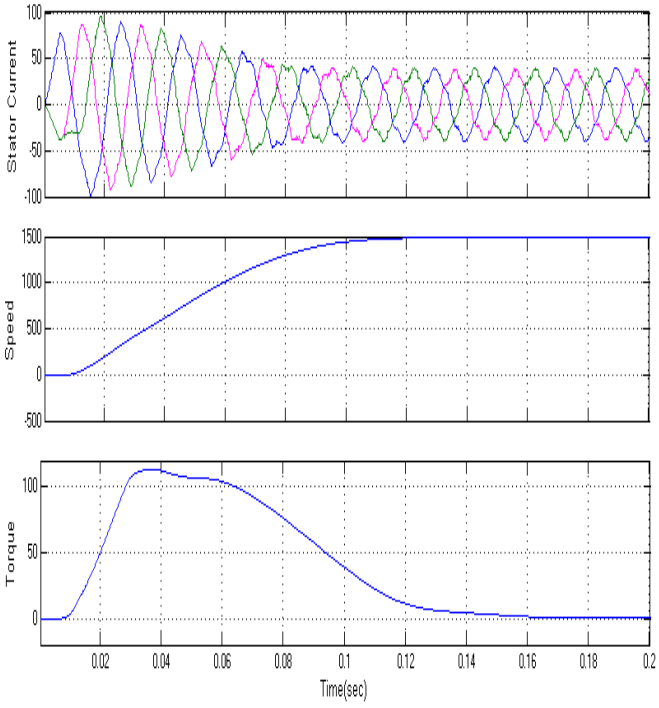

Fig.16. waveforms of Stator current, Speed & Torque

V. CONCLUSION

In conclusion it is strongly confirmed that the proposed topologies required less numbers of switch count to get more levels. The T-Type Multilevel inverter proposed is an symmetrical type converter which gives 9 level output voltage waveform with 10 switches and Cascaded Half bridge MLDCL inverter proposed is an asymmetrical type converter which gives 31 level output waveform with 12 switches, The proposed inverter has the advantage of reducing the number of power switches and gate drive circuits compared with conventional multilevel inverter. Therefore, the developed proposed topologies has better performance and needs minimum number of power electronic devices that lead to reduction in the installation space and cost of the inverter. Thus single phase voltage is converted to three phase and connected to induction motor drive and the performance of entire system is analysed.

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