International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

ELSEVIER
SSRN

IJIEMR Transactions, online available on 4th Jan 2019. Link :

http://www.ijiemr.org/main/index.php?vol=Volume-08&issue=ISSUE-01

Title: **A FELL PARTICULAR STAGGERED INVERTER TOPOLOGY UTILIZING NOVEL ARRANGEMENT ESSENTIAL UNITS WITH A DIMINISHED NUMBER OF INTENSITY ELECTRONIC COMPONENTS**

Volume 08, Issue 01, Pages: 20–35.

Paper Authors

D.RAMESH, K.KALYANI
Nova College Of Engineering &Technology

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

A FELL PARTICULAR STAGGERED INVERTER TOPOLOGY UTILIZING NOVEL ARRANGEMENT ESSENTIAL UNITS WITH A DIMINISHED NUMBER OF INTENSITY ELECTRONIC COMPONENTS

[1] D.RAMESH, [2] K.KALYANI
[1] Assistant Professor Nova College Of Engineering &Technology
[2] Power Electronics (M.Tech), Nova College Of Engineering &Technology

ABSTRACT:
In this investigation, another sort of fell secluded staggered inverters (CMMLIs) is displayed which can create a significant number of yield voltage levels with a sensible number of parts. In like manner, every arrangement phase of the proposed CMMLI is included two same essential units that are associated with one another through two unidirectional power switches without pointing any of the full H-connect cells. Likewise, since the possibility for producing a higher number of yield voltage levels in CMMLIs depends on the extent of the dc voltage sources utilized in every arrangement unit, in whatever remains of this paper, four distinct calculations for deciding a suitable incentive for the dc sources' size are additionally exhibited. In the accompanying, an extensive topological examination between some CMMLI structures detailed in the writing and proposed structure alongside a few reenactment and exploratory outcomes will be additionally given to approve the lucrative advantages and feasibility of the proposed topology.

Catchphrases: Course staggered inverter, Assurance of dc voltage sources, Secluded staggered inverter topologies, Diminished number of parts.

1. INTRODUCTION

In the field of modern power electronic utilities, multilevel voltage source inverters MLVSIs) offer the promising potential for use in medium and high power applications because of their different notable highlights such as lo voltage weights on switches, low aggregate harmonic contortion (THD) of the yield waveforms, no requirement for vast yield channels or transformers, and ease n general there are three kinds of MLVSIs. These are the diode cinch MLVSIs flying capacitor MLVSIs and cascaded H-bridge MLVSIs. However, these customary sorts dependably experience the ill effects of requiring an extensive number of intensity electronic parts, disengaged dc voltage sources and charge adjusting control systems which can build the general working and upkeep costs. These days, keeping in mind the end goal to lighten the previously mentioned constraints, numerous

structures have been introduced in the writing. They have tended to the height of the yield voltage levels through the minimization of the general expenses by with respect to the essential idea of MLVSIs. Hence, a few new essential units were proposed which can fill in as a level maker sub-unit. These proposed fundamental units are associated with a full H-bridge unit for changing the voltage extremity of the yield waveform and after that these modules are cascaded with each other in arrangement frame to produce numerous yield voltage levels moreover, cascaded association of arrangement essential units offers the modularity property which can fortify the dependability and adaptability of framework. Since cascaded modular multilevel inverters (CMMLI) can commonly produce any coveted number of higher yield voltage levels, the estimation of the dc voltage sources which can be given from a few sustainable power source assets (REs) can be chosen to be either symmetric or uneven. In the symmetric structures, the sizes of the dc voltage sources are same. Therefore, the assortment of segregated dc voltage sources is low which makes them more reasonable for savvy control electronic applications. Then again, these dc voltage esteems can be chosen to be distinctive in the lopsided setups. For this situation, although the assortment of disengaged dc voltage sources is high, the quantity of produced yield voltage levels is significantly more than the symmetric structures which endeavors to achieve a superior power quality through a lower estimation of the THD and a lessened number of intensity electronic components. Nevertheless, utilizing an extra full H-bridge unit in the new created MLVSIs as a rule prompts an expansion in the quantity of intensity switches and in the most extreme number of current path segments which can enhance the aggregate conduction misfortune and corrupt the general proficiency thereby. The point of this paper is to diminish the general segment tally of CMMLIs through introducing a novel topology which does not require an ordinary full H-bridge cell for changing the yield voltage extremity and can enhance the adaptability of the framework by the commitment of the capacitive divider technique connected on the dc-joins.

Therefore, whatever is left of this examination is sorted out as takes after. At initial, another fundamental modular MLVSI topology is displayed which is contained six unidirectional and two bi-directional power switches, two disengaged dc voltage sources and four capacitors as the dc interface vitality sharing components in the power circuit. For this situation, the four used capacitors are charged and discharged as often as possible amid the positive and negative half cycles of the yield waveform by control supply self-voltage adjusting. Meanwhile, the recommended topology does not contain any full H-bridge cells.

2. RESEARCH WORK

2.1 Diode-Clamped Multilevel Inverter

The nonpartisan point converter proposed by Nabae, Takahashi, and Akagi in 1981 was basically a three-level diode-clasped inverter In the 1990s a few researchers published

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

articles that have announced trial results for four-, five-, and six-level diode-clipped converters for such uses as static var pay, variable speed engine drives, and high-voltage framework interconnections. A three-phase six-level diode-clasped inverter is shown in Figure 3.1 Each of the three phases of the inverter shares a typical dc transport, which has been subdivided by five capacitors into six levels. The voltage over each capacitor is Vdc, and the voltage worry over each switching gadget is restricted to Vdc through the clasping diodes. The Table records the yield voltage levels workable for one phase of the inverter with the negative dc rail voltage V0 as a source of perspective. State condition 1 implies the switch is on, and 0 implies the switch is off. Each phase has five corresponding switch matches such that turning on one of the switches of the combine necessitates that the other integral switch be killed. The correlative switch sets for phase leg an are (Sa1, Sa1), (Sa2, Sa2), (Sa3, Sa3), (Sa4, Sa4), and (Sa5, Sa5). The Table additionally shows that in a diode-braced inverter, the switches that are on for a specific phase leg are constantly neighboring and in arrangement. For a six-level inverter, an arrangement of five switches is on at any given time.

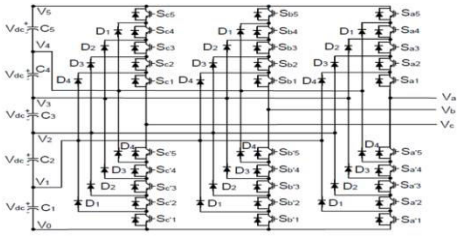


Fig 3.1 Three-phase six-level structure of a diode-clamped inverter.

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5Vdc$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4Vdc$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	0	1	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

Table 3.1 Diode-clamped six-level inverter voltage levels and corresponding switch states

Points of interest:

- All of the phases share a typical dc transport, which limits the capacitance prerequisites of theconverter. Thus, a consecutive topology isnt just conceivable yet additionally functional for utilizations such as a high-voltage consecutive between association or a customizable speed drive.
- The capacitors can be pre-charged as a gathering.
- Efficiency is high for basic recurrence switching.

Disservices:

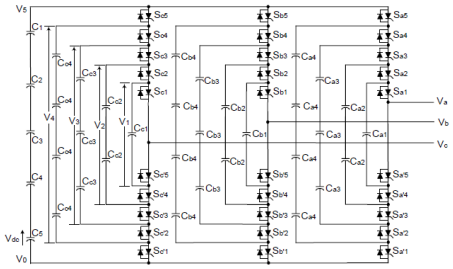


Fig 3.2 Three-phase six-level structure of a flying capacitor inverter.

One preferred standpoint of the flying-capacitor-based inverter is that it has redundancies for inward voltage levels; in other words, at least two substantial switch mixes can synthesize a yield voltage. The Table shows a rundown of the considerable number of mixes of phase voltage levels that

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

are workable for the six-level circuit shown in Figure 3.2. Not at all like the diode-braced inverter, the flying-capacitor inverter does not require the greater part of the switches that are on (directing) be in a sequential arrangement. Additionally, the flying-capacitor inverter has phase redundancies, whereas the diode-clipped inverter has just line-line redundancies. These redundancies permit a choice of charging/discharging particular capacitors and can be consolidated in the control framework for adjusting the voltages over the different levels.

Notwithstanding the (m-1) dc interface capacitors, the m-level flying-capacitor multilevel inverter will require (m-1) × (m-2)/2 helper capacitors for each phase if the voltage rating of the capacitors is indistinguishable to that of the principle switches. One application proposed in the writing for the multilevel flying capacitor is static var age The fundamental points of interest and disservices of multilevel flying capacitor converters are as per the following.

Points of interest:

- Phase redundancies are accessible for adjusting the voltage levels of the capacitors.
- Real and responsive power stream can be controlled.
- The expansive number of capacitors empowers the inverter to ride through short span blackouts and profound voltage lists.

Weaknesses:

- Control is muddled to track the voltage levels for the greater part of the capacitors. Likewise, precharging the greater part of the capacitors to a similar voltage level and startup are unpredictable.
- Switching usage and proficiency are poor for genuine power transmission.

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_{a0} = 5V_{dc}$ (no redundancies)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_{a0} = 4V_{dc}$ (4 redundancies)										
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
$V_{a0} = 3V_{dc}$ (5 redundancies)										
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
$V_{a0} = 2V_{dc}$ (6 redundancies)										
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 3V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_{a0} = V_{dc}$ (4 redundancies)										
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$V_{a0} = 0$ (no redundancies)										
0	0	0	0	0	0	1	1	1	1	1

Table 3.2Flying-capacitor six-level inverter redundant voltage levels and corresponding switch states

2.2 Other Multilevel Inverter Structures

Other than the three fundamental multilevel inverter topologies already examined, other multilevel converter topologies have been proposed; however, the vast majority of these are hybrid circuits that are blends of two of the essential multilevel topologies or slight varieties to them. Furthermore, the mix of multilevel power converters can be intended to match with a particular application in light of the essential topologies. In light of a legitimate concern for culmination, a portion of these will be recognized and quickly depicted.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

2.2.1 Mixed-Level Hybrid Multilevel Converter

To lessen the quantity of isolated DC hotspots for high-voltage, high-control applications with multilevel converters, diode-braced or capacitor-clasped converters could be utilized to supplant the full-bridge cell in a cascaded converter. The nine-level course converter consolidates a three-level diode-cinched converter as the cell. The first cascaded H-bridge multilevel converter requires four separate DC hotspots for one phase leg and twelve for a three-phase converter. On the off chance that a five-level converter replaces the full-bridge cell, the voltage level is viably multiplied for each cell. Thus, to achieve a similar nine voltage levels for each phase, just two separate DC sources are required for one phase leg and six for a three-phase converter. The arrangement has blended level hybrid multilevel units since it inserts multilevel cells as the building square of the course converter. The benefit of the topology is it needs less separate DC sources.

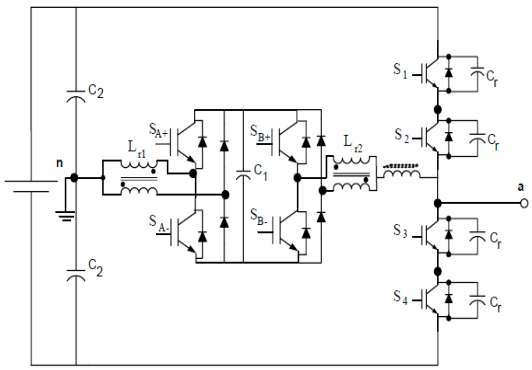


Fig 3.4 Zero-voltage switching capacitor-clamped inverter circuit.

2.2.2 Soft-Switched Multilevel Converter

Some delicate switching methods can be executed for various multilevel converters to diminish the switching misfortune and to expand proficiency. For the cascaded converter, in light of the fact that each converter cell is a bi-level circuit, the execution of delicate switching isnt at all not the same as that of customary bi-level converters. For capacitor-cinched or diode-braced converters, delicate switching circuits have been proposed with various circuit mixes. One of delicate switching circuits is a zero-voltage-switching compose which incorporates assistant resounding commutated post (ARCP), coupled inductor with zero-voltage progress (ZVT), and their blends as shown in Figure 3.4.

2.2.3 Back-to-Back Diode-Clamped Converter

Two multilevel a consecutive plan and afterward the all inclusive power conditioner when utilized on electrical dispersion frameworks and as an all inclusive power stream controller when connected at the transmission level. Beforehand, Lai and Peng proposed the consecutive diode-braced topology for use as a high-voltage dc bury association between two asynchronous air conditioning frameworks or as a rectifier/inverter for a customizable speed drive for high-voltage engines. The diode-cinched inverter has been chosen over the other two fundamental multilevel circuit topologies for use in a widespread power conditioner for the accompanying reasons:

- All six phases (three on each inverter) can share a typical dc interface. On

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

the other hand, the course inverter necessitates that each dc level be discrete, and this isnt helpful for a consecutive plan.

• The multilevel flying-capacitor converter likewise shares a typical dc interface; however, each phase leg requires a few extra assistant capacitors. These additional capacitors would add generously to the cost and the extent of the conditioner.

Since a diode-cinched converter going about as a widespread power conditioner will be required to make up for harmonics as well as work in low sufficiency modulation list locales, a more sophisticated, higher-recurrence switch control than the crucial recurrence switching method will be required. Thus, multilevel space vector and bearer based PWM approaches are thought about in the following area, and additionally novel transporter based PWM methodologies.

2.3 Multilevel Converter PWM Modulation Strategies

Pulse width modulation (PWM) procedures utilized in a regular inverter can be changed to use in multilevel converters. The approach of the multilevel converter PWM modulation methodologies can be ordered by switching recurrence The three multilevel PWM methods most talked about in the writing have been multilevel bearer based PWM, specific harmonic end, and multilevel space vector PWM; all are expansions of conventional two-level PWM techniques to a few levels. Other multilevel PWM methods have been utilized to a much lesser degree by researchers; therefore, just the three noteworthy techniques will be examined in this chapter.

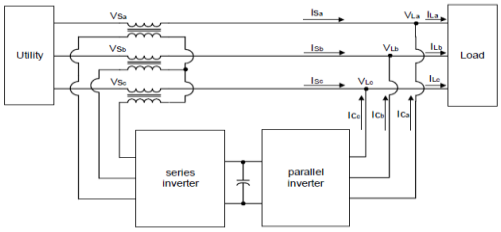


Fig 3.5 Series-parallel connection to electrical system of two back-to-back inverters.

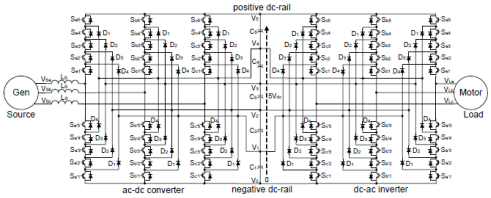


Fig 3.6 Six-level diode-clamped back-to-back converter structure.

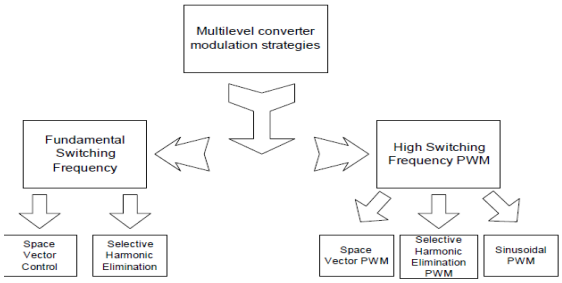


Fig 3.7Classification of PWM multilevel converter modulation strategies

In a multilevel inverter, deciding the quantity of levels will be a standout amongst the most imperative components since this influences a significant number of the other measuring variables and control techniques. Tradeoffs in indicating the quantity of levels that the power conditioner will require and the favorable circumstances and many-sided quality of having different voltage levels accessible are the essential contrasts that set

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

a multilevel channel apart from a solitary level channel.

The parallel inverter must have the capacity to infuse streams by forcing a voltage over the parallel inductors, LPI, that is the contrast between the heap voltage VL and parallel inverter yield voltage VPI. The most troublesome time to force a voltage over the inductors is when the heap voltage waveform is at its greatest or least. Recreation results have shown that the abundancy of the coveted load voltage Vnom should not be in excess of 70 percent of the general dc connect voltage for the parallel inverter to have adequate edge to infuse fitting remuneration streams. Without this edge, finish remuneration of receptive streams may not be conceivable. This edge can be consolidated into an outline factor for the inverter. Since the dc interface voltage and the voltage at the association point can both differ, the plan calculate utilized the rating choice process joins these components and additionally the little voltage drops that happen in the inverters amid dynamic gadget conduction.

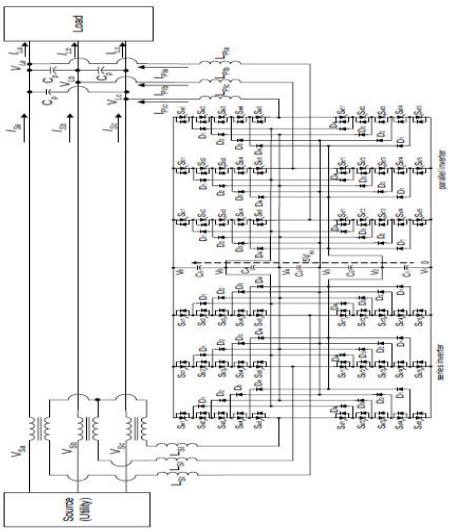


Fig 3.8Electrical system connection of multilevel diode-clamped power conditioner.

Expanding the quantity of levels does not influence the aggregate voltage blocking ability of the dynamic gadgets in each phase leg since bring down gadget evaluations can be utilized. A portion of the advantages of utilizing more than the base required number of levels in a diode clasped inverter are as per the following:

1. Voltage worry over each gadget is lower. Both dynamic gadgets and dc interface capacitors could be utilized that have bring down voltage evaluations (which at times are much cheaper and have more prominent accessibility).
2. The inverter will have a lower EMI in light of the fact that the dV/dt amid each switching will be lower.
3. The yield of the waveform will have more advances, or degrees of opportunity, which empowers the yield waveform to all the more intently track a reference waveform.

4. Lower singular gadget switching recurrence will achieve indistinguishable outcomes from an inverter with a less number of levels and higher gadget switching recurrence. Or then again the switching recurrence can be kept the same as that in an inverter with a less number of levels to achieve a superior waveform.

The downsides of utilizing more than the required least number of levels are as per the following:

1. Six dynamic gadget control signals (one for each phase of the parallel inverter and the arrangement inverter) are required for each hardware level of the inverter i.e.6·(m-1) control signals. Extra levels require more computational assets and add many-sided quality to the control.

2. In the event that the blocking diodes utilized in the inverter have indistinguishable rating from the dynamic gadgets, their number increments significantly on the grounds that 6·(m-2)·(m-1) diodes would be required for the consecutive structure.

Considering the exchange offs between the quantity of levels and the voltage rating of the gadgets will by and large lead the creator to choose a proper incentive for each.

Blame finding in multilevel converters

Since a multilevel converter is ordinarily utilized in medium to high power applications, the dependability of the multilevel converter framework is vital. For example modern drive applications in assembling plants are needy upon enlistment engines and their inverter frameworks for process control. By and large, the ordinary insurance frameworks are inactive gadgets such as wires, over-burden transfers, and circuit breakers to secure the inverter frameworks and the enlistment engines. The insurance gadgets will separate the power sources from the multilevel inverter framework whenever a blame happens, ceasing the worked procedure. Downtime of assembling gear can indicate be thousands or hundreds of thousands of dollars for each hour, therefore blame recognition and determination is crucial to an organizations main concern. Keeping in mind the end goal to keep up constant task for a multilevel inverter framework, information of blame behaviors, blame expectation, and blame determination are fundamental. Deficiencies should be identified as quickly as time permits after they happen, on the grounds that if an engine drive runs constantly under unusual conditions, the drive or engine may rapidly come up short.

The conceivable structure for a blame determination framework is delineated in Figure 3.8. The framework is made out of four noteworthy states: include extraction, neural system grouping, blame determination, and switching design figuring with entryway flag yield. The element extraction plays out the voltage input flag change, with evaluated flag esteems as vital highlights, and the yield of the changed flag is exchanged to the neural system order. The systems are prepared with both typical and strange information for the MLID; thus, the yield of this system is almost 0 and 1 as twofold code. The twofold code is sent to the blame finding to interpret the blame kind

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

and its area. Then, the switching design is figured to reconfigure the multilevel inverter.

Switching designs and the modulation record of other dynamic switches can be changed in accordance with keep up voltage and current in an adjusted condition after reconfiguration recoups from a blame. The MLID can consistently work in an adjusted condition; obviously, the MLID wont have the capacity to work at its appraised control. Therefore, the MLID can work in adjusted condition at lessened power after the blame happens until the point that the administrator finds and replaces the harmed switch

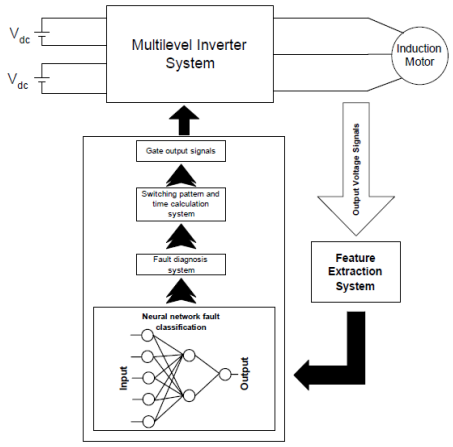


Fig 3.8 Structure of fault diagnosis system of a multilevel cascaded H-bridges inverter.

2.4 Applications

DC control source use

Inverter intended to the unit shown gives up to 1.2 amperes of rotating current, or enough to control two sixty watt light knobs.

HVDC control transmission

With HVDC control transmission, AC control is amended and high voltage DC control is transmitted to another area. At the getting area, an inverter in a static inverter plant changes over the power back to AC.

Variable-recurrence drives

A variable-recurrence drive controls the working rate of an AC engine by controlling the recurrence and voltage of the power provided to the engine. An inverter gives the controlled power. By and large, the variable-recurrence drive incorporates a rectifier with the goal that DC control for the inverter can be given from principle AC control. Since an inverter is the key segment, variable-recurrence drives are at times called inverter drives or just inverters.

Electric vehicle drives

Movable speed engine control inverters are as of now used to control the footing engines in some electric and diesel-electric rail vehicles and additionally some battery electric vehicles and hybrid electric highway vehicles such as the Toyota Prius. Different changes in inverter technology are being created particularly for electric vehicle applications. In vehicles with regenerative braking, the inverter likewise takes control from the engine (now going about as a generator) and stores it in the batteries.

3. IMPLEMENTATION

PROPOSED MLVSI TOPOLOGY

The fundamental part of the proposed modular MLVSI topology named as the proposed essential unit is shown in Fig. 1.1. As can be seen, the proposed fundamental unit comprises of one dc voltage source, two capacitors as dc interface vitality sharing components, and one bi-directional and two unidirectional power switches which should be activated by integral tasks to maintain a

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

strategic distance from short circuit issues. For this situation, the bi-directional power switch can be substituted by one common power switch and four power diodes to attempt the conduction of the invert current in both ways.

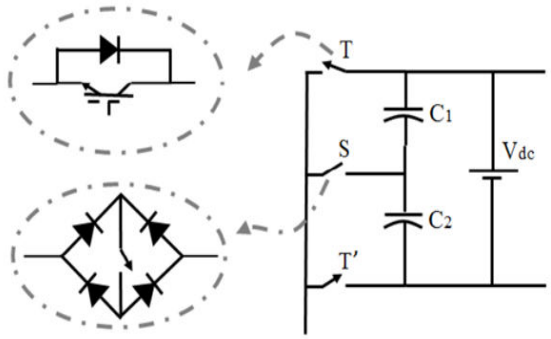


Fig. 4.1 Proposed basic unit.

Keeping in mind the end goal to exhibit the working methods of the proposed fundamental unit, the present stream path of four passible yield voltage states are delineated in Fig. 4.2(a)- (d).

As per Fig.4. 2(a) and (b), when either the switch of T or T □ is killed ON and S turns into, the voltage of the dc source (Vdc or -Vdc) is exchanged to the yield. At this stage, none of the dc connect capacitors go into the present path and subsequently both of them are straightforwardly charged by control supply.

Also, as indicated by Fig. 4.2(c) and (d), when S moves toward becoming ON and switches T or T end up OFF, the crosswise over voltage of C1 or C2 is pumped to the yield. Here, when the crosswise over voltage of one gathered capacitor (C1 or C2) is being pumped to the yield, another capacitor is specifically charged by the power supply.

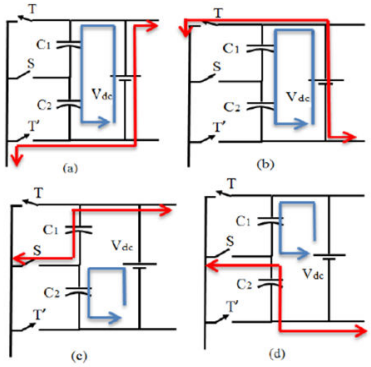


Fig.4 2. Different current flow path of operating modes for proposed basic unit when (a) $V_{d\ c}$(b) V_{dc}(c) across voltage of C_1 (d) across voltage of $C_2$is transferred to the output.

The proposed MLVSI topology shown in Fig. 3(a) is made by the commitment of the presented fundamental unit. Here, to make an ideal structure of a MLVSI as far as having the most minimal number of switching gadgets with most prominent number of produced yield voltage levels, two same fundamental units with inverse polarities are utilized in the proposed generally speaking structure as opposed to utilizing a full H-bridge unit in the front of the proposed essential unit. Table I shows the seventeen diverse ON switching conditions of the proposed topology in which C and D remain for the charging and discharging methods of the capacitors, individually.

Also, C1,L V , C 2,L V , C1,R V and C 2,R V are the crosswise over voltages of the capacitors C1,L , C2,L , C1,R and C2,R , individually.

Meanwhile, V dc,L and V dc,R indicate the required dc voltage sources situated at the left and right half of the circuit, individually.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

For this situation, to dodge short circuit issues, the combined switches (T) , (TR) and (TL) should not be turned ON, all the while.

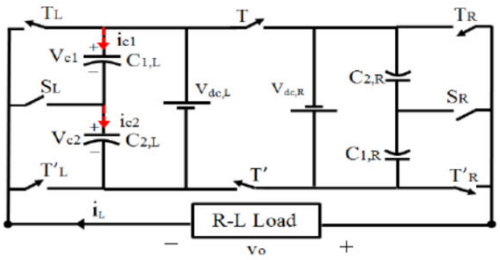


Fig4.3 Proposed MLVSI topology

Fig. 4.3(b) shows typical output voltage and currentwaveforms of the proposed topology based on a 50Hzswitching frequency. In this case, two utilized dc voltagesources are assumed to be non-equal and a resistive-inductiveload has been connected at the output of the proposedtopology.

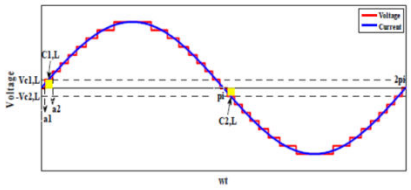


Fig4.3(b) Typical output voltage and current waveforms of proposed topology.

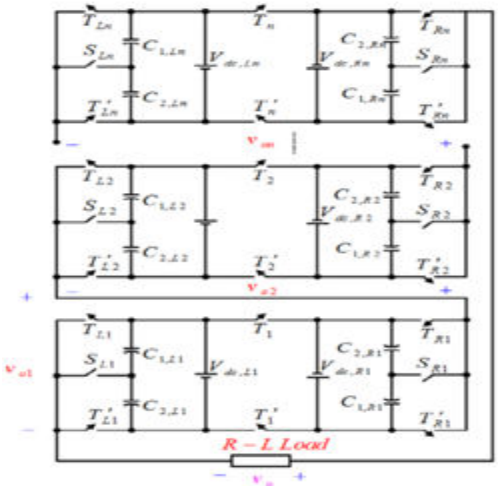


Fig. 4.4 Proposed CMMLI topology.

4.1 PROPOSED ALGORITHMS TO DETERMINE THE MAGNITUDE OF DC VOLTAGE SOURCES

In this section, to determine a suitable magnitude for the dcvoltage sources of the proposed CMMLI topology, fourdifferent passible algorithms are presented. In addition, thenumber of generated output voltage levels, the maximumvalue of the output voltage, the variety of the isolated dcvoltage sources and the total value of the blocked voltage arecalculated for each of them.

4.1.1 First Proposed Algorithm

In the first algorithm, the magnitude for all of the dc voltage sources is assumed to be the same (symmetric algorithm) and equal to:

$$v_{dc,Li} = v_{dc,Ri} = 2v_{dc} for (i=1,2,.....,n)$$

It is clear that the variety of isolated dc voltage sources basedon the proposed symmetric algorithm is one. Therefore, thenumber of output voltage levels and the maximum value ofthe output voltage are expressed as (13) and (14),respectively.

$$N_{level} = 8n+1$$

$$V_{o,max} = 4nv_{dc}$$

Another critical parameter which usually influences theoverall cost function of an inverter is the total value of themaximum blocked voltage across the switches in their OFFstate condition. Therefore, this value is calculated by thefollowing equations for all of the involved switches in theproposed CMMLI based on the first proposed method.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

$$V_{Block\,T_i'} = V_{Block\,T_i} = 4V_{dc}$$
$$V_{Block\,T_{Li}'} = V_{Block\,T_{Li}} = V_{Block\,T_{Ri}'} = V_{Block\,T_{Ri}}$$
$$V_{Block,S_{Li}} = V_{Block,S_{Ri}} = \pm V_{dc}$$
$$V_{Block} = 2\sum_{i=1}^{n}(V_{Block\,T_i} + V_{Block\,T_{Li}} + V_{Block,S_{Li}})$$

A. *Second Proposed Algorithm*

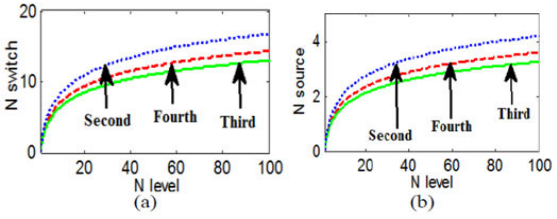
The second proposed algorithm is dedicated to the binary pattern for the magnitude of the dc voltage sources in each series unit, which can be written according to

$$V_{dc,Ri} = 2V_{dc,Li} = 2\times 13^{n-1}V_{dc} \quad for(i = 1,2,.$$

Hence, the number of output voltage levels, the maximumvalue of the output voltage, the maximum value of theblocked voltage and the variety of the isolated dc voltagesources are calculated by the following equations:

$$N_{level} = 13^n$$
$$V_{o,\max} = \frac{(13^n - 1)}{2}V_{dc}$$
$$V_{Block} = 9\times(\frac{13^n - 1}{4})V_{dc}$$
$$N_{Variaty} = 2n$$

At this stste in order to evaluate the three supposed asymmetric algorithms for the proposed CMMLI topology, variations of the number of required power switches, the number of required dc voltage sources and the variety of isolated dc voltage sources versus different numbers of output voltage levels have been shown on the basis of Fig 4.4



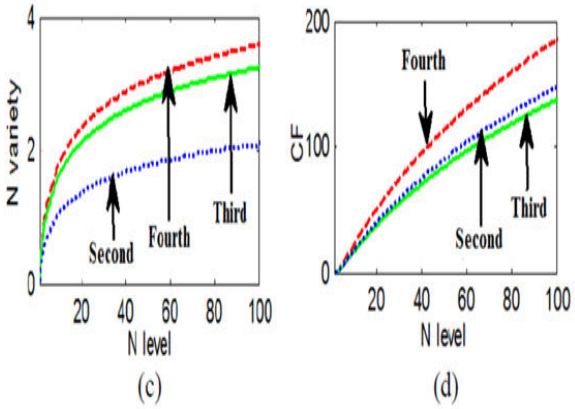


Fig 4.4 Comparisons between three supposed asymmetric algorithms (a) variations of N_{Switch} versus N_{level}(b) variations of N_{Source}versus N_{level}(c) variations of $N_{Variaty}$versus N_{level}(d) variations of CF versus N_{level}.

Then its respective variations are shown by Fig. 4(d). Here,the per unit value of the total blocked voltage (V_{Block}^{pu}) canbe denoted by (35).

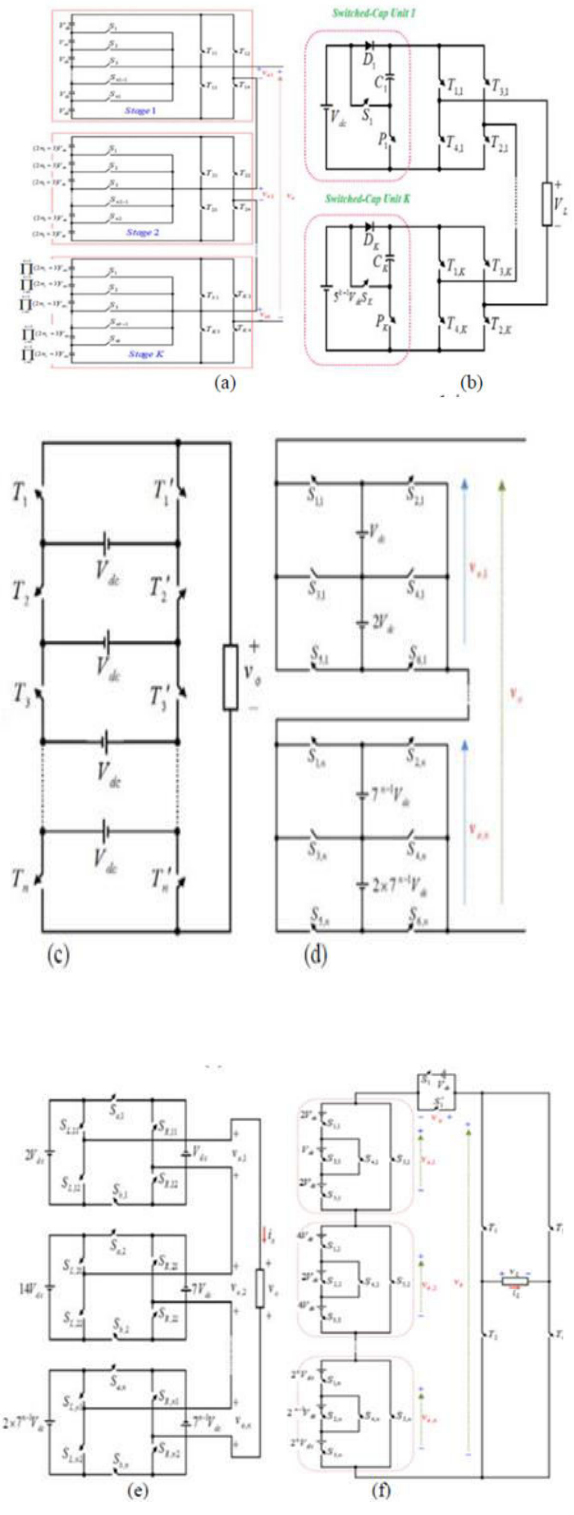
$$CF = (N_{Switch})\times(N_{Source})\times(N_{Variaty})\times(V_{Block}^{pu})$$
$$V_{Block}^{pu} = \frac{V_{Block}}{V_{o,\max}}$$

It should be noted that, the values of the blocked voltages foreach of the proposed algorithms, in terms of number ofoutput voltage levels, are always equal to each other and canbe written as:

$$V_{Block} = \frac{9\times(N_{level} - 1)}{4}$$

By taking these figures into account, it is clear that thethird proposed algorithm offers the better condition incontrast to others and since it can minimize the cost, thisalgorithm would be selected as the main proposedasymmetric structure for the comparison done in the nextsection.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org



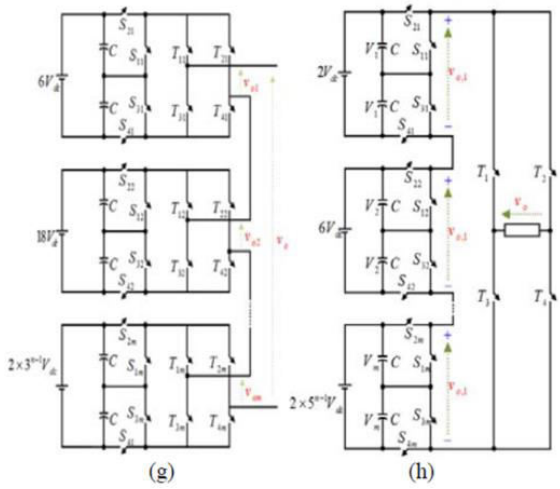


Fig. 4.5 Suggested CMMLI topologies & its operation(a)(b)(c)(d)(e)(f)(g)(h)

4. RESULTS

In this section, obtained simulation and experiment resultsbased on the proposed MLVSI topology shown in Fig. 3(a)and the proposed CMMLI depicted in Fig. 4 are presented. Inthe computer simulation process, PSCAD/EMTDC softwareis used and all of the semiconductor devices are assumed tobe ideal.

In all processes of simulation and experimental tests, aresistive-inductive load with values of

$R = 25\Omega$ and

$L = 250mH$ is considered.

The experimental setup of theproposed topology is shown in Fig 8. The power MOSFETsused in the prototype are SPW47N60C3s (with antiparalleldiode) that can tolerate 650V as the maximum value of thepeak inverse or blocked voltage value. Meanwhile, a 89C52microcontroller made by ATMEL Company has been utilizedin the experimental tests to generate the respective gateswitching pulses at the fundamental switching frequency

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

withrespect to the table In addition, among the four proposed algorithms to meet the precise magnitudeof dc voltage sources, the thirdasymmetric pattern which could attain the best cost-effectivecapability of generating the largest number of output voltagelevels with the minimum devices count, is considered in theperformance evaluation. Therefore, the values of two utilizeddc voltage sources are set on 100V and 300V based on thethird presented algorithm. In addition the capacitance of alldc link capacitors are assumed same and equal to 2200F .Below fig show the output 17-level voltage and nearlysinusoidal load current in the simulation and in experiment,respectively. As can be seen, the obtained results have goodagreement with each other. Here, the maximum amplitude ofthe load voltage and current are 400V and 5A, respectively.Furthermore, the balanced voltage waveforms of the dc linkcapacitors on the basis of experimental results are shown inFig. 10. As can be seen, the dc link voltages are quite smoothand have acceptable ripple values, which can attest to theprecise capacitive divider feature of the proposed topologyduring the loading condition. The peak inverse voltage (PIV)or blocked voltage waveforms across the switches T_L,T , T_RS and S $_L$ in the experimental process have also been illustrated in Fig. 11. In this case, the maximum value of blocked voltage is about 400V which can be tolerated by two interconnected switches.

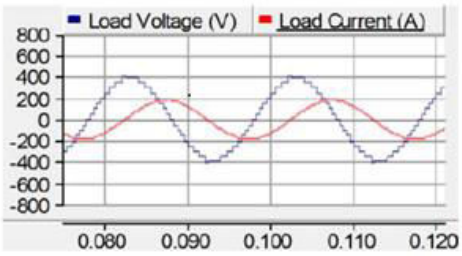


Fig. 6.1. Output voltage and current waveforms in simulation

Finally, in order to assert the capability of the proposedstructure in a higher number of output voltage levels and toauthenticate the performance of the other recommendedalgorithms for the dc voltage sources magnitude, theconnection of two series units of the proposed MLVSI based is considered at this stage, when an inductive loadhas been connected at the output. In this case, by utilizingonly 16 switching devices, two dc sources in each unit and the fourth presented pattern for the magnitude of the dcvoltage sources, an 81-level output voltage is made

the corresponding output voltages of thefirst unit, second unit and 81-level load voltage and currentwaveforms of this structure in the experiment, while a 3Ainductive load is connected at the output. Here, the magnitudeof the used dc-sources are set a

$V_{dc,L1} = V_{dc,R1} = 20V$ and

$V_{dc,l2} = V_{dc,R2} = 180\ V$

Therefore, both of the units of the proposed MLVSIs producefour positive levels, four negative levels and one zero level attheir output with amplitudes of $\pm 10V$,$\pm 20V$,$\pm 30V$,$\pm 40V$and $\pm 90V$,$\pm 180V$

,□270*V* ,□360*V* , for the first andsecond proposed series units, respectively.

5. CONCLUSION

In this projects to generate a higher number of output voltagelevels with reductions in the components count and in theother important power electronic parameters of the cascadedmodular multilevel inverters (CMMLIs), a new topology waspresented in which does not require any H-bridge cells ineach series unit to turn the output voltage polarity. Hence,each series unit of the proposed CMMLI is composed of twoisolated dc voltage sources, four capacitors and eight gatedrivers. In this case, all of the dc link capacitors are directlycharged by power supplies without utilizing any complicatedcontrol strategies. In addition, in order to achieve a differentnumber of output voltage levels, four different algorithms fordetermining the magnitude of the dc voltage sources weresuggested. A comprehensive comparison from differentaspects confirms the advantages of the proposed structure incomparison to several recently presented CMMLIs. Finally,the effectiveness and correct performance of proposed17-level and 81-level derived topologies have been verifiedby simulation and experimental results.

6. REFERENCES

[1] J. Rodriguez, L. J.Sheng, and P. Fang Zheng, Multilevelinverters: A survey of topologies, controls, and applications, *IEEE* Trans. Ind Electron., Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[2] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, A survey on cascaded multilevel inverters, IEEE Trans. Ind. Electron., Vol. 57, No. 7, pp. 2197-2206, Jul. 2010.

[3] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, A survey on natural point clamped inverters,*IEEE Trans. Ind. Electron*., Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.

[4] M. Ebadi, M. Joorabian, and J. S. Moghani, Multilevel cascade transformerless inverter for connecting distributed-generation sources to network,*IET Power Electron,* Vol. 7, No. 7, pp. 1691-1703, Dec. 2014.

[5] M. M. Renge and H. M. Suryawanshi, Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives,*IEEE Trans. Power Electron.,* Vol. 23, No. 4, pp. 1598-1607, Jul. 2008.

[6] M. Khazraei, H. Sepahvand, M. Ferdowsi, and K. A. Corzine, Hysteresis based control of a single-phase multilevel flying capacitor active rectifier,*IEEE Trans. Power Electron*., Vol. 28, No. 1, pp. 154-164, Jan. 2013.

[7] J. Huang and K. A. Corzine, Extended operation of flying capacitor multilevel inverters,*IEEE Trans. Power Electron.,* Vol. 21, No. 1, pp. 140-147, Jan. 2006.

[8] P. Roshankumar, R. S. Kaarthic, K. Gupakumar, J. I. Leon and L. G. Franquelo, A seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridge, *IEEE Trans. Power*

Electron., Vol. 30, No. 7, pp. 3471-3478. Jan. 2015

[9] M. FarhadiKangarlu and E. Babaei, A generalized cascaded multilevel inverter using series connection of sub multilevel inverters,*IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 625-636, Feb. 2013.

[10] A. Ajami, M. R. J. Oskuee, A. Mokhberdoran, and A. Van den Bossche, Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches,*IET Power Electron.,* Vol. 7, No. 2, pp. 459-466, Feb. 2014.

[11] Y. Hinago and H. Koizumi, A single-phase multilevel inverter using switched series/parallel dc voltage sources, *IEEE Trans. Ind. Electron.,* Vol. 57, No. 8, pp. 2643-2650, Aug. 2010.

[12] R. S. Alishah, D. Nazarpour, S. H. Hosseini and M. Sabahi, Reduction of power electronic elements in multilevel converters using a new cascade structure,*IEEE Trans. Ind. Electron.* Vol. 62, No. 1, pp. 256-269, Jan. 2015.

[13] M. F. Kangarlu, E. Babaei, M. Sabahi, and M. R. AlizadehPahlavani, Cascaded multilevel inverter using sub-multilevel cells,*J. Elect. Power Syst. Res,* Vol. 96, pp. 101-110, Mar. 2013.

[14] E. Babaei and S. S. Gowgani, Hybrid multilevel inverter using switched-capacitor units,*IEEE Trans. Ind. Electron*., Vol. 61, No. 9, pp 4614-4621, Sep. 2014.

[15] A. K. Sadigh,. V. Dargahi, M. Abarzadeh, and S. Dargahi,Reduced DC voltage source flying capacitor multicell multilevel inverter: analysis and implementation,*IET Power Electron*., Vol. 7, No. 2, pp. 439-450, Feb. 2014.

[16] R. Barzegarkhoo, H. M. Kojabadi, E. Zamiry, N. Vosoughi, and L.Chang Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple dc link producer with reduced number of switches,*IEEE Trans. Power Electron.,* Vol. 31, No. 8, pp 5604-5617, Aug. 2016.

[17] R. ShalchiAlishah, D. Nazarpour, S. H Hosseini, and M. Sabahi, New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels,*IET Power Electron*., Vol. 7, No. 1, pp. 96-104, Jan. 2014.

[18] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications,*IEEE Trans. Power Electron.*, Vol. 26, No. 11,pp. 3109-3118, Nov. 2011.