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IMPLEMENTATION OF SRAM CONTROLLER AND ITS CELL ARCHITECTURE FOR DATA PROCESSING APPLICATION

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ABSTRACT: Memory is most imperative sub-arrangement of advanced circuit which store information/data. The goal of this paper is to utilize Verilog Hardware Description Language& examine in FRONT AND BACK end to create Verilog code for appropriate activity of SRAM. This paper investigates the tradeoffs that are engaged with the plan of SRAM. The real segments of a SRAM, for example, the line decoders, the memory cells and the sense speakers have been considered in detail. The circuit methods used to decrease the power dissemination and deferral of these segments has been investigated and the tradeoffs have been clarified. The way to low power activity in the SRAM information way is to decrease the flag swings on the high capacitance hubs like the bit lines and the information lines. Timed voltage sense speakers are fundamental for acquiring low detecting power, and exact age of their sense clock is required for rapid task. The following circuits basically utilize an imitation memory cell and a copy bit line to track the postponement of the memory cell over an extensive variety of process and working conditions. We present exploratory outcomes from two distinct models. At last a 8Kb model SRAM has been planned and confirmed. This outline fuses a portion of the circuit strategies used to diminish control scattering and deferral. Trial information has been given which demonstrates the adequacy of utilizing the resetting plan for the line decoders. While planning the SRAM, strategies, for example, circuit dividing, entryway oxide thickness varieties and low power design systems are made utilization of to limit the power scattering. The combination and Simulation device ISE 14 is utilized to outline configuration in to focused gadget. Approval of the outcome and timing recreation are finished utilizing XST apparatus of XILINX 14.2.

1. INTRODUCTION TO SRAM CONTROLLER AND ITS FUNCTIONALITIES:

Static random-access memory (SRAM) continues to be a critical component across a wide range of microelectronics applications from consumer wireless to high-end workstation and microprocessor applications. For almost all fields of applications, semiconductor memory has been a key enabling technology. It is

forecasted that embedded memory in SOC designs will cover up to 90% of the total chip area. A representative example is the use of cache memory in microprocessors. The operational speed could be significantly improved by the application of on-chip cache memory.Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development toward more compact design rules and, consequently, toward higher storage densities. This project deals with design of low power static random-access memory cells and peripheral circuits for standalone RAMs, in 180nm focusing on stable operation and reduced leakage current and power dissipation in standby and active modes. The detailed view of the designed 8Kb SRAM memory block is as shown in Fig. 1, this total block is built up of two 4Kb memory cuts along with decoding sections and control logics for proper operation of the memory. In this project work, emphasis is laid on minimizing power consumption. The decoding logic is implemented as a tree (multi-stage path) to reduce power dissipation in active mode. To reduce the power in standby mode, adopting a multi-Vth technique reduces the leakage current [2].As the technology shrinks (in Sub-micron technologies), the power issue becomes very prominent due to high transistor density, increased leakage currents and increase in interconnect parasitics. In spite of the cropping up of power issues, the power consumption can be reduced by adopting suitable techniques, such as circuit partitioning, increasing gate oxide thickness in non-critical paths, reducing Vth (dual Vth) etc. According to Benton H. Calhoun, AnanthaChandrakasan [2] an 180nm SRAM can be designed that functions into the sub-threshold region and examines the impact of process variation for low-voltage operation is described. He also depicts the impact of number of transistors and their structure on the leakage power of the memory bit cell. The circuit partitioning technique also improves the speed of our memory. The control block, the decoders and IO blocks are all in low Vth, whereas the memory cells, the dummy column and dummy row along with the sense amplifier are in high Vth [1]. Having this kind of configuration has helped in gaining in speed and also reducing the dynamic and static power consumption by a considerable amount The concepts of variation of threshold voltages and increased gate-oxide thickness [4], for reduced leakage currents due to subthreshold conduction and gate tunnel current are included, which assure the design of low-voltage random-access memory (RAM) cells and peripheral circuits for standalone SRAMs, focusing on stable operation and reduced subthreshold current in standby and active modes A number of researchers have studied the low power design of SRAM memories; they concluded that by circuit partitioning, variable Vth techniques and reducing capacitance along word lines, the power consumed in SRAM memories can be minimized. This paper focuses to the algorithms used for testing memories in SoC and faults coverage through them. BIST based algorithms have a wonderful solution for this scenario. As per

comparison of various algorithms, on the basis of fault coverage and error free memory assurance, the BIST algorithms has chosen in this research. This paper implemented BIST algorithm for high speed and low area performance. The memory BIST controller architecture has designed and tested on Field Programmable Gate Array (FPGA) device.

A. Advantages and Uses of Low Power SRAM

1) 1.1.1 SRAMs are basically used as:

- Embedded memory, e.g.: First and second level caches in processors Data buffers in various DSP chips
- Standalone SRAMs: This can be integrated as an external memory during board design stage.
- Caches in computer systems Main memory in low power applications

2) 1.1.2 Advantages of SRAM memories:

- Faster Data Access speeds.
- Standby power of SRAM memories is very low inspite of high density of transistors.
- SRAM cells have high noise immunity due to larger noise margins, and have ability to operate at lower power supplies.

2. RESEARCH WORK

Semiconductor memory is an electronic data storage device, often used as computer memory, implemented on a semiconductor-based integrated circuit. It is made in many different types and technologies.Semiconductor memory has the property of random access, which means that it takes the same amount of time to access any memory location, so data can be efficiently accessed in any random order.[1] This contrasts with data storage media such as hard disks and CDs which read and write data consecutively and therefore the data can only be accessed in the same sequence it was written. Semiconductor memory also has much faster access times than other types of data storage; a byte of data can be written to or read from semiconductor memory within a few nanoseconds, while access time for rotating storage such as hard disks is in the range of milliseconds. For these reasons it is used for main computer memory (primary storage), to hold data the computer is currently working on, among other uses. Shift registers, processor registers, data buffers and other small digital registers that have no memory address decoding mechanism are not considered as memory although they also store digital data.

Non-volatile SRAM:

Non-volatile SRAMs, or nvSRAMs, have standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. nvSRAMs are used in a wide range of situations—networking, aerospace, and medical, among many others[3] —where the preservation of data is critical and where batteries are impractical.

Asynchronous SRAM:

Asynchronous SRAM are available from 4 Kb to 64 Mb. The fast access time of SRAM makes asynchronous SRAM appropriate as main memory for small cache-less embedded processors used in everything from industrial electronics and measurement systems to hard disks and networking

equipment, among many other applications. They are used in various applications like switches and routers, IP-Phones, IC-Testers, DSLAM Cards, to Automotive Electronics.

By transistor type

- Bipolar junction transistor (used in TTL and ECL) – very fast but consumes a lot of power
- MOSFET (used in CMOS) – low power and very common today

By function

- Asynchronous – independent of clock frequency; data in and data out are controlled by address transition
- Synchronous – all timings are initiated by the clock edge(s). Address, data in and other control signals are associated with the clock signals

By feature

- ZBT (ZBT stands for zero bus turnaround) – the turnaround is the number of clock cycles it takes to change access to the SRAM from write to read and vice versa. The turnaround for ZBT SRAMs or the latency between read and write cycle is z-ero.
- syncBurst (syncBurst SRAM or synchronous-burst SRAM) – features synchronous burst write access to the SRAM to increase write operation to the SRAM
- DDR SRAM – Synchronous, single read/write port, double data rate I/O
- Quad Data Rate SRAM – Synchronous, separate read and write ports, quadruple data rate I/O

3. IMPLEMENTATION

With the rapid growth of digital circuits in recent years, the need for high-speed data transmission has been increased. The VLSI industry faces the problem of providing the technology that can be able to support a high data capacity and to with low power. [2] Many memories are available but SRAM has gained much attention for different reasons. SRAM has been recognized as an outstanding memory for high-speed data access. Standby power of SRAM memories is very low in spite of high density of transistors. SRAM cells have high noise immunity due to larger noise margins, and have ability to operate at lower power. [5] This work deals with the design and analysis of 8Mb Static Random Access Memory (SRAM), focusing on optimizing power and delay to achieve high throughput for RF applications. The SRAM access path is split into two portions: from address input to word line rise (the row decoder) and from word line rise to data output (the read data path). Techniques to optimize both of these paths are investigated and implemented. In this work the existing SRAM architectures are analyzed and innovative SRAM structure with a throughput of up to 12.6 Gbit/s at a clock frequency of 168 MHz is tried to achieve. The proposed SRAM with data, address and control lines is planned to design and code in VeriLog, simulate and synthesize using Xilinx ISE 9.1i and finally implement using FPGA Spartan II Pro kit. The characterization is done on single bit SRAM cell to determine the cell characteristics in static mode. The simulated results obtained after performing the

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characterization of a single bit SRAM cell is tested using FPGA Spartan II pro kit.

3.1 ARCHITECTURES OF SRAM

A. Synchronous Sram and Its Working

As computer system clocks increased, the demand for very fast SRAMs necessitated variations on the standard asynchronous fast SRAM. The result was the synchronous SRAM (SSRAM).Synchronous SRAMs have their read or write cycles synchronized with the microprocessor clock and therefore can be used in very high-speed applications. An important application for synchronous SRAMs is cache SRAM used in Pentium- or Power-based PCs and workstations. SSRAMs typically have a 32 bit output configuration while standard SRAMs have typically a 8 bit output configuration. Figure 1 shows a typical functional block diagram.The memory is managed by three control signals. One signal is the chip select (CS) or chip enable (CE) that selects or de-selects the chip. When the chip is de-selected, the part is in stand-by mode (minimum current consumption) and the outputs are in a high impedance state. Another signal is the output enable (OE) that controls the outputs (valid data or high impedance). Third is the write enable (WE) thatselects read or write cycles.

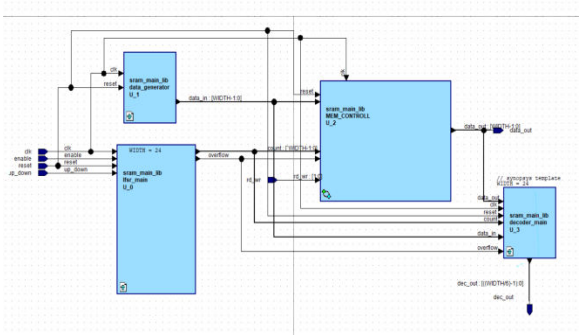

Figure1: Functional Block diagram of SRAM

A Circuit Partitioning

A conventional memory has a single core with input/output block, control and the decoding circuit builds around it. This arrangement works well for a small memory, but as the memory size increases, the load (capacitive and the resistive) on the word lines and bit lines also increases which in turn reduces the speed of the memory. If by any means we can reduce the resistive and the capacitive load, we can control the delay. The popular approach is to divide the core into numberof pages and banks, this approach is good for both power and speed as the load on bitlines and wordlines is reduced, but it is not an area efficient solution as we need to have local wordlines and decoders for each page which increases the area. A very simple approach is to just split the core in two parts (see fig. 2) and use the same wordline driver for it This way there will be two paths for the driver and each of the paths will see half of the capacitive and resistive loads as compared to the case in which there is only a single core.

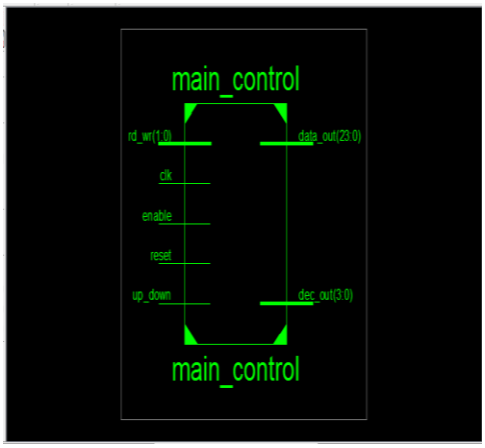

Figure 2: Functional Block diagram of SRAM

3.2 B Dual Vth Usage

In order to gain in speed, reducing the threshold voltage is a very effective

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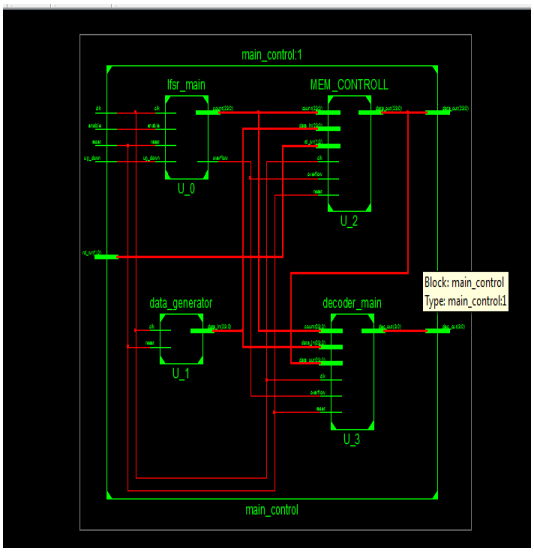
technique. It is also advantageous at low voltage operations where we gain both in terms of speed and power. We have used this technique to improve the speed of our memory. Excluding the memory cells, the dummy row and the sense amplifier, rest all of the digital logic has been converted to low Vth transistors. The memory cells have been excluded since being very small transistors, the leakage current will increase whereas the gain in speed is almost negligible.



3.3 C DWL Architecture

During an access to some row, the word line activates all the cells in that row and the desired sub word is accessed via the column multiplexers. This arrangement has two drawbacks for macros that have a very large number of columns: the word line RC delay grows as the square of the number of cells in the row, and bitline power grows linearly with the number of columns. Both these drawbacks can be overcome by further sub dividing the macros into smaller blocks of cells using the Divided Word Line (DWL) technique first proposed by Yoshimoto.In the DWL technique the long word line of a conventional array is broken up into k sections, with each section activated independently thus reducing the word line length by k and hence reducing its RC delay by K2. The row selection is now done in two stages, first a global word line is activated which is then transmitted into the desired block by a block select signal to activate the desired local word line. Since the local word line is shorter, it has a lower RC delay. Before Divided Word Line (DWL) technique power is 20.423mw after Divided Word Line (DWL) technique power is reduced to 15.267mw.

3.4 D Low Power Decoders

However, the normal decoder built using logic gates has the following drawbacks. The main problem is that the decoder will require a very large number of transistors. The capacitance associated with the long runs of wires and high gate input count will add to long delays. The address inputs will also have to be buffered to drive this huge capacitance load. The layout will become unnecessarily complex and so more time-consuming. Another problem is that the power consumption of such a decoder will be very high due to the large number of gates. SRAM chips are important components of embedded mobile systems, which generally run on batteries. To overcome these problems, we have used a dynamic NOR decoder. This structure reduces the number of transistors by half. It also increases the speed of the decoder and makes the layout simple and less time-consuming. Before low power decoders power is 15.267mw after using of low power decoder's power is reduced to 12mw.

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3.5FSM DESIGN FOR SRAM CELL MAIN CYCL E:

The SRAM memory cell consist of case MAIN_CYCLE in their current_ state MAIN_CHECK: begin input d1=0; d2=0; d3=0; d4=0; if rd = 2b'00 then data_ out=0 Read operation begin its reads the given input data ,else if rd_ en=1; then hold the read operation into the rd_ wait condition either if wr = 2b'01 then perform write operation begin the given input data is stored or wrote ,else if wr_ en=1; then hold the write operation into the wr_ wait condition either if wr = 2b'10 then it's perform Read-write operation, Neither else if rd_ wr en=1; then hold the read_write operation into the rd_ wr wait condition else if default b'11 or MAIN_CHECK=Next stage its restart the program else if end the program.

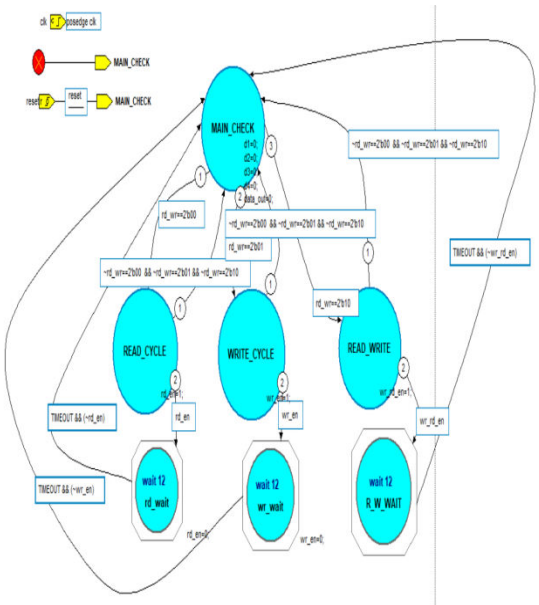

Figure 3 for SRAM_ main cycle

3.6 BACK END DESIGN PROCESS AND ITS IMPLEMENTATION FOR SRAM CELL:

The standard cell comprises six transistors, as shown in Figure 1. The nMOS access transistors (A1 and A2) located at the ends of circuit and a pair of cross-coupled inverters constitute memory cell. The nMOS elements (D1 and D2) of the latch are the driver transistors, while pMOS (P1 and P2) are the pull-up transistors. The access transistors operate when the word line is raised, for read or write operation, connecting the cell to the bit lines (Bit line, ~Bit line). The cell has three different operation modes.

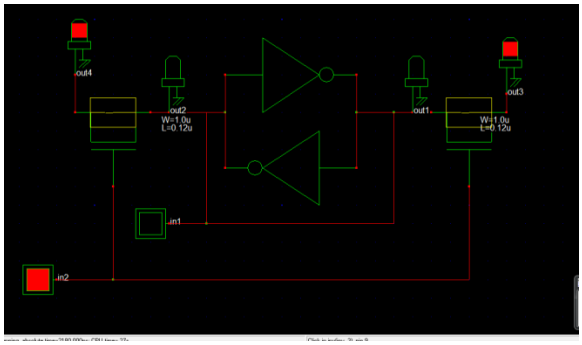

Figure 4 SRAM Schematic diagram in back end design

In the standby state, word line is not asserted, so access transistors are turned off. Therefore, cell cannot be accessed and two cross-coupled inverters will continue to feed back each other, as long as they are connected to the supply, and data will hold in the latch. The read operation starts by precharging the bit lines high, then allowing them to float. Afterwards, word line is asserted, turning on all access transistors. The data stored in the nodes are driven onto bit lines. A voltage difference is developed between bit lines and a sense amplifier

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detects the value of the cell. below figure for single sram cell.

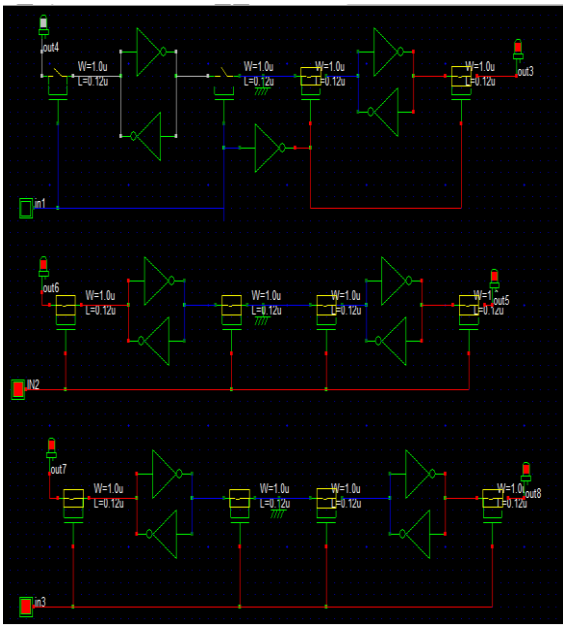

Figure 5 SRAM6T Schematic diagram in back end design

The 6T SRAM cells are divided into four variations that result from the different placement of the two inverters constituting the core of the 6T cell. The first type consists of two sub-types, making a total of five basic cells. Amongst the conventional 1-3 types, type 1b [6] presents characteristics suitable for deep nanoscaling, while type 2 [7] is the most popular design, having been widely used until the 90 nm generation. Due to the increasing lithography limitations of new technology nodes, the type 2 cell was replaced by the lithographically friendly type 4 cell [8], also known as the thin cell [9], which has been the industry standard since 65 nm [4]. The cell is long and skinny, reducing the critical bit line capacitance at the expense of longer word lines. Ishida's categorization has been recently expanded to include a type 5 category, introducing the type 5 ultra-thin cell [10], which, compared to the thin cell, is said to offer lower bit line capacitance, reduced metal complexity and notchless design for improved resistance to alignment induced device mismatch, thus adapting to the increasing scaling and lithographic restrictions.

4.RESULTS AND DISCUSSION

Simulation results for front end

In this Simulation is used for testing, and their all it's functions programs recitifies,functional sequences,timing constraints,and specifications.one has to check here whether all the functions are carried out as expected and rectified by simulation tool. In this we are taken results for read_write operation, read operation,write operation and default operation.In the read _ write operation it's write the data, when overflow is high then stop the write operation and it's reads the given data or stored data. In the read operation reads the given data or stored data. In the write operation it's write the data, when overflow is high then stop the write operation. In the process sram main controller default operation performed. when count[23:0]cycle is completed,or overflow is high then default operation occured to restart the process of program form initally stage of operation with respected inputs and outputs.or stop their processof present operation of program, and end the process of all program.In the simulation process intiallay consider inputs clk is 1with 100 us time period,enable is 1, reset 1 ,up_down is 1 and read_write main check is 01 .then run the program get the result as shown below figure.

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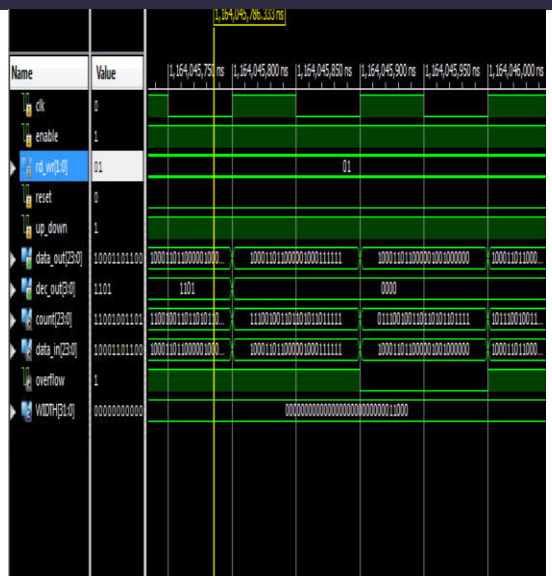

Figure 6 for SRAM write operation simulation'

In the read operation initially consider inputs as clk is 1with 100 us time period,enable is 1, reset 1 ,up_down is 1and read operation main check is 00 .then run the program then its reset the the values ,and chane the reset as 0,and clk is 1 with 100 us and up_down is 0 . Run the simulation get the result for rear operation as shown below figure.

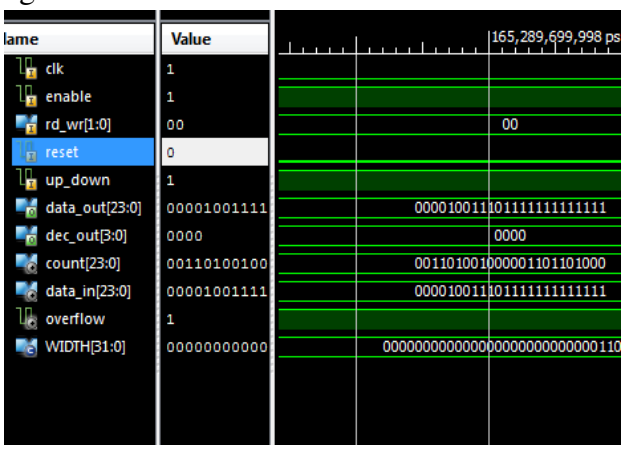

Figure7 for SRAM read operation simulation'

Then change valued for output the reset input is 0,clk input is 1 with 100 us time period and up_down is 1 RUN simulation get the results for read_write operation. In their reset is 0 then read _write opertion will be performed,and if over flow is 1 then stops opertion, as shown below figure for read_write operation.

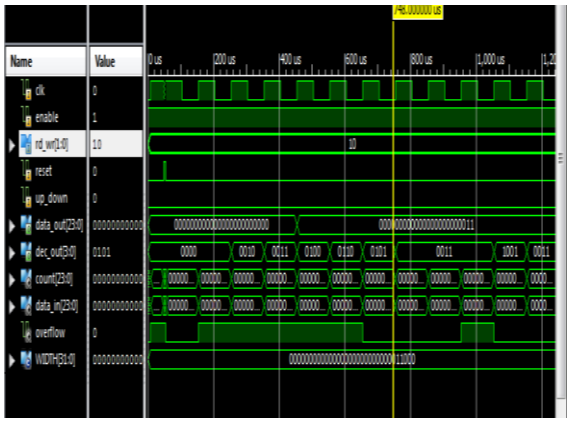

Figure 8 for SRAM read write operation simulation'

layout desing for back end design

The layouts of the examined cell types were implemented using a standard 3-metal CMOS n-well process at the 12um technology node. To ensure both read stability and writability, transistors must satisfy certain dimensional limitations. Additionally, in order to attain good layout density, transistors must be designed to be as small as possible. In general, driver transistors must be stronger than access transistors (read ability) and access transistors should prevail against pull-up transistors (writability).

Design rules and electrical parameters

Layer	Width	Spacing	Surface	Surf capa	Lin capa	Clk capa	Res	Unsalicid	Thickn	Height	Permitt
	lambda	lambda	lambda2	af/µm2	af/µm	af/µm	ohm	ohm	µm	µm	
nitride	0	0	0								
siOxNy	167	167	0								
metal2	5	3	16	16.00	42.00	10.00	0.04/sq	1.00/sq	1.10	2.50	4.00
via	3	4	0				1.00/via		0.50	2.00	4.00
metal	4	3	16	29.00	44.00	10.00	0.08/sq	1.00/sq	0.80	1.20	4.00
poly	2	3	16	63.00			25.00/sq	40.00/sq	0.50	0.40	4.00
poly2	2	2	8				30.00/sq	1.00/sq	0.20	0.27	4.00
contact	2	3	0				1.00/via		1.20	0.00	4.00
diffn	4	3	16	360.00	350.00		300.00/sq	250.00/sq	1.00	0.00	4.00
diffp	4	3	16	340.00	220.00		250.00/sq	300.00/sq	1.00	0.00	4.00
nwell	9	12	144				120.00/sq		3.50	0.00	4.00
oxide				1500.00					25.00nm	(3.00nm)	4.00

OK Techno: CMOS 1.2µm CMOS loaded from file "D:\microwind 3.1 full\Microwind 3.1 Full\rule

Figure 9 for SRAM6T LAYOUT DESIGN RULES'

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In type 1b cell, metal-1 wires are used for the supply voltage (Vdd) and ground (Vss), metal-2 wires for the bit lines and a metal-3 wire for the word line. In type 2 cell, metal-1 wires are used for the supply voltage and ground, metal-2 wires for the bit lines and the word line propagates through a long polysilicon line. In type 4 cell, metal-1 wires are used for the ground, metal-3 wire for the word line and metal-2 wires for the bit lines and supply voltage. In type 5 cell, metal-2 wires are used for the ground, supply voltage and bit lines, while word line is designed by metal-3 wire. Proper contacts are used for the connection of the cells with the various metal layers, the n-wells and the p-substrate. The layouts of the cells are illustrated in Figures 9 and 10 respectively.

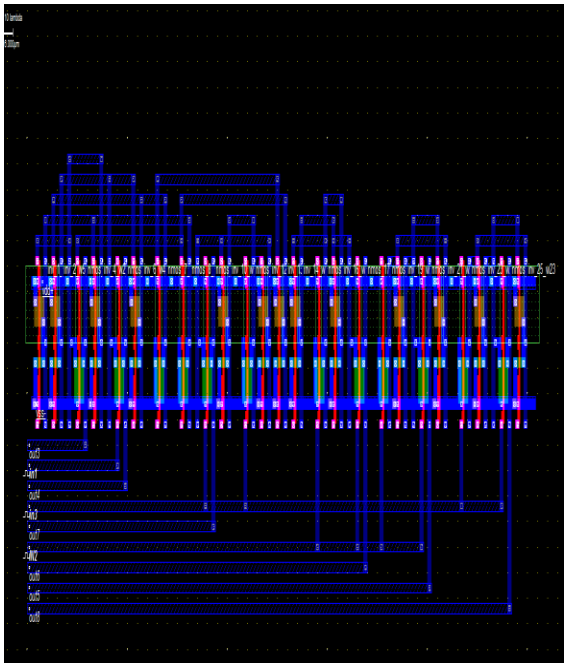

Figure10 for SRAM6T layout design

below figure for layout design of sram 6T cell simulation cursor in 6.41ns at4.14 v and power is 1,713mW.

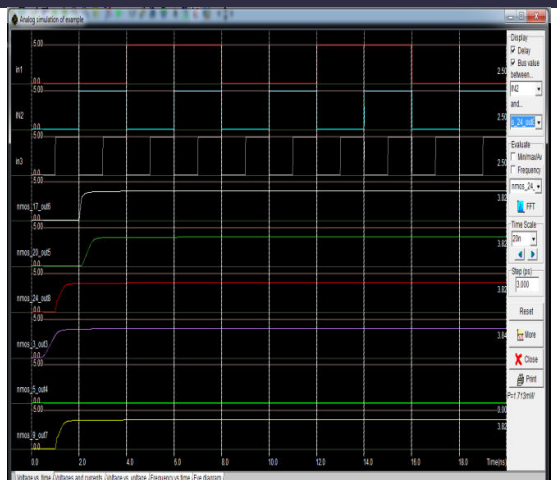

Figure 11 for layout simutation results.

The design which ensures that the design is optimized for the design architecture. as seen below figure for complete circuit usage of logic elements.

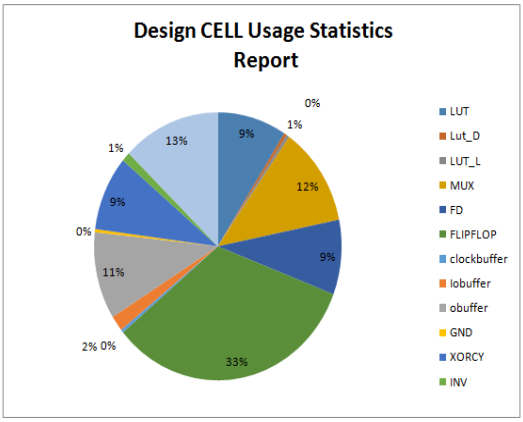

Figure 12: for cell usage of statistics report.

In the below bar chart explains how many numbers of slices ,LUTs, flip_ flop slice, and IOBS, BUGS are available and Its compared to usage of total components.

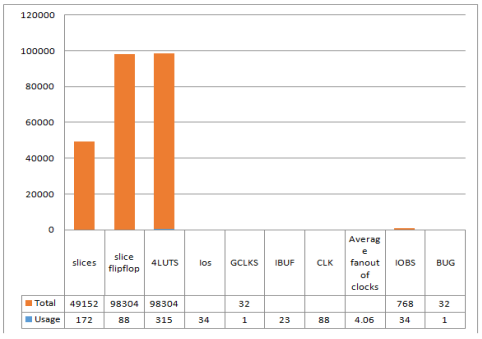

Figure 3: for cell usage of total components.

4. CONCLUSION

This paper work is dedicated to SRAM implementation and addressing of the critical issues in the designing of low power static RAM along with the design techniques used to overcome them. In this work techniques to optimize both of these paths are investigated and implemented. In this paper, all possible technique for SRAM implementation are compared and XILINXs is found to be golden suitable for SRAM implementation using Verilog. With appropriate positioning of memory blocks and the use of proper Verilog constructs, we achieve a high speed static RAM that will not dissipate too much power. We can say that our design is best suitable for advance application like networking etc.

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