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SURVEY ON VLSI USING 8X10 ENCODER & 10X8 DECODER WITHOUT RIPPLE COUNTER

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ABSTRACT:- In recent days the VLSI organization is developing rapidly and it demands for the gadgets which consume much less energy and there may be no effect on their common overall performance. Maintaining the overall performance with an awful lot much less strength intake is the large challenge for the engineers. Therefore, the maximum time is spent at the power reduction with out affecting the overall performance via the VLSI engineers. There are many strategies used to reduce the strength consumption of the design. The format and the implementation of 8x10 encoder and 10x8 decoder. We can lessen the electricity intake of hardware. Less strength intake will virtually results in less charge of the hardware. The VLSI company growing very suddenly with the benefits of lowering power, velocity and location with out modifying the given gadget specs. The essential task in VLSI is to lessen the electricity consumptions as a good buy as feasible. Power may be decreased through manner of clock gating is one of the technique to lessen the power consumption. Clock gating and to keep the disparity is (+2 to -2) approach reduce the power consumption via reducing the unwanted transitions inside the applied clock sign without changing machine specs. In this paper we are used pulse triggering approach and disparity of DC Balance to shop the energy. The verbal exchange gadget consists of encoder and decoder blocks along aspect parallel to serial and serial to parallel converter with respective. These strategies also may be used to reduce the clock skew problem and because of removal of clock skew strength intake may be decreased. In this we have designed the 8x10 encoder and 10x8 decoder the use of VHDL. The 8x10 encoder and 10x8 decoder have mainly talents because of which they're in top notch name for for excessive pace communique. First is low transmission charge and second is DC reimbursement. They have many packages which incorporates PCI precise, USB 3.0, GB Ethernet and plenty of more.

Keywords: Xilinx; Verilog; Altera QUARTUS-II;8x10 encoder and 10x8 decoder;Pulseclock;

INTRODUCTION:

The VLSI engineers offer extra emphasis on the assets used by the hardware. They attempt difficult to lessen the consumption of assets which finally ends up within the increase of the VLSI company. The vital aid comes into role is power. Less strength intake will absolutely leads to lots much less charge of the hardware. Lot of studies goes on reduction of strength consumed with the useful resource of the hardware.There are many techniques which are used to reduce the electricity which include clock gating

and clock divider etc These strategies additionally may be used to lessen the clock skew problem and because of removal of clock skew energy intake can be decreased. USB 3.0 provides the brand new switch fee referred to as Super Speed USB (SS) that might transfer statistics at up to 5 Gbit/s (625 MB/s), which is set ten instances as speedy because the USB 2.Zero popular. Manufacturers are endorsed to differentiate USB three.0 connectors from their USB 2.Zero opposite numbers by way of blue colour-coding of the Standard-A receptacles and plugs, and through the initials SS. In USB three.Zero, dual-bus architecture is used to permit both USB 2.Zero (Full Speed, Low Speed, or High Speed) and USB 3.0 (Super Speed) operations to take region concurrently, for that reason imparting backward compatibility. Connections are such that in addition they allow in advance compatibility, that is, jogging USB 3.Zero gadgets on USB 2.Zero ports. The structural topology is the same, together with a tiered massive call topology with a root hub at degree 0 and hubs at lower tiers to provide bus connectivity to devices In this paper, we've designed the 8x10 encoder and 10x8 decoder using Verilog HDL. The encoder and decoder is applied with 3-bit down ripple counter to enhance the clock skew which definitely leads to an awful lot much less energy intake of encoder and decoder. The 8x10 encoder and 10x8 decoder have specially functions because of which they may be in extraordinary name for for excessive pace communique. First is low transmission price and 2d is DC compensation . They have many programs together with PCI particular, USB 3.0, gigabit Ethernet and many.

2. ARCHITECTURE

In this paper, we applied three-bit down ripple counter that's one of the strategies to reduce the clock skew hassle. By lowering the clock skew we will capable of reduce the energy consumption of the hardware. We carried out this ripple counter with the encoder and decoder format the use of verilog HDL. There are many methods to put in force the ripple counter depending at the traits of the flip flops used and the requirements of the depend sequence. The running of encoder, decoder and ripple counter layout is illustrated later in this section.The clock ports of the encoder and decoder block are pushed thru the output of the remaining flip-flop of the 3-bit ripple counter. By using ripple counter the consumed power of encoder is reduced. The connection between the encoder and ripple counter block is extra apprehend via the use of the RTL view proven in Fig.1 and the connection the various decoder and ripple counter block is demonstrated through the RTL view in Fig.1

DEVELOPMENTS:

The first semiconductor chips held transistors each. Subsequent advances brought greater transistors, and accordingly, extra individual capabilities or structures had been integrated over time. The first incorporated circuits held just a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or greater common sense gates on a unmarried tool. Now recognised retrospectively as small-scale integration (SSI), improvements in method led to

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devices with hundreds of common sense gates, known as medium-scale integration (MSI). Further enhancements led to huge-scale integration (LSI), i.E. Structures with at least a thousand logic gates. Current technology has moved a ways beyond this mark and trendy microprocessors have many tens of millions of gates and billions of individual transistors.One time, there has been an attempt to name and calibrate numerous stages of huge-scale integration above VLSI. Terms like ultra-huge-scale integration (ULSI) were used. But the huge quantity of gates and transistors available on not unusual gadgets has rendered such first-class distinctions moot. Terms suggesting greater than VLSI ranges of integration are not in extensive use.

In 2008, billion-transistor processors became commercially available. This have become extra not unusual as semiconductor fabrication advanced from the then-modern-day era of sixty five nm strategies. Current designs, not like the earliest devices, use good sized design automation and automated good judgment synthesis to lay out the transistors, permitting higher degrees of complexity in the ensuing good judgment capability. Certain excessive-performance good judgment blocks just like the SRAM (static random-get admission to memory) mobile, are nevertheless designed via hand to ensure the highest performance.

RIPPLE COUNTER

A ripple counter is an asynchronous counter wherein handiest the primary flip-flop is clocked by means of an outdoor clock. All subsequent flip-flops are clocked by way of way of the output of the preceding flip-flop. Asynchronous counters also are referred to as ripple-counters because of the manner the clock pulse ripples it manner thru the flip-flopsIn the ripple counter format, the succeeding flip flop clock port is pushed through the preceding turn flop output port as proven in Fig.1. The clock skew is reduced by means of using this because of the reality the turn flops don't toggle on the same clock. The first flip flop is clocked at the excessive first-class fringe of the CLK sign and the second one and the 1/three stage flip flops are clocked at the exquisite edge of the output of the previous Flip flop

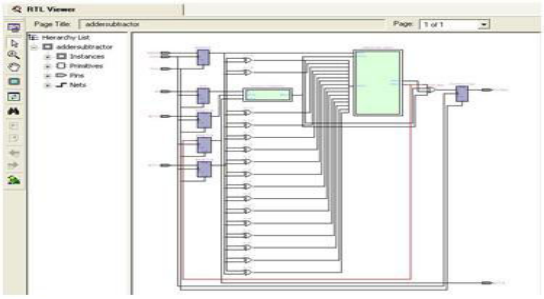

Fig:RTL Semantic Ripple Counter

LITERATURE SURVEY:

In nowadays's time the VLSI industry is growing swiftly and it needs for the gadgets which consume less energy and there's no effect on their overall performance. Maintaining the performance with much less energy consumption is the big undertaking for the engineers. Therefore, the maximum time is spent on the energy discount without affecting the overall performance via the VLSI engineers. There are many techniques used to reduce the strength consumption of the layout. Less strength consumption will absolutely ends in less value of the hardware. Lot of studies goes on discount of energy fed on with the aid of the hardware.Clock Gating is a technique used for reduction of energy within the virtual

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layout through clock net. In clock gating technique the clock is disabled on the scenario in which it isn't always important, for this reason this reduces the electricity consumption. Clock gating in reality transfer off the clock in which it's far unnecessarily consumes electricity. By doing this the energy intake is less without affecting the overall performance of the layout. There are various techniques used for clock gating as: NAND gate, AND gate, latch based totally AND/NOR gate clock gating, multiplexer based totally clock gating. The present day method for clock gating generation is using of terrible/superb latch. There are many techniques which can be used to lessen the strength such as clock gating and clock divider and so on these strategies also can be used to reduce the clock skew problem and because of removal of clock skew strength intake may be decreased. In this paper, we've designed the 8x10 encoder and 10x8 decoder using Verilog HDL. The encoder and decoder is applied with three-bit ripple counter to improve the clock skew which without a doubt ends in less power intake of encoder and decoder. The 8x10 encoder and 10x8 decoder have specifically two capabilities due to which they're in incredible demand for excessive speed verbal exchange. First is low transmission fee and second is DC repayment. They have many programs inclusive of PCI specific, USB 3.Zero, gigabit Ethernet and plenty of extra.The 8b/10b coding scheme was to begin with proposed through Albert X. Widmer and Peter A. Franaszek of IBM Corporation in 1983. This coding scheme is used for high-speed serial statistics transmission. The encoder at the transmitter side maps the 8-bit parallel statistics enter to 10-bit output. This 10-bit output is then loaded in and shifted out thru a excessive-pace Serializer (Parallel-in Serial-out 10-bit Shift Register). The serial statistics stream might be transmitted thru the transmission media to the receiver. The excessive-pace Deserializer (Serial-in Parallel-out 10-bit Shift Register) on the receiver aspect converts the obtained serial data flow from serial to parallel. The decoder will then remap the 10-bit information returned to the original eight-bit facts. When the 8b/10b coding scheme is hired, the serial facts movement is DC-balanced and has a most run-duration with out transitions of five. These traits resource in the recuperation of the clock and statistics at the receiver. Figure 3.2 suggests the 8b/10b encoder/decoder utilization in a conversation device.

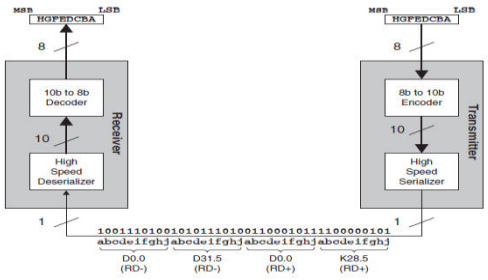

Fig 4.2: The 8b/10b Encoder/Decoder in a System.

4.2.1 DC Balance and Run Length:

A DC-balanced serial information stream way that it has the identical quantity of 0s and 1s for a given duration of statistics movement. DC-stability is critical for sure media because it avoids a price being constructed up in the media. The run-duration is described because the maximum numbers of contiguous 0s or 1s in the serial data flow. A small run period facts

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movement offers facts transitions inside a small period of information. Data transitions are critical for clock healing. The PLL of the CDR generates a section-adjustable output clock from the reference clock input. Transitions at the serial information circulate offer the transmission clock section statistics to the PLL and permit the PLL to recover the transmission clock with the precise phase. Note that the reference clock input is constantly vital for the CDR. The serial records circulate embeds the segment of the transmission clock, now not the clock itself. This reference clock comes from the receiver system, now not the transmitter gadget.

4.3 8B/10B CODE MAPPING:

The 8b/10b encoder converts 8-bit code groups into 10-bit codes. The code groups include 256 data characters named Dx.y and 12 control characters named Kx.y.

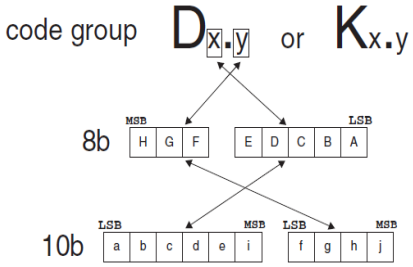


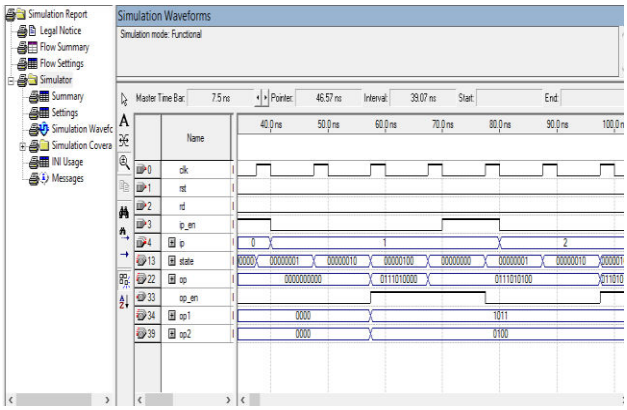
Fig 4.3: The 8b/10b Coding Scheme

The coding scheme breaks the original 8-bit data into two blocks, 3 most significant bits (y) and 5 least significant bits (x). From the most significant bit to the least significant bit, they are named as H, G, F and E, D, C, B, A. The 3-bit block is encoded into 4 bits named j, h, g, f. The 5-bit block is encoded into 6 bits named i, e, d, c, b, a. As seen in Figure 4.3, the 4-bit and 6-bit blocks are then combined into a 10-bit encoded value.

Simulation Result

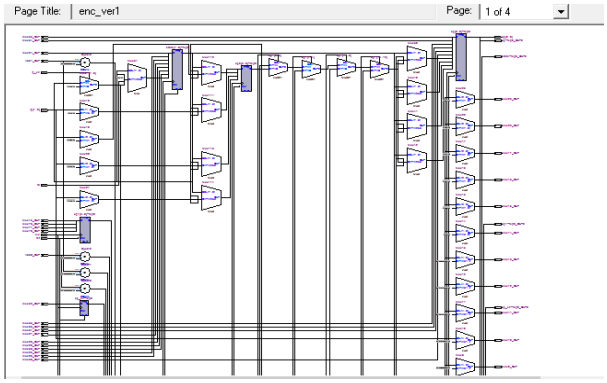
The 8x10 encoder, 10x8decoder and ripple counter circuit are implemented using verilog HDL and stimulated on ModelSim 10.3c. The RTL and the technology view of the encoder with ripple counter and decoder with ripple counter is done in Quartus II software . **Fig-2:** Demonstrations the stimulation waveforms of the 3bit down ripple counter **Fig-3:** Stimulation Output of 3-bit Down Ripple counter The 8x10 encoder with ripple counter circuit is shown in Figs.4. In these figures the encoder clock port is driven by the output of the ripple counter

5.2.1 8b/10b encoder:



5.2.2 RTL schematic for encoder:

The 10x8 decoder with ripple counter circuit is shown in Figs.6, 7, eight. In these figures the decoder clock port is pushed via the output of the ripple counter



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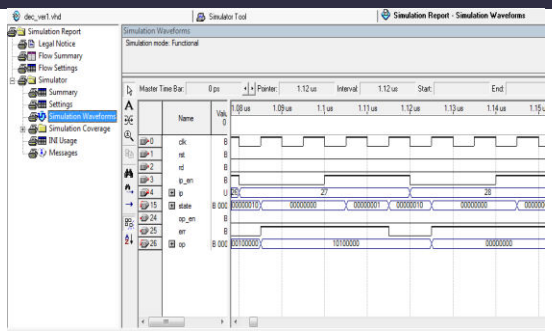

Fig 5.3: Decoder Simulation

CONCLUTION:

In this paper we will lessen the power intake of 8x10 encoder and 10x8 decoder. The encoder & decoder circuit consumes much less electricity and also avoids the hassle of clock skew and jitter problems by the technique of clock gating and disparity (+2 to -2). The 8x10 encoder and 10x8 decoder are demonstrated using FPGA and CAN in Quartus II model 9.1. These powers are calculated via the usage of VHDL power analyser of Quartus II 9.1sp2. It enhance the transmission traits of data to be transferred Coding Gain. The transitions in the PHY bit movement to make clock recovery possible on the receiver. It give unique code-organizations for clean analyze bit sample which assists a receiver for USB three.Zero packages. In this paper many of the 10bits facts we're the use of simplest 8bits data and closing 2 bits are used as a clock. And we also can put into effect the 64x66 encoder/decoder and 128x130 encoder/decoder.

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