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HIGH STEP-UP CLOSED LOOP CONTROLLED DC-DC CONVERTER WITH MINIMUMOUTPUT VOLTAGE RIPPLE

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ABSTRACT A new high step-up dc–dc converter with high voltage gain is proposed on this work. This converter is suitable for the applications with a high voltage gain between the input and the output. The proposed converter combines the it is possible to extend the topology by increasing the number of active–passive inductor cells. High voltage gain with lower duty cycle, low-current and –voltage stresses on switches, small inductors, and small size of filter are the main advantages of the proposed structure. The proposed converter is analyzed in different operating modes. In order to design the components' values of the proposed converter, the equations of output voltage ripple are calculated in each operating mode and a design procedure is proposed based on the aforementioned equations.. In order to verify the feasibility topology; principle of operation, simulation analysis, and closed loop operation, reference and line regulations and waveforms are shown.

Index Terms—Active–passive inductor cell (APIC), high step-up dc–dc converter, high voltage gain, output voltage ripple (OVR).

1. INTRODUCTION

The future is looking towards alternative power sources allof which will need to be regulated in one Form or another.To make this possible, a highly efficient low cost productwill have to be designed. Among all the different converterdesigns only a few are capable of providing high powerwith high efficiency. The basic switched-mode dc–dcconverters including buck, boost, buck-boost, cuk, zeta, andsepic have been used in various electronic applications dueto their numerous advantages such as good performance,simple structure, , high efficiency, easy design, and simplecontrol circuit. To get high voltage from low voltage boostconverters are used. The high voltage converters arewidely used in many industry applications, such asphotovoltaic systems, fuel cell systems, electric vehicles,and high intensity discharge lamps. PV cells can beconnected in series in order to obtain a large dc voltage.Though PV cells can be made into array and connected inseries to produce high voltage there exist serious problemslike shadowing effects, short circuit which drasticallyreduces its

efficiency. In order to overcome such adverseeffects this micro source energy is utilized by the high stepup converter to produce high voltage and satisfy thedemands. Thus high step up dc-dc converters are used asfront end converters to step from low voltage to highvoltage which are required to have a large conversion ratio,high efficiency and small volume [2].The conventional boost converters are not suitable for thehigh step-up conversion [3] applications because the dutycycle of the boost converter with high step-up conversionis large, which results in narrow turn off time. Theextremely narrow turn-off time will bring large peakcurrent and considerable conduction and switching losses[4] .conventional boost converter is shown in fig(1).However extreme duty ratio will result in serious reverserecovery problems and electromagnetic interferences.Impacts of SiC (silicon carbide) MOSFETS on converter,switching and conduction losses are reduced even thoughfast switching is done. Si diodes have ideal, but sill SiCdevices processes large amount of ringing current at turnoff relatively to other devices. And the SiC are comparing0with Si [5].Forward converter, push-pull converter and flybackconverters are transformer based converters (isolatedconverters) ,can achieve high voltage gain by adjusting theturns ratio of the transformers. But it has thedisadvantages of voltage spike across the main switch andpower dissipation due to leakage inductance of thetransformer [7] and safety standard needs [8]. In [9] itproposes a novel single switch high step-up converter. Thecoupled inductor is act as both forward and flybackconverter, thus it can charge two capacitors in parallel anddischarge in series.A high gain transformer less converter is presented in[10]. It consisting of a hybrid combination of two twolevel dc/dc converters . Thus it have large no ofcomponents and it will increase cost. Switched capacitortechniques have been used widely inorder to improve highvoltage gain [11-12]. But here high charging current willflowing through main switch and increase the conductionlosses.

Converters with charge pump will provide voltage gainin proportion to the stage number of capacitors, but itsdrawback includes fixed voltage gain and large device area.In [15] diode capacitor techniques are implemented. It canachieve high voltage gin in proportional to the number ofstages, which is able to be extended by adding capacitorsand diodes. But it may result in the larger voltage dropconsumption due to cut in voltage of the diodes in series.Tapped inductor technology is explained in [13].Different converter topologies are explained. Coupledinductor based converters also achieve high step-upvoltage gain by adjusting the turns ratio [14]. However thestored energy in the leakage inductor causes a voltagespike on the main switch and deteriorates the conversionefficiency. To overcome this problem, coupled inductorbased converter with active clamping circuits arepresented [16].It compare proposed converter andconventional boost converter with coupled inductor onlyand active clamp circuit only. High step-up converter withtwo switch [17-19] and one switch [20] are explained. Asno of switches increased losses will increased. However theconversion ratio is not large enough.

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2 PROPOSED CONVERTER

The power circuit of the proposed converter is shown in Fig. 1. The operation of this converter in continues conduction mode (CCM) is classified into complete inductor supply mode (CISM) and incomplete inductor supply mode (IISM). Discontinues conduction mode (DCM) just includes IISM. To simplify the analysis, all elements are assumed ideal and also the capacitance of capacitors is considered high and all of the inductors have the same inductance. In the proposed converter, by comparing minimum current of inductors with load current, CISM and IISM operations are determined. In CISM, the minimum current of inductors is more than the load current, whereas in IISM, the minimum current of inductors is less than the load current. Current and voltage of the inductor, the capacitor current, and the output voltage waveforms during operational modes are shown in Fig. 2.

3. ANALYSIS THE PROPOSED CONVERTER

A Analysis of the Proposed Converter in CCM

Time interval of Ton: All of the switches are turned ON simultaneously and diodes D12, D22, . . . , Dn2 and D11, D21, . . . , Dn1, Do are turned ON and OFF, respectively. The voltage across the inductors is given by

$$v_L = V_i. \tag{1}$$

Current of inductors is as follows:

$$i_L = \frac{V_i}{L}t + I_{LV}. \tag{2}$$

Considering (2), during this time interval, the inductors are charged and the current through them is increased so that in t = DT , the inductors current will be at its maximum value. Applying t = DT to (2), the maximum current of inductors is obtained as follows:

$$I_{LP} = \frac{V_i DT}{L} + I_{LV}. \tag{3}$$

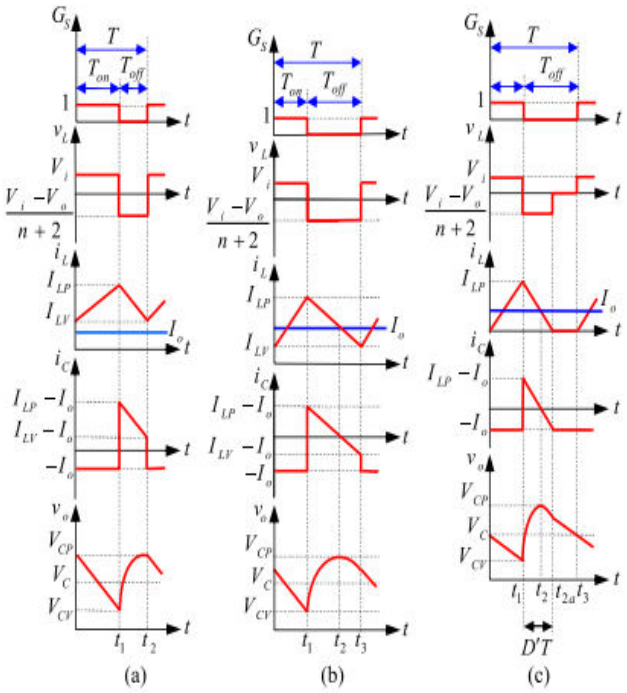

Fig.2. Voltage and current waveforms. (a) CISM-CCM. (b) IISM-CCM. (c) IISM-DCM.

During this time interval, the capacitor current equals to –Io and provides load current. At the end of this time interval, the capacitor energy is discharged and its voltage is decreased to VCV .Time interval of Toff : The switches are turned OFF simultaneously and diodes D12, D22, . . . , Dn2 and D11, D21, . . . , Dn1, Do are turned OFF and ON, respectively. The voltage across the inductors is given by

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$$v_L = \frac{V_i - V_o}{n+2} \tag{4}$$

Where n is the number of the APICs. By assuming t1 = 0 (new time base), the inductors' current is calculated as follows:

$$i_L = \frac{V_i - V_o}{(n+2)L} t + I_{\mathrm{LP}}. \tag{5}$$

In this time interval, the inductors are discharged and at the end of this time interval, their current is reached to ILV . Applying t = (1 − D)T to (5), the minimum current of inductors is given by

$$I_{\mathrm{LV}} = \frac{(V_i - V_o)(1-D)T}{(n+2)L} + I_{\mathrm{LP}}. \tag{6}$$

During Toff , the capacitor current is calculated as

$$i_C = \frac{V_i - V_o}{(n+2)L} t + I_{\mathrm{LP}} - I_o. \tag{7}$$

Considering (7), the currents of capacitor and inductors are decreased [see Fig 2(a)]. The inductors provide load current and also along charge the capacitor. During Toff , the capacitor is charged and its voltage is increased from VCV to VCP. The time interval of Toff in IISM-CCM is divided into times intervals of (t1, t2) and (t2, t3).Time interval of (t1, t2): Considering (6), as iL decreases, iC will decrease and reaches zero at the moment of t2. Considering Fig. 2(b) and (7), iC decreases same as iL. iC decreases to the value of ILV − Io at the moment of t3. The inductor and capacitor provide the load current together at this time interval. Voltage gain Calculation: By applying the volt-second balance law, and considering (1) and (4), the voltage gain is obtained as follows:

$$M_{\mathrm{CCM}} = \frac{V_o}{V_i} = \frac{1 + (n+1)D}{1 - D}. \tag{8}$$

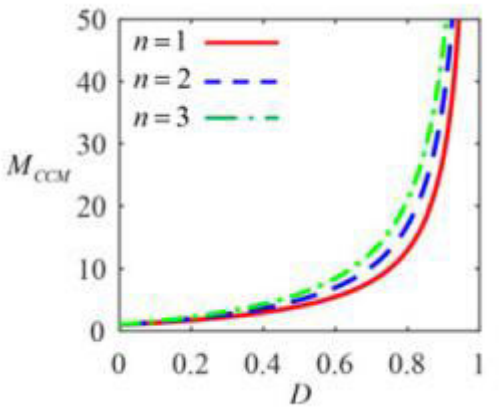

Fig. 3.Variation of voltage gain versus duty cycle and n.

Fig. 3 shows the variation of voltage gain versus duty cycle and n in CCM. As can be seen for certain value of duty cycle, as the value of n increases the voltage gain will be increased. Voltage stress of the diodes and switches: Similarly to the voltage gain, the normalized voltage stress of the diodes and switches versus output voltage can be obtained by applying volt-second balanced law. These results are given in Table I.

B. Analysis of the Proposed Converter in DCM

This mode is divided into four time intervals. Time interval of Ton: Analysis of the proposed converter at this time interval is same as the CCM, which was mentioned before. By applying ILV = 0

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and t = DT in (3), ILP is obtained as follows:

$$I_{\mathrm{LP}} = \frac{V_i DT}{L}.$$

(9)

Time interval Toff : This time interval is divided into three time intervals of (t1, t2), (t2, t2a), and (t2a, t3). Time interval of (t1, t2): iC and iL can be obtained from (5) and (7). The energy transmission process is same as CCM during (t1, t2) [see Fig. 2(c)].Time interval of (t2, t2a): The energy transmission process is same as the CCM during (t1, t2) with a difference that iL is zero in t = t2a. In this time interval, capacitor's current equals load current. According to Fig. 2(c), the capacitor voltage decreases as the capacitor energy is discharged. Assuming t1 = 0 (new time base), ILP is as follows:

$$I_{\mathrm{LP}} = \frac{(V_o - V_i)D'T}{(n+2)L}.$$

(10)

By applying (9) to (10), D is obtained as follows:

$$D' = \frac{(n+1)V_i D}{(V_o - V_i)}.$$

(11)

Time interval of (t2a, t3): At this time interval, iC equals (−Io). The capacitor provides the load current alone. The capacitor's voltage decreases as the capacitor's energy is discharged [see Fig. 2(c)]. Voltage gain calculation: By using the current-second balance law for capacitor, voltage gain in DCM is obtained as follows:

$$\frac{V_o}{V_i} = \frac{1}{2} + \sqrt{\frac{(n+2)RD^2}{2Lf} + \frac{1}{4}}.$$

(12)

4 CRITICAL CONDUCTION MODE

In order to determine the critical inductance between different operating modes, first, ILV should be obtained.

A Critical Inductance Between CCM and DCM

The maximum current of inductors can be obtained as follows:

$$I_{\mathrm{LP}} = I_o\left[\frac{1}{1-D} + \frac{RD}{2Lf}\frac{(1-D)}{[1+(n+1)D]}\right].$$

(13)

By applying (13) in (6), ILV is obtained as follows:

$$I_{\mathrm{LV}} = I_o\left[\frac{1}{1-D} - \frac{RD}{2Lf}\frac{(1-D)}{[1+(n+1)D]}\right].$$

(14)

By applying ILV = 0 in (14), the critical inductance between CCM and DCM is obtained as follows:

$$L_C = \frac{(n+2)(V_o - V_i)V_i^2 R}{2fV_o[(n+1)V_i + V_o]^2}.$$

(15)

B. Critical Inductance Between CISM and IISM

By applying ILV = Io in (14), the critical inductance between CISM and IISM is obtained as follows:

$$L_K = \frac{(n+2)RV_i^2}{2fV_o[(n+1)V_i + V_o]}.$$

(16)

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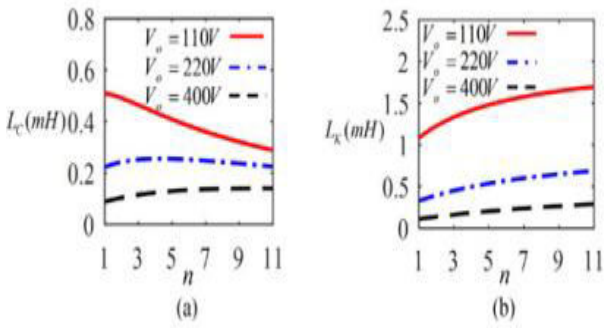

Fig. .4. (a) Variation of LC versus n. (b) Variation of LK versus n

Variations of the critical inductances versus n are shown in Fig. .4. Considering Fig. 4(a), it is obvious that the critical inductance is decreased as the output voltage is increased. Therefore, for low value of inductance when the output voltage is high, the converter can operate in CCM. This figure shows that by increasing the number of APIC, LC is decreased and LK is increased.

5 COMPARISON

In this section, the proposed converter is compared with the literature. For comparison, some important indexes are shown in Table II. Variation of the voltage gain versus duty cycle is shown in Fig. 5(a). As it is shown, voltage gain of the proposed converter for n = 5 is more than the other converters. It is obvious that for lower duty cycles, voltage gain of the converter proposed in [15] is more than the others. But in this condition, the converter is not applicable in high voltage. Variation of the normalized voltage stress of the switches versus voltage gain is shown in Fig. 5(b). As can be seen the voltage stress of S is less than the others. As it is shown S is more than the others, for specific voltage gain. But by considering Fig. 5, this voltage gain for the proposed converter is obtained for low duty cycles compared with the others. Variation of the maximum current of the switches versus voltage gain is shown in Fig. 5(c). As it is shown, the maximum current through the proposed converter switches is less than the others. It can be concluded for the proposed converter that the voltage stress and conduction loss of the switches is low. In [10], in addition to high current stress caused by using four coupled inductors, leakage inductance causes voltage stress to increase, too. Variation of the normalized power of the inductors versus voltage gain is shown in Fig. 5(d). As can be seen, the power of the proposed converter's inductors is lower than the others. Therefore, the inductance for proposed converter can be selected low; however, the amount of the power is just for one inductor but it is obvious that the summation of the powers is also lower than the others.

6 VOLTAGE GAIN AND EFFICIENCY IN REAL CONDITION

The average current through the inductors is as follows

$$I_L = \frac{I_o}{1-D}. \tag{17}$$

The average input current is as follows:

$$I_i = I_L[(n+1)D+1]. \tag{18}$$

By applying (17) in (18), the average input current is as

$$I_i = \frac{[1+(n+1)D]}{1-D} I_o. \tag{19}$$

The efficiency of proposed converter can be obtained by the following equation:

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$$\eta = \frac{1}{1+\frac{(n+2)(r_s D+r_L)}{R(1-D)^2}+\frac{r_{Do}+Dr_C+nr_{D1}}{(1-D)R}+\sum_{j=3}^{n}\frac{D(n-j+1)^2 r_{Dj}}{(1-D)^2 R}} \quad (20)$$

The voltage gain in real condition is obtained as follows:

$$\frac{V_o}{V_i} = \frac{M_{CCM}}{1+\frac{(n+2)(r_s D+r_L)}{R(1-D)^2}+\frac{r_{Do}+Dr_C+nr_{D1}}{(1-D)R}+\sum_{j=} \quad (21)$$

Variations of voltage gain and efficiency of the proposed converter versus duty cycle are shown in Fig. 6. This figure shows that in real conditions and for high values of duty cycle, by increasing the duty cycle, the voltage gain is decreased.

7 DESIGN OF THE PROPOSED CONVERTER

The designing of the proposed converter is done based on the OVR [22] and [23]. In order to have a minimum OVR, the value of the elements should be selected suitably.

7.1 Output Voltage Ripple

The OVR is calculated as follows:

$$V_{CP} = V_{CV} + \frac{1}{C}\int_0^t i_C dt. \quad (22)$$

According to (22), the OVR in CISM can be determined by integrating the capacitor current in time interval of Ton and also it can be determined in IISM-CCM and IISM-DCM, by integrating the capacitors current in (t1, t2).The OVR in the operation modes of the converter is obtained as Table III. As can be seen, the OVR is independent of inductance values in CISM-CCM and is reversely related with Vi and R. The ratio of the OVR variations is reversely related with inductance, Vi, and R values in IISM-CCM and IISM-DCM.In order to design the converter, it is assumed that Vi,min< Vi <Vi,max and Rmin< R <Rmax. As it is understandable from (15) and (16), LC and LK are functions of Vi and R. For a specific inductance, the converter can operate in one of the modes, whereas the input voltage and load resistance values vary. The minimum and maximum critical inductances are

TABLE II
PERFORMANCE BETWEEN DIFFERENT CONVERTERS

Converter	Conventional	[21]	[15]	[12]	[10]	Proposed
Switches	1	2	1	1	2	$n+2$
Diodes	1	1	3	2	2	$2n$
Inductors	1	1	2	2	4	$n+2$
Voltage gain	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{2-D}{1-D}$	$\frac{1+ND}{1-D}$	$\frac{1+(2N+1)D}{1-D}$	$\frac{1+(n+1)D}{1-D}$
Voltage stress of the switches	V_o	$\frac{V_o(1+M)}{2M}$	$\frac{V_o(1-M)}{M}$	$\frac{V_o(N+M)}{(N+1)M}$	$\frac{V_o[(2N+1)+M]}{(2N+2)M}$	$\frac{V_o[(n+1)+M]}{(n+2)M}$
Summation of Voltage stress of the switches	V_o	$\frac{V_o(1+M)}{M}$	$\frac{V_o(1+M)}{2M}$	$\frac{V_o(N+M)}{(N+1)M}$	$\frac{V_o[(2N+1)+M]}{(N+1)M}$	$\frac{V_o[(n+2)(1+M)+M]+\sum_{j=1}^{n}[(n-j+2)+jM]}{(n+2)M}$
Voltage stress of the output diode	V_o	$\frac{V_o(1+M)}{M}$	$\frac{V_o(M+1)}{M}$	$\frac{V_oN(N+M)}{(N+1)M}$	$\frac{V_o(1+2N)[(2N+1)+M]}{(2N+2)M}$	$\frac{V_o(1+M)}{M}$
The maximum current through the switches	$2I_i$	$\frac{I_i(1+M)}{M}$	I_i	$\frac{(M+N)(1+N)I_i}{M(N+2)-1}$	$\frac{I_i(1+N)(2N+M+1)I_i}{(2N+2)M}$	$\frac{I_i(n+1+M)}{(n+2)M}$
Efficiency P_{out} = 200 W	%98.33	%98.89	%90.5	%93.8	%95.1	%96.35

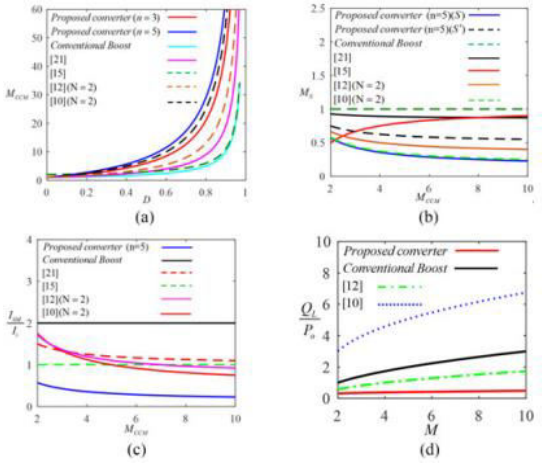

Fig. 5. Variation of (a) the voltage gain versus duty cycle, (b) voltage stress of the switches, (c) maximum current of the switches, (d) normalized power of the inductors versus voltage gain.

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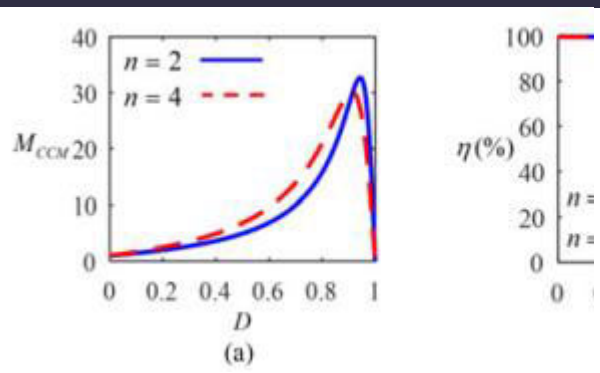

Fig. 6.Variation of (a) voltage gain and (b) efficiency versus duty cycle.

given, respectively, as follows:

$$L_{C,\min} = \frac{(n+2)(V_o - V_{i,\min})V_{i,\min}{}^2 R_{\min}}{2fV_o[(n+1)V_{i,\min} + V_o]^2} \quad (23)$$

$$L_{C,\max} = \frac{(n+2)(V_o - V_{i,\max})V_{i,\max}{}^2 R_{\min}}{2fV_o[(n+1)V_{i,max} + V_o]^2} \quad (24)$$

TABLE III

OUTPUT VOLTAGE RIPPLE IN THE OPERATION MODES

CISM-CCM	$V_{PP}^{CISM-CCM} = \frac{V_0(V_0 - V_i)}{fRC[V_0 + (n+1)V_i]}$
IISM-CCM	$V_{PP}^{CISM-CCM} = \frac{(n+2)(V_0 - V_i)L}{2C} \times \left[\frac{V_0}{(n+2)V_iR} + \frac{V_i}{2Lf[(n+1)V_i + V_0]}\right]^2$
IISM-DCM	$V_{PP}^{IISM-DCM} = \frac{(n+2)L}{2C(V_0 - V_i)}\left[\frac{V_0}{R} + \sqrt{\frac{2V_0(V_0 - V_i)}{(n+2)Lf R}}\right]^2$

TABLE IV

DIFFERENT OPERATIONAL MODES IN THE PROPOSED CONVERTER

VERSUS INDUCTANCE VALUES

State	Operational mode	
$L > L_{C,\max}$	CCM	
$L < L_{C,\min}$	DCM	
$L_{C,\min} < L < L_{C,\max}$	$L > L_C$	CCM
	$L < L_C$	DCM
$L > L_{K,\max}$	CISM	
$L < L_{K,\min}$	IISM	
$L_{K,\min} < L < L_{K,\max}$	$L > L_K$	CISM
	$L < L_K$	IISM

$$L_{K,\min} = \frac{(n+2)R_{\min}V_{i,\min}{}^2}{2fV_o[(n+1)V_{i,\min} + V_o]} \quad (25)$$

$$L_{K,\max} = \frac{(n+2)R_{\max}V_{i,\max}{}^2}{2fV_o[(n+1)V_{i,\max} + V_o]}. \quad (26)$$

Classification of the modes and the operational regions versus the inductance values is shown in Table IV.

7.2 Maximum Output Voltage Ripple

The maximum OVR (MOVR) for a specific inductance value is obtained as Vi,min and Rmin. Due to the different inductance values, the operational region of proposed converter can possess five distinctive sections on the inductance axis. Parameters LK,min and LC,max are significantly related to Vi and R. Therefore, the operation region classification would differ considering LC max <LK,min or LC max >LK,min conditions. Analysis the MOVR for the proposed converter is as same as [22] and [23]. Relation between MOVR in the operational region

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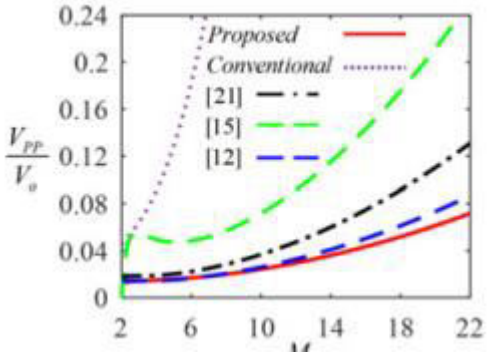

Fig. 7.Variation of the normalized OVR versus voltage gain.

TABLE V
MAXIMUM CURRENT THROUGH THE SWITCHES

CCM	$I_{SP}^{CCM} = \frac{V_o[V_o+(n+1)V_i]}{(n+1)RV_i} + \frac{(V_o-V_i)V_i}{2Lf[V_o+(n+1)V_i]}$
DCM	$I_{SP}^{DCM} = \sqrt{\frac{2V_o(V_o-V_i)}{(n+2)RfL}}$

of proposed converter is as follows:

$$L_{C\max} < L_{K,\min}$$

$$V_{PP1,\max} > V_{PP2,\max} > V_{PP3,\max} > V_{PP4,\max} = V_{PP5,m} \quad (27)$$

$$L_{C,\max} > L_{K,\min}$$

$$V_{PP1,\max} > V_{PP2,\max} > V_{PP3,\max} = V_{PP4,\max} = V_{PP5,m} \quad (28)$$

Variation of the normalized OVR versus voltage gain is shown in Fig. 7. The curves are plotted under the same condition for all of the converters, as can be seen the OVR of the proposed converter is lower than the others for high voltage gains. But it has the same amount as [12] in low voltage gains.

7.3 Current Stress of the Switches

The maximum current of switches equals the maximum current of inductors. The maximum current of switches in CCM and DCM is given in Table V. The maximum value of iS in CCM and minimum value in DCM are obtained for L = LC . Considering (15) in Table V, results in

$$I_{SP,\min}^{DCM} = I_{SP,\max}^{CCM} = \frac{V_o[(n+1)V_i + V_o]}{(n+2)RV_i}. \quad (29)$$

8.Closed loop Operation

The closed loop operation carried out by the voltage controller (PI controller) processes the error signal and produces appropriate current signal (*I*S). The current signal (*I*S) is multiplied with unit sinusoidal template which is produced by using phase locked loop (PLL), to produce *I*S sinωt. The load current *iL*subtracted from the *I*S sin ωt to produce the reference current signal *i*S*. As the boost inductor current can't be alternating, the absolute circuit gives the absolute value of the reference current signal *i*S* that is *iC*. The actual signal (*i*C) and the required reference signal (*iC*) are given to the current controller to produce the proper gating signal. The current controller adopted is a hysteresis current controller. Upper and lower hysteresis band is created by adding and subtracting a band '*h*' with the reference signal *i*C* respectively shown in the Fig. 8. The inductor current is forced to fall within the hysteresis band. When the current goes above the upper hysteresis band, i.e. *i*C *+*h*, the pulse is removed resulting the current forced to fall as the current will flow through the load. When the current goes below the lower hysteresis band i.e. *i*C *-*h*, the pulse is given to the switch, so the current increases linearly.

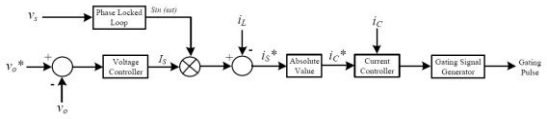

Fig 8 Adopted control scheme for the Closed Loop operation

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9. MATLAB AND SIMULINK RESULTS

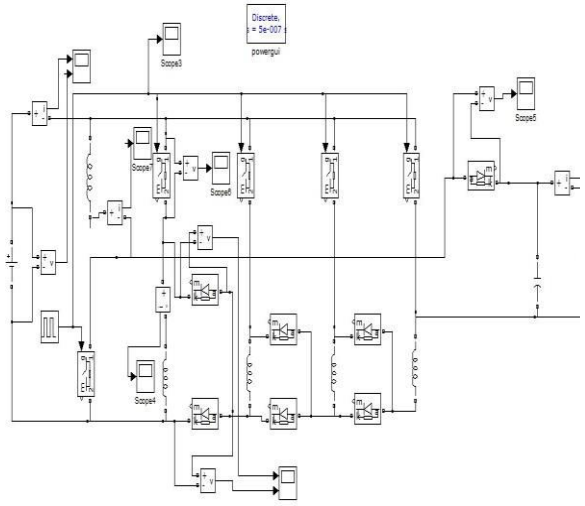
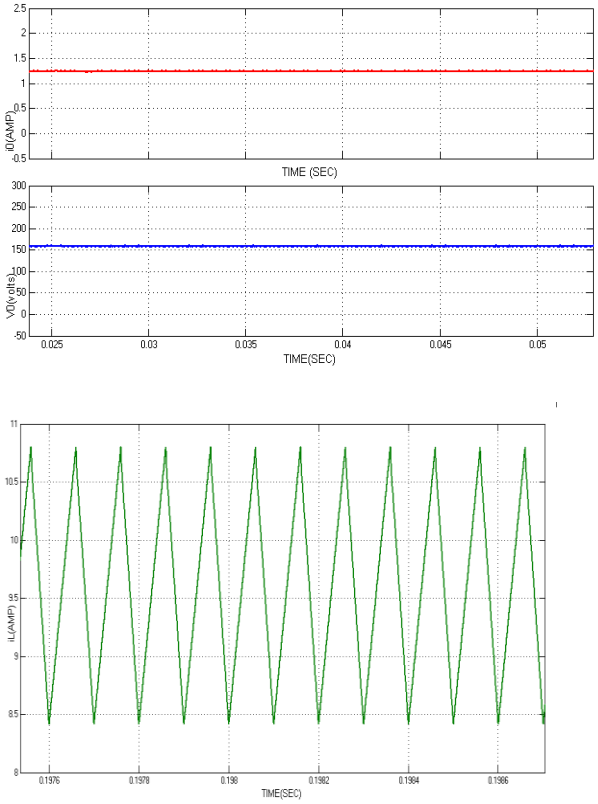
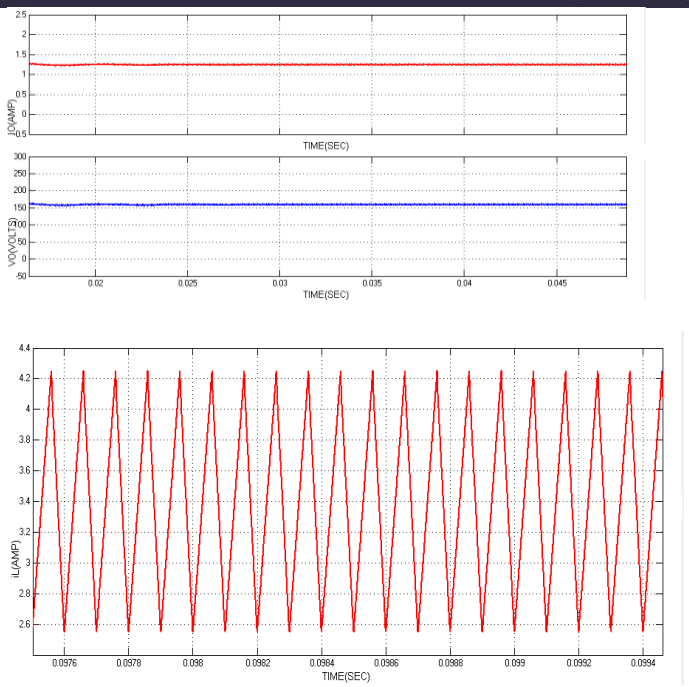


FIG 9 simulink diagram of proposed concept



(a) L= 500 µH.



(b) L = 700 µH.

fig. 10 simulation results for vi,m in = 20 v and rm in = 150 ω.

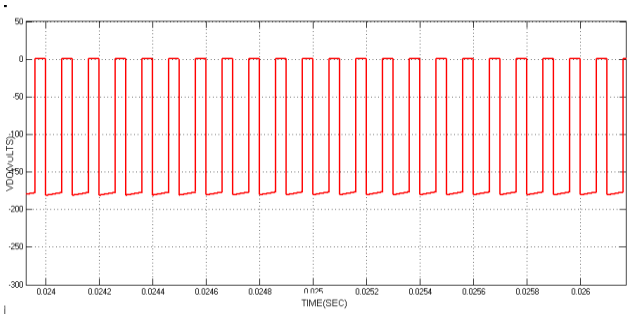


fig 11 Voltage stress of the diode (vdo)

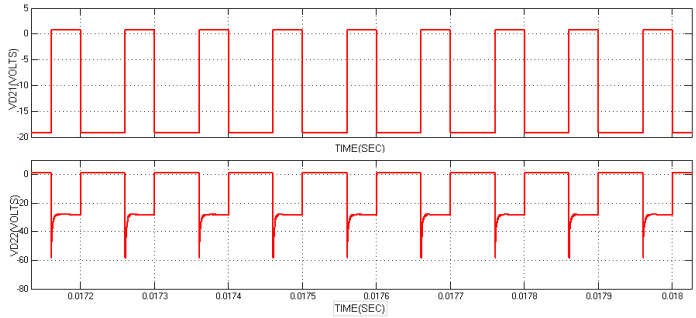


fig 12 Voltage stress of the diodes (vd21 & vd22)

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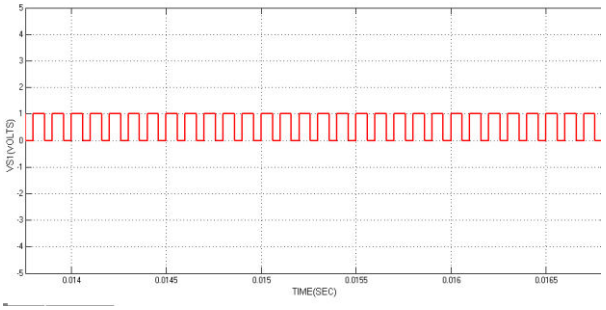

fig 13 Voltage stress of the swithVs1

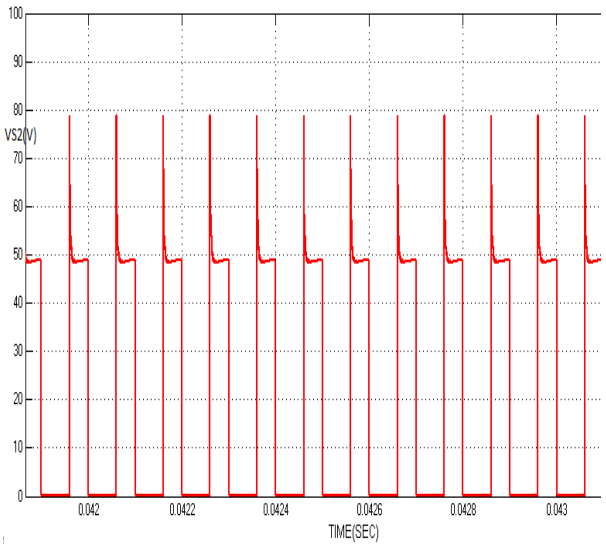

fig 14 Voltage stress of the swithVs1

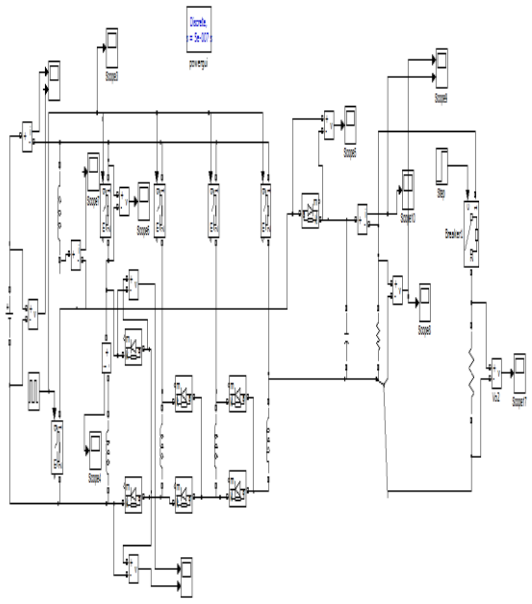

fig 15simulink diagram of sudden load changes of proposed concept

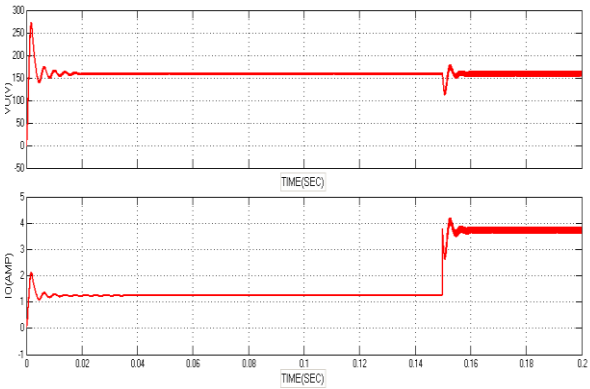

fig 16 resistive load output voltage and current wave forms

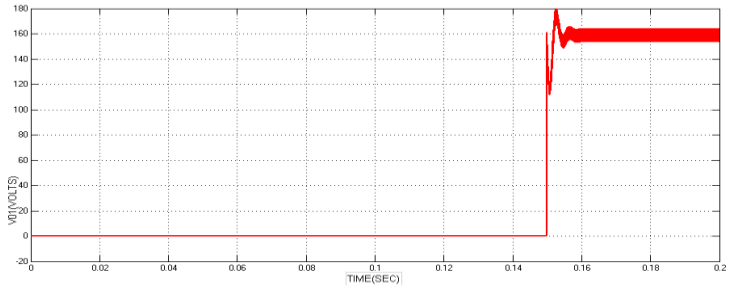

fig 17 sudden load output voltage wave forms

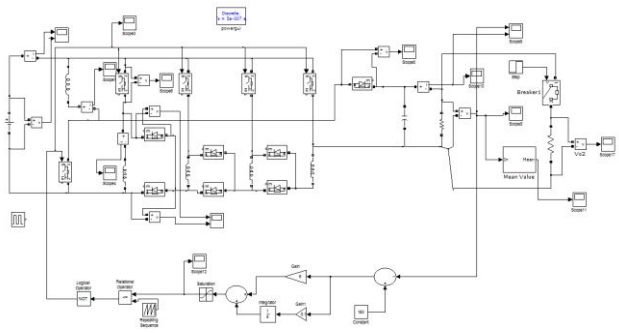

fig 18simulink diagram of proposed concept with closed loop system

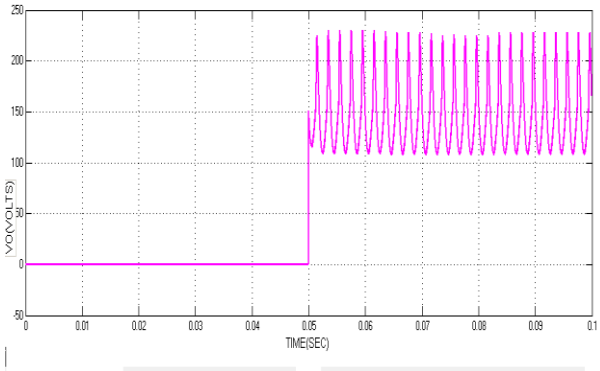

fig 19: final output voltage waveform of closed loop system

9)CONCLUSION

In this paper, a high step-up dc–dc converter was proposed. In the proposed converter by increasing the number of APICs, the voltage gain is increased and voltage stresses on switches is decreased. The high voltage gain has been obtained for low duty cycle that it results in reducing the conduction loss of converter. Maximum current of switches is low that can cause low conduction loss, too. Because of low inductor current ripple, inductor with small inductance is needed, which causes reduction in the size of the magnetic core. Moreover, the critical inductance is reduced by increasing the number of APICs. In the proposed converter, because the switches are turned ON and OFF simultaneously, so, one switching control circuit can be used. The elements of converter were designed based on the maximum output voltage ripple. Closed loop operation of dc-dc converter; line and reference regulations, principle of operation, Simulation analysis, and waveforms are discussed.

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