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DESIGN OF NONVOLATILE HYBRID MTJ/CMOS BASED FULL ADDER

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Abstract:
Very large-scale integrated circuit (VLSI) design based on today's CMOS technologies, arefacing various challenges.Shrinking transistor dimensions, reduction in threshold voltage, and lowering power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design challenges, hybrid MTJ/CMOS based design can resolve the issue of leakage power and bring the advantage of nonvolatility. However, radiation-induced soft error is still an issue in such new designs as they need peripheral CMOS components. As a result, these magneticbased circuits are still susceptive to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Comparing with the previous work, the proposed MFA is capable of tolerating any particle strike regardless of the induced charge. Besides, our MFA circuit offers lower energy consumption in write operation as compared with previous counterparts. We also suggest an incremental modification to the proposed MFA circuit to give it the advantage of full nonvolatility for future nonvolatile microprocessors.

Existing Method:
Magnetic tunnel junction (MTJ) is the basic element of magnetic memories and logics. MTJ is Comprised of three layers including an ultra-thin oxide barrier (e.g. MgO) as the mid-layer And two ferromagnetic (FM) layers in top and bottom (Fig.1). There are two possible modes for the MTJs; first, the parallel mode that refers to the case which both of the FM layers has an identical magnetic direction. And the second, the antiparallel mode that refers to the case which the FM layers are in opposite magnetic directions [6-9]. When an MTJ is in a parallel mode, it shows a lower resistance (denoted by RP) than the case it has an antiparallel mode (with a resistance of RAP).

Proposed Method: Hybrid MTJ/CMOS memory and logic design offers some distinguished features such as very low power consumption, nonvolatility, high endurance, and an easy 3D integration with CMOS technology. Heretofore, a number of MTJ/CMOS-based logic and memory circuits are suggested in the literature. A magnetic latch (mlatch) is proposed. This

circuit includes a CMOS sequential logic for reading the state of MTJs (the sense amplifier), a CMOS combinational logic for reconfiguring the MTJs (the write circuit) and also two MTJ cells. The proposed mlatch circuit offers lower power consumption and also nonvolatility in comparison with the CMOS latches. However, the proposed mlatch is susceptive to radiation-induced SEUs.anothermlatch robust against radiation is proposed. This mlatch uses four MTJs instead of two and therefore, suffers from a high energy consumption for write operation. As discussed in, at least more of total energy consumption in magnetic-based memory/logic circuits is used for the write operation to reconfigure the MTJs. Other radiation hardened (rad-hard) mlatches are proposed in.simple unprotected magnetic flip-flops (MFF) are proposed. This paper proposes a rad-hard MFA (the so-called RHMFA) that is capable of toleration particle strikes with any amount of energy level. Over the previous work, the proposed RHMFA uses only one reconfigurable MTJ and consumes a lower write-energy. We also, suggested a serial rad-hard and also a fullnonvolatile rad-hard MFA based on the proposed RH-MFA.

I. Introduction

As we know the major concern in VLSI is about area, speed and power. But actually there is no much importance given to the power when compared to the speed and area in VLSI circuits. But as per the current growing technology, power has become placing a major role to reduce the power consumption of the electronic circuits. In these applications, average power consumption is a critical design concern. In the absence of low-power design techniques then, current and future portable devices will suffer from either very short battery life or very heavy battery pack. To reduces this power consumption and for good battery life we are proposing a Hybrid- CMOS logic design of the Full adder. Full adder is a basic block for various arithmetic circuits such as multipliers, compressors, comparators etc. The power consumption, requirement and output delay of arithmetic circuits is surely depending upon the power requirement and delay of the full adder circuits. So for designing the high performance arithmetic circuits, minimization of the delay and power of the full adder circuit is required. Several logic styles for designing the Full adder have been proposed. In conventional design of full adder normally single CMOS structure is used for the complete design, Such as the standard static CMOS full adder is based on regular CMOS structure with conventional pull -up and pull-down transistors providing full swing output and good driving capabilities but the main drawback of this circuit is less speed due to more number of PMOS and large capacitance. Now here we are proposing a One bit Full Adder (FA) cell with Hybrid-CMOS logic, and it is the building block for most implementations of addition operations with less area and less power consumption. Full adder circuit which is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALU‟s.

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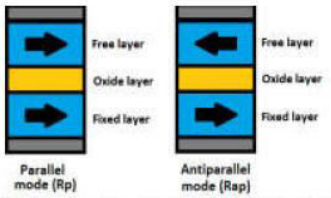

Fig.1. MTJ structure in two modes of parallel and antiparallel

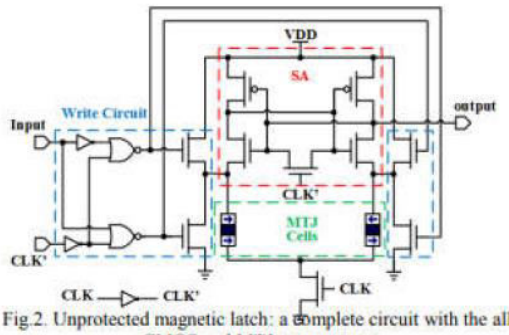

Fig.2. Unprotected magnetic latch: a complete circuit with the all CMOS and MTJ components

The conventional CMOS 28 transistor Full adder, as shown in above Figure 1, is considered as one of the Base case throughout this paper. The circuit is having inputs are a, b, cin and the sum, cout are the outputs of the one bitconventional 28 transistor full adder of 180 nm technology.

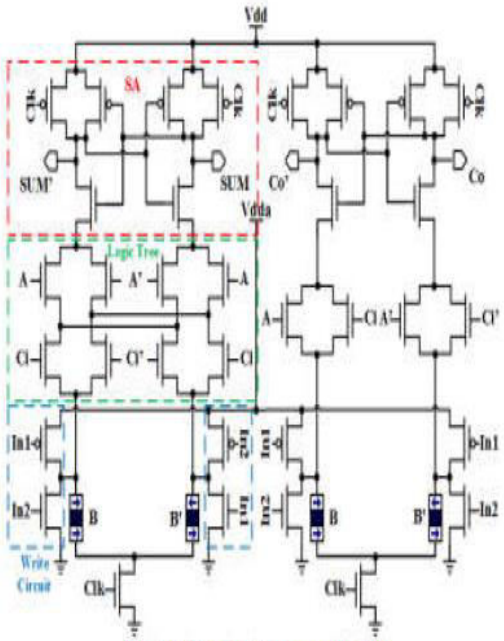

Fig.3. MFA circuit proposed in [7]

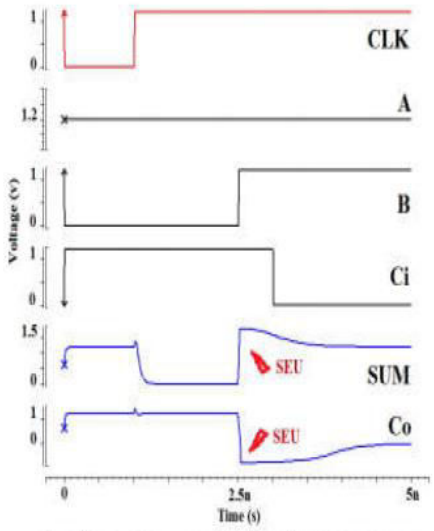

Fig.4. the results associated with SEU injection to MFA proposed in [7]

The above figure 2 represents the proposed one bit full adder with 130 nm technology. In hybrid-CMOS architecture, we get XOR and XNOR operations as module I. Module I circuit is an XOR -XNOR circuit. Many XOR-XNOR circuits are proposed by many authors. Circuit uses only 6 transistors and provides full output swing. This circuit is widely used in hybrid CMOS logic style. Module II and Module III are for the both sum and carry generation as individually. Here we have combined the three modules and designed the one bit full adder of 16 transistors for the 130 nm technology.

Table 1: The truth table of outputs SUM and Co

A	B	Ci	SUM	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

As can be found from the truth table, Co is a majority function of the inputs (denoted by

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Eq. 2). When inputs A and Ci are both the same, Co does not depend on input B. For example, if both A andCi are '1' (in the evaluation phase), the LT of right branch in the output Carry circuit will construct the pulldown path and causes Co′ to go down. When inputs A and Ci disagree, both branches of the LT circuit will being connected and based on the free MTJ configuration, the pull-down path will ben constructed and the related output will be provided. As another example, when A andCi are not the same and input B is '1', Co must be '1'. In this case, the free MTJ will demonstrate a path with lower resistance than the reference MTJ. Therefore, the applied resistance in the left branch becomes smaller than the one at the right side resulting to constructing the pulldown path in the left side. As a result, output Co′ goes '0' and Co stays at '1'. To understand how the sub-circuit of SUM works, we should consider Eq.3 for SUM

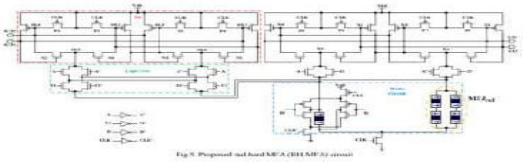
$$Co = AB + AC_i + BC_i$$

$$SUM = A \oplus B \oplus C_i = ABC_i + AB'C_i' + A'BC_i' + A'B'C_i$$

The functionality of the SUM-circuit can be understood easily by tracking the LT's path considering the configuration of the free MTJ. By the rise of the CLK signal, one of the paths will demonstrate a lower resistance regarding this configuration; so its corresponding node will be pulled down and the proper output will be provided. For example, consider the case which A and Ci are respectively '1' and '0' and a value of '1' isstored by the MTJ for input B. The parallel configuration of the MTJ will create a path with lower resistance in the left branch of LT, resulting the pull down of node SX6 and causing the output of '0' for the SUM's value. On the contrary, node SX5 will have no established path to ground and it will be pulledup by Vdd that results in a high logic value for SUM′.

4- Incremented Rad-Hard MFA Circuits

A. A rad-hard and low power serial magnetic binary adder based on the proposed RH-MFA (SRH-MBA) A serial binary adder is a digital circuit that performs binary addition in continuous clock signals. As shown in Fig.7, this circuit employs a full-adder as well as a flip-flop [20]. The fulladder has two direct inputs and a carry-in bit that is the previous calculated carry-out output. This circuit provides two output bits as the SUM and carry-out bits by adding inputs A and B (Fig.7), in a clock cycle. The conventional serial binary adder (shown in Fig.7) suffers from radiation-induced SEUs in the employed flip-flop. This circuit also has high power consumption due to its data storage method. We employed our proposed RH-MFA circuit to design a serial and radhard magnetic adder circuit (shown in Fig.8). Our proposed serial magnetic binary adder uses only two reconfigurable MTJs to save the resulted carry-out (Co) output as the next carry-in (Ci) input.



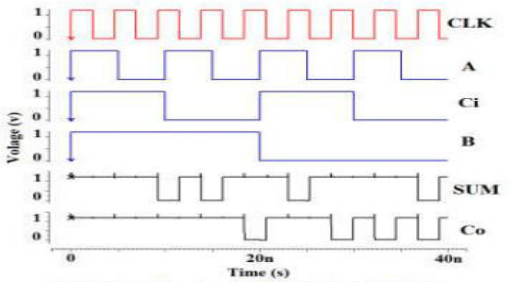


Fig.6. Normal functionality of the proposed RH-MFA

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MTJs are inherently robust against particle strikes. Also, our sense amplifier circuit is radiation hardened. Therefore, the proposed serial magnetic binary adder is robust against SEUs. Also, due to the presence of MTJs in all the paths between the supply voltage and the ground, the issue of leakage current is not concerning. In this circuit, the saved value in each clock signal pulse as the carry-in (Ci), will be restored in by the SA circuit at the next clock rise. In fact, when the clock signal is high, one of the reconfigurable MTJs employed (M1 or M2) is being sensed by the SA circuits and the other one (M2 of M1) is being reconfigured by the write circuit (Fig.8). The MTJ connected to the SA circuits includes the previous Co (as the present Ci) that along with the present inputs A and B, result in the new Co and SUM. At this time, the write circuit reconfigures the other MTJ based on new Co to be used as Ci by the next clock cycle.

B. Proposed fully nonvolatile and radiation hardened MFA (NVRH-MFA) As one of the most promising choices, hybrid design using MTJ and CMOS are being taken into consideration for the future IC designs thanks to their attractive futures such as nonvolatility, high endurance, high performance, CMOS integration compatibility and low power consumption. Nonvolatile nature of the MTJ cells can be used to design full nonvolatile logic circuits. These circuits can be employed to design a nonvolatile microprocessor or any other digital integrated circuit. Also, for the power-gating architectures nonvolatile logics can resume the last state by power on.

In this section, a fully nonvolatile and also rad-hard MFA is proposed. To have nonvolatility, a spin transfer torque magnetic random access memory (STT-MRAM) circuit (shown in Fig.10) is suggested to save inputs A and Ci. This circuit is a lowcost and high-speed MTJ-based memory that is proposed and validated in [6]. As Fig.10 shows, data can be saved by the employed two MTJs. If the clock signal has a logic value of '1', then the path between the supply voltage and the ground will be established through transistors P4-N4 and the MTJ cells. In suggested circuit shown in Fig. 10, there are two modes of write (CLK=0) and read (CLK=1).

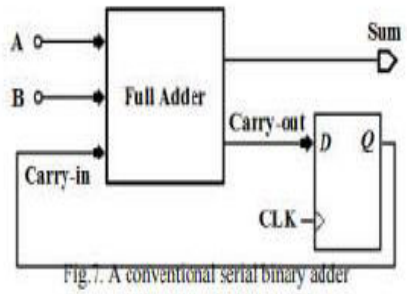

Fig.7. A conventional serial binary adder

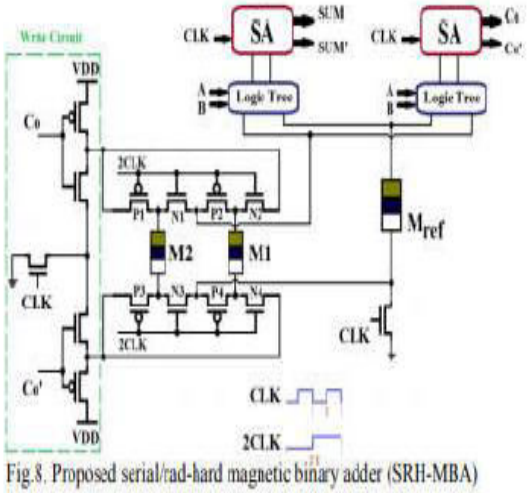

Fig.8. Proposed serial/rad-hard magnetic binary adder (SRH-MBA)

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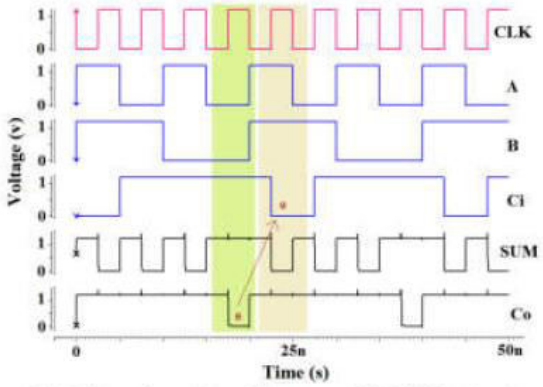
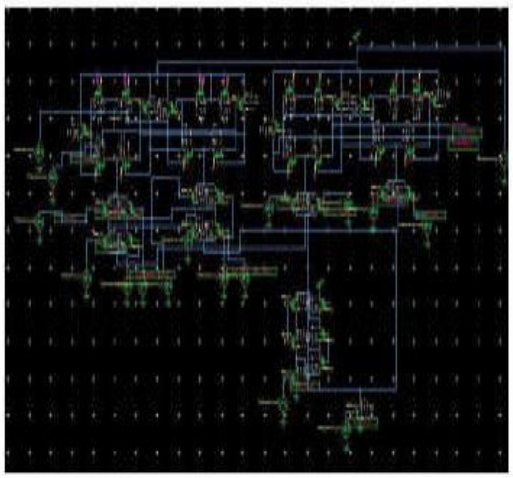


Fig.9. Normal operation of the proposed SRH-MBA circuit

In the write mode (CLK is low), when "Input" is '0', a current flows from Vdd to ground through transistor P2, the MTJs, and transistor N3. On the contrary, when "Input" is '1', the current flows through P3 and N2 in a reverse direction of the prior case. Therefore, based on "Input" to configurations for the MTJs are possible including a case that the upper MTJ is in antiparallel mode and the other in parallel and vice versa. The attached output of designed circuit to the logic tree of the proposed RHMFA circuit, the resulted design will be a non- volatile and rad-hard MFA. The designed circuit can be used in computing applications and power gating structures.

Simulation results and analysis

The below simulation results are showed for the conventional one bit full adder layout of 180 nm technology, proposed full adder of both schematic and layouts, 4-bit carry select adder of both schematic and layouts of 130 nm technology. In general, fault tolerance is achieved at the expense of redundancies that result in energy, performance and area overhead. In this section, we show that, the proposed radhard MFA circuits improving fault tolerance have reasonable design parameters. Comparing the properties of proposed RH-MFA with the state-of-art counter part. As the reported results reveal, our proposed MFA circuits offer a lower energy consumption over the other considered designs as they use fewer MTJs. To investigate the radiation hardening of the proposed MFA circuit, some circuit-level simulations using the TANNER tool have been carried out. The MTJ's used in proposed circuits are inherently robust against radiation effect, in result strike of energetic particles will not change their reconfiguration. Besides, it increases the associated energy or delay of read operation while offering an SEU- tolerant sensing. Our MFA circuits have improved the delay and energy. Besides, our circuits have decreased energy consumption in the pre-approval change or write mode employing fewer reconfigurable MTJ's. Ascan be found from the results, the energy consumed for reconfiguration. Comparing with the considered previous MFA's, our designs incurred a little duration in performance while offered radiation immunity and energy saving.



PROPOSED DESIGN

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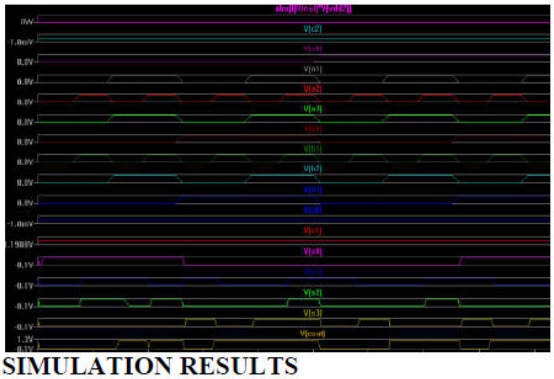

SIMULATION RESULTS

Conclusion

This paper proposed an SEU-tolerant magnetic full-adder (RH-MFA). In comparison with the previous work, the proposed RH-MFA circuit offers a low energy consumption as well as radiation hardening. A serial magnetic adder as well as a full-nonvolatile MFA based on the proposed RH-MFA circuit are also suggested and evaluated. The proposed nonvolatile and rad-hard MFA circuit (NVRH-MFA) can be used for the power gating and reliable architectures. In conclusion, we can claim that the energy consumption and also robustness against radiation effects in magnetic full-adders are improved over the previous work.

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