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A NOVEL AREA-EFFICIENT VLSI ARCHITECTURE FOR TURBO DECODERS IN-VEHICLE SYSTEM

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ABSTRACT: This paper studies design and implementation of the Turbo encoder to be an embedded module in the in-vehicle system (IVS) chip. Field programmable gate array (FPGA) is employed to develop the Turbo encoder module. Both serial and parallel computations for the encoding technique are studied. The two design methods are presented and analysed. Developing the parallel computation method, it is shown that both chip size and processing time are improved. The logic utilization is enhanced by 73% and the processing time is reduced. The Turbo encoder module is designed, simulated, and synthesized using Xilinx tools. Xilinx is employed as an FPGA device to implement the developed module. The Turbo encoder module is designed to be a part of the IVS chip on a single programmable device.

KEY WORDS: Turbo encoder module; field programmable gate array; emergency call; in-vehicle system chip.

I.INTRODUCTION

Inter symbol Interference (lSI) caused by multi-path propagation is a significant problem in digital mobile communication systems. In addition, the channel characteristic is time varying due to the movement of mobile station relative to its surroundings, so channel estimation and equalization have great role for the reliability of the received data. The conventional method is the Maximum Likelihood Sequence Estimation which employs the Viterbi algorithm. Such an approach is sub optimal due to reason that separation of channel estimation and data detection results in performance loss. Turbo equalization was motivated by the breakthrough of Turbo Codes and has emerged as a promising technique for drastic reduction of the inter symbol interference effects in frequency selective wireless channels. Turbo equalization procedure, in its generic form, exhibits the following two traits a) the decoder and the equalizer exchange soft information between each other, with this soft information being interpreted as a-priori probability information, and b) the decoder and the equalizer exchange extrinsic information, which is possible if their output at time instant n does not directly rely on their soft input for the same time index but only on information gained by using the soft information about symbols at adjacent (past and future) time instantsAs there is an increase in dependency in wireless communication, it is necessary to improve the capacity of transmission in date without any errors and

with maximum efficiency. The wireless communication through a channel is more affected by noise, and this leads to errors in the data to be transmitted than in wired communication. For a reliable and efficient transmission of data, various error correction codes are developed. Among them, two main channel codes are Block codes and Convolutional. Block codes are a code which accept a block of k data bits, perform complex operations or finite field arithmetic operation and generates the block of m code bits. It can be represented as (m, k) codes. The k bits in a code word do not depend on the previous information bits in any other code word; it means the block codes are memory less codes. It is good for the small streams of data; it is not for improving the error correction rate and efficiency. Convolutional codes are developed for real-time error correction. Convolutional codes generate one single code word from the entire input bit stream. The encoded bit depends not only on the current bit but additionally on the antecedent bit information. More computational complexity arises as we increase the length of the code word exponentially. Turbo Codes are a class of powerful error correcting codes, introduced and developed in the year 1993, whose performance is very close to the limit as it is compared with other class of error correcting codes. Turbo codes produce high weight codes by using recursive convolutional encoders, useful to distinct the codes easily in the decoding process. Recursive convolutional encoders are most suitable when compared with the non-recursive convolutional encoders. The difference between recursive and non-recursive convolutional is that the recursive encoders have feedback connection whereas no recursive doesn't have.

II. RELATED WORK

Over the years, there has been an increase in the use of digital communication in the field of computer communication, cellular and wireless sensor networks (WSN). In digital communication, error correction codes are an essential component. To ensure the robust and reliable operation of digital communication applications like data encoding, data decoding and data storage systems require error correction. Wireless communications always requires highly reliable data transfer in the presence of data corrupting noise. It requires good error correcting codes. There are various types of forward error correcting (FEC) codes such as block codes, linear codes, convolutional codes and turbo codes. Forward error correction or channel coding is a technique which is used for controlling errors in data transmission over unreliable or noisy communication channels. The main idea is that the sender encodes the message in a redundant way by using an error-correcting code (ECC).Turbo Encoder is a parallel concatenation of Two Recursive Systematic Convolutional (RSC) Encoders and is separated by interleaved. RSC Encoders generates two different codes one is systematic output and the second one is parity bits. But each RSC encoders takes different bit stream as an input. In Each iteration, the equalizer attempts to improve its mitigation of the deleterious effect of the channel induced distortion and noise by using side information or extrinsic symbol

information obtained from the decoders. The equalizer output, in tum, feeds the decoders, which yield a better estimate of the symbols due to the improved input from the equalizer. The process is continued until no further improvement is gained from iteration The first one will take original data as input and second will take interleaved data as input. Interleaving is a process in which bits are rearranged by using the desired algorithm. The Turbo Encoder gives output of 28 bits which is a combination of input data and an output of two RSC encoders which is thrice the length of the input bits. These RSC encoders are identical and generate two codes i.e parity and other is systematic code, i.e. the output contains input bits in it. Turbo Encoder takes m information bits as an input and generates m data bits and m parity bits as an output. The traditional Turbo codes are consist of two RSC Encoders and one interleaved which is used to separate the RSC encoders by appending interleaved input to the every encoder. Interleaver is main component which greatly affects the performance of the Turbo Encoder. The intelaver is designed for generating code words with high weight and to eliminate low weight hamming codes. It shows that interleaving algorithm affects the performance of turbo codes. If the interleaving pattern is more random then the performance improves. Block interleaver or Matrix interleaver is a most popular interleaver used in digital data transmission. When compared with the other interleavers, it is very simple and easy to design and implement. A block interleaver writes data in a matrix row wise from left to right and top to bottom. After all the information bits are writing into a matrix, it reads the data in column wise from top to bottom and left to right. The output of the interleaver is applied to the RSC 2.

III. EXISTED SYSTEM

The European emergency call (eCall) system is a telematics system designed to save more lives in vehicle accidents. It is a governmental mandatory system that is to be implemented by March 2018. The EU eCall system provides an immediate voice and data channel between the vehicles and an emergency centre after car accidents. The data channel provides the emergency centre with the necessary data for emergency aids. The EU eCall system main parts includes the in-vehicle system (IVS), the public safety answering point (PSAP), a cellular communication channel. The IVS activates the data channel automatically when a car accident occurs. The IVS collects the minimum set of data (MSD) that includes GPS coordinates, the VIN number, and all required data for an emergency aid. It sends the MSD to the closest PSAP through a cellular channel in up to 4 seconds. The PSAP sends the emergency team to the location of the accidents. The IVS modem employs multiple modules for the MSD signal processing. The IVS employs a Turbo encoder as a forward error correcting (FEC). The Turbo encoder implements the digital data encoding technique in data transmissions. Turbo coding is one of the most popular and efficient coding technique to improve bit error rate (BER) in digital communications. The cyclic redundancy check (CRC), the modulator, the demodulator-decoder modules are

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projected and implemented on an FPGA device. They are developed to be embedded modules of the IVS chip this work studies the hardware development of the Turbo encoder. It employs FPGA technologies to develop the Turbo encoder to be an embedded module in the IVS modem. It discusses serial and parallel computation techniques for the Turbo encoder. It does not only design and implement the Turbo encoder module, but also proposes a better solution for the turbo encoder implementation. The improvement of the chip size and processing time are exhibited by developing the parallel computation technique for the Turbo encoder. The turbo encoder technique is one of the most powerful FEC techniques in digital communication. It employs a Turbo encoder module with 1=3 code rate. The Turbo encoder functionalities are detailed in the third generation partnership project (3GPP) standards. The input signal of the turbo encodes is the MSD data appended with the CRC parity bits in binary. The block length of the MSD data is 1148 bits. The output of the module is the MSD encoded data in binary. Implementing the turbo coding technique with 1=3 coding rate and thrills bits, the length of the output is 3456 bits.The thrill Structure has an impact of the Turbo encoder. The Turbo encoder employs a parallel concatenated convolutional code (PCCC). The PCCC uses two constituent encoders with eight states. The initial status of the register is zeros. The first constituent takes the MSD bits and implements the employed convolutional 978-1-5386-4649-6/18/$31.00 c 2018 IEEE technique. It takes one bit at a time and generates one bit of parity1 bits. The second constituent implements an identical technique of the first constituent, but it calls for the MSD bit after they are interleaved with a 3GPP designed interleaved technique. The length of the input data, parity1, and parity2 are 1148 bits. There are 12 bits of the tail bits. They are driven from The shift register feedback. The tail bits are applied for end points between the encoded data blocks. The output structure of the Turbo encoder is illustrated in Figure 1.

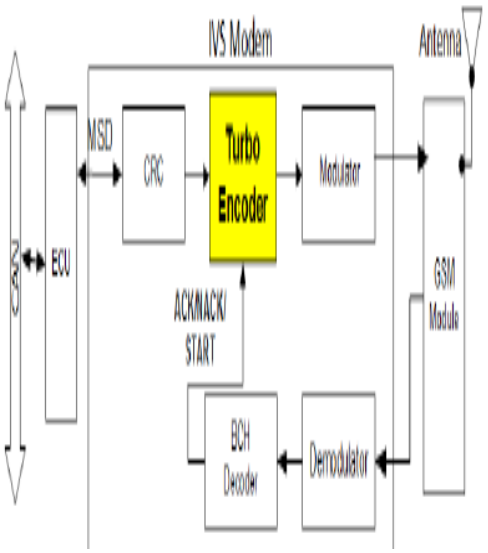

FIG. 1: EXISTED SYSTEM

IV. PROPOSED SYSTEM

The RSC codes introduced in the previous section are generally considered most suitable for application in low SNR environments, where they outperform a non-systematic convolutional (NSC) code that has comparable memory. At higher SNRs, the NSC code will generally provide a lower bit error rate (BER) than the RSC code4. In 1993, Berrou and his colleagues described a new class of error-correcting code that used RSC encoders, but could achieve better performance than

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NSC codes at any SNR. In fact, one example code in this class could come within 0.7 dB of the Shannon limit for a BER of 10-5. This innovation was dubbed turbo coding. A turbo encoder uses parallel concatenation of multiple RSC encoders with pseudorandom Interleaves preceding all but one of the constituent encoders. Although touts turbo codes as a new class of convolutional codes, they can also be considered to be block codes. The data to be transmitted is partitioned into blocks so that the interleaves can perform their operation.Parallel concatenation means that multiple encoders are acting on the same data stream, and the outputs of the encoders are concatenated to form the overall encoder output. The code is then decoded by several corresponding decoders in the receiver. This is in contrast to serial concatenation, which is a technique whereby data is encoded in multiple encoders in a serial fashion in order to take advantages of properties of each code. This is shown in where the data is first encoded by an outer encoder whose output is then encoded by an inner encoder. After demodulation, the inner decoding is performed first, followed by the outer decoding to produce the overall. Estimate of the transmitted message. One such arrangement, has a Reed-Solomon (RS) block code as the outer code and a convolutional code as the inner code to take Advantage of the performance at low SNR of the convolutional code and the tolerance of burst errors of the RS code

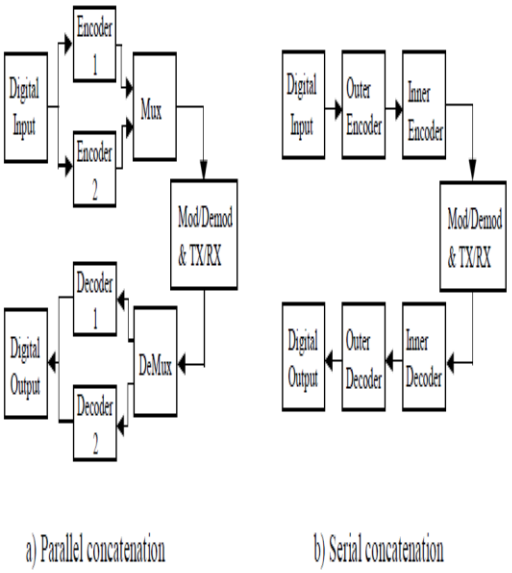

FIG. 2: PROPOSED SYSTEM

In many cases, although it is not shown in Figure 2, the multiple decoders share information in order to obtain the best estimates of the transmitted data. Interleaves can be used to help the code combat burst errors by spreading out bit information over a larger block of data. With no interleaving, convolutional codes are quite susceptible to burst errors since the *K* output bits that contain information from a single data bit are adjacent in the encoder output stream. By interleaving the data stream before transmission and interleaving it after it is received, the burst errors appear to the decoder to be random. The most common type of interleaver is a block interleaver, which is a rectangular array where data is read into the columns and out of the rows (or vice versa). This type of interleaving is referred to as channel interleaving. The interleavers used in turbo coding are not channel interleavers. Referred to as code interleavers, they arrange the data block in a row and then rearrange the rows

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according to a pseudo-random pattern. While this technique also has the effect of spreading out the data bits to protect against burst errors, the more important effect is the reduction of the probability of having all of the encoders produce low Hamming weight code words at the same time. In a turbo encoder with Ne constituent encoders, the encoder output contains a single systematic output and Ne parity outputs from the RSC encoders (assuming no puncturing), Ne – 1 of which operate on an interleaved version of original data block. Thus, the output of the turbo encoder can be viewed as the output of Ne independent RSC encoders, except the systematic information only need be transmitted for one of the encoders.The decoder can reconstruct the systematic bits for the other encoders because it knows the interleaving patterns that were used. Thus, the decoder can be decomposed into Ne convolutional decoders with each one operating on the output of a single constituent encoder. In order to get the best possible estimate of the original message, these separate decoders must be able to share the results of their calculations. To accomplish this, turbo decoders use iterative feedback decoding.

V. RESULTS

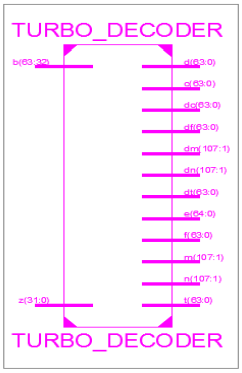

FIG.3. RTL SCHEMATIC

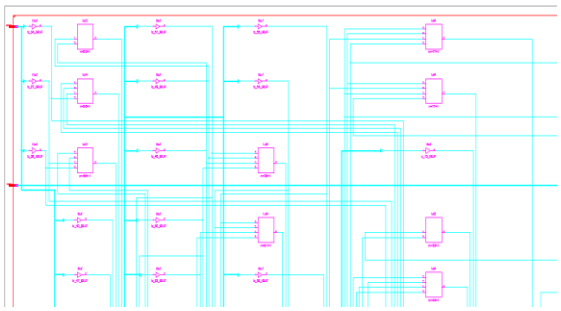

FIG.4. TECHNOLOGY SCHEMATIC

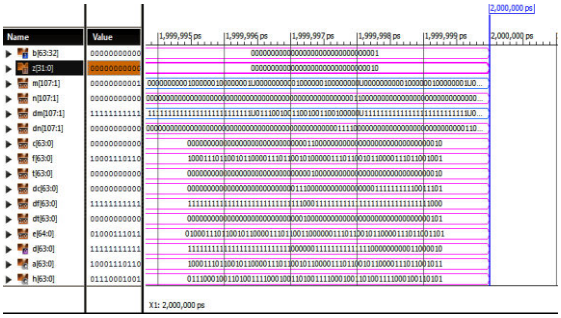

FIG.5. OUTPUT WAVEFORM

D Project Status (12/01/2018 - 12:20:59)			
Project File:	ET34.xise	**Parser Errors:**	X 4 Errors
Module Name:	TURBO_DECODER	**Implementation State:**	Synthesized
Target Device:	xc3s100e-5vq100	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	9 Warnings (9 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	297	960	30%
Number of 4 input LUTs	556	1920	28%
Number of bonded IOBs	999	66	1513%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat 1. Dec 12:20:57 2018	0	9 Warnings (9 new)	0
Translation Report					
Map Report					

FIG. 6: REPORT

VI. CONCLUSION

In this brief, by investigating the relation between the recursion computations, a novel method has been proposed, which is called MSR. The proposed method is applied to the previous ACS architectures then achieves an area-efficient architecture for recursive computations. The proposed architectures achieve, at most reduction in complexity, which notably reduces the complexity of the whole MAP core of the turbo decoder. Furthermore, the proposed

method can be also used for higher radix designs to reduce complexity.

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