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SIMULATION OF CURRENT SOURCE MODULAR MULTILEVEL CONVERTER FOR FUZZY CONTROLLER BASED STATCOM APPLICATION

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ABSTRACT- In this paper a multilevel current source converters is utilized for the high power applications with high current low and voltage requirements. Therefore we can totally analysis of a current source modular multilevel converter (CSMMC) with its application such as STATCOM. Fuzzy control is employed to the system for deduction of THD. There are different properties of CSMMC which are correlated with the voltage source modular multilevel converter (VSMMC). There are two method for inductor current balancing they are sub module inductance selection method and a sorting based algorithm which are proposed for CSMMC. Moreover for the switching technique we are implementing the carrier phase shifted sinusoidal pulse width modulation. Here the performance of a converter can be analyzed under non-interleaved and interleaved carrier signals during the upper and lower arms. Here we are using the fuzzy controller compared to other controllers i.e. The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. The proposed STATCOM will display that the transient and steady state performance of the system are satisfactory. By using the simulation results we can analyze the proposed method.

Index Terms—Current balancing, current source modular multilevel converter (CSMMC), Fuzzy logic controller, HVDC transmission, STATCOM.

(I) INTRODUCTION

This paper presents a new control scheme to control a transform less STA–TCOM topology based on multilevel converter (MC) in order to manage more accurate compensation for high-power applications. The main objective of this paper is to analyzed in detail the operation of a CSMMC, a dual of VSMMC, and to investigate its feasibility as a STATCOM. In CSMMC, a variable current source in each converter arm is created using parallel connected inductor SMs. Voltage source modular multilevel converters are used for high power applications. Main features of the VSMMCs include reduced harmonics, lower switching frequency, and reduced stress on each device, amongst others [1]. By using this technique besides minimizing the harmonic level, the inverter unit fundamental output voltages are equalized. Moreover, because of modular structure, scalability to various power and voltage levels is easily achieved and reliability can be improved by

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including redundant sub modules in each phase [2]. These features make the VSMMCs more attractive and competitive for HVDC and FACTS applications [3].In this paper, detail theoretical analysis of CSMMC is presented and various parameters of the converter are correlated with VSMMC. SM inductance selection method and SM inductor current ++balancing strategy are presented for CSMMC. Furthermore, equations are developed in dq frame to design a controller for CSMMC based STATCOM. The CSCs using fully controllable switches have many advantages than LCCs. The main features of CSCs using self-commutating devices are: 1) independent control of the active and reactive power, 2) it can be operated in weak grids or with passive loads, and 3) relatively small footprint because the ac side filters can be eliminated due to low harmonic distortion [10].An MMC topology using a modified current source H-bridge cell is proposed, to address the voltage scaling problem. Dynamic performances of the STATCOM during step change in capacitive mode to inductive mode and vice versa, and during ac and dc faults are evaluated.

2. CSMMC STRUCTURE AND OPERATION

Fig. 1 shows one phase of a three phase CSMMC. Each phase of a converter consists of two arms and each arm consists of N parallel connected half bridge SMs and the arm capacitor. The inductors of the SMs act as current sources that can be inserted or bypassed in each arm of the CSMMC. This way the ac output current can be controlled by varying the number of inserted SMs in the upper and lower arms by using appropriate modulation technique. The inductor currents of all SMs are kept balanced by using a balancing technique as explained in Sec. III-B. The arm capacitor, Carm, is dual to the arm inductance of a VSMMC. Carm is considered to be identical for all arms of the converter. The main functions of the arm capacitor are to absorb any unbalances and harmonics generated in the arm currents [22].

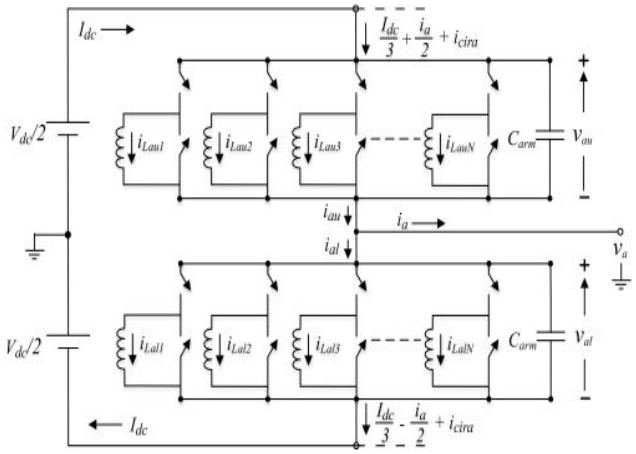

Fig 1. Configuration of phase-a of a three phase CSMMC.

A. SM Structure and Operation

A half bridge SM of a VSMMC is shown in Fig 2(a). This is the basic building block of a VSMMC which consists of two bidirectional switches and a capacitor. The corresponding dual, a half bridge inductor SM for a CSMMC is shown in Fig 2(b). The controlled bidirectional switches and a capacitor are replaced with controlled reverse voltage blocking switches and an inductor respectively. In Fig 2(b), two switches S1 and S2 are complimentary and their switching states are decided by using appropriate modulation technique to get the desired output current from the SM. In Fig 2(c), S1 is ON (S2 is OFF), hence, the SM is inserted in the arm and the output current of the SM is effectively the inductor current. In Fig 2(d), S1 is OFF (S2 is ON), hence, the SM is bypassed and the output current of the SM is zero.

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Nevertheless, the inductor current remains continuous through switch S2. Hence the output current of the converter can be controlled by inserting or bypassing the SMs connected in parallel.

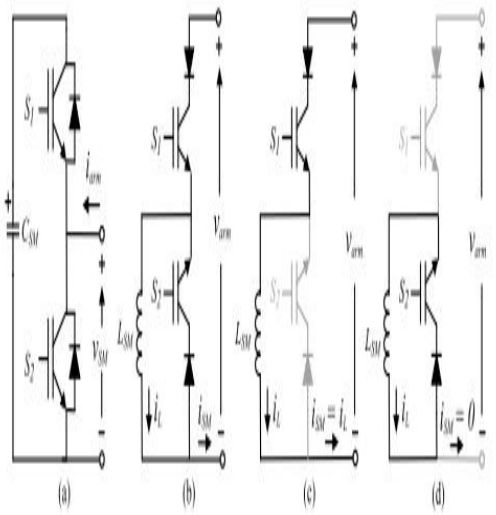

Fig 2. (a) Half bridge capacitor SM (b) Half bridge inductor SM (c) SM inserted (d) SM bypassed

In an SM shown in Fig 2(b), a current path for the inductor should be provided to protect the converter against the over-voltage caused by open circuit faults. Fig 3 shows the configuration of an SM with open circuit protection using a bypass switch T1 and a thyristor T2 [22]. In normal operation, switch T1 is closed and thyristor T2 is turned-off as shown in Fig 3(a). When the fault is detected in the SM, thyristor T2 is turned-on and switch T1 is opened to bypass the faulty SM from the system as shown in Fig 3(b). The SM inductor current remains continuous through thyristor T2 and thus protects the SM from possible damage. Simultaneously, if the redundant SM is available then the switch T1 of a redundant SM is closed to replace the faulty SM with a redundant SM.

Hence, continuous operation of the CSMMC is ensured with increased safety and availability.

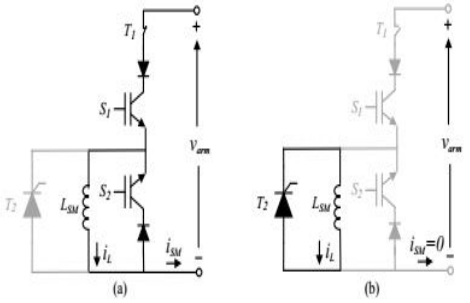

Fig Sub module open-circuit protection using thyristor (a) normal operation (b) operation during fault.

B. Assumptions

In order to simplify the mathematical analysis, some assumptions are made. These assumptions are as follows:

1) Only fundamental frequency component in the ac output waveforms is considered. This is a reasonable assumption because the number of levels in the output or the switching frequency is generally high. It will considerably simplify the analysis as well [25].

2) It is assumed that the SM inductor currents are balanced at all times to ensure stable operation of the CSMMC. This can be guaranteed by the control scheme presented in Sec. III-B, and subsequently demonstrated in Sec. V.

3) For circulating current analysis, only 2nd harmonic component is considered. Aside from the 2nd harmonic component, there may be other harmonics in the circulating current. However, these harmonics have a negligible impact on the accuracy of the analytical results because their amplitude is very small. This is verified using the simulation results shown in Sec. V-A.

4) For simplicity, balanced grid voltages have been assumed and hence only positive sequence components of the three phase voltages and currents are considered. Under unbalanced grid conditions, not only the positive sequence components,

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but also the negative sequence components are taken into considerations [26].

C. Analysis and Operation of CSMMC

To analyse the operation of a converter, phase-a of a three phase CSMMC, shown in Fig 1, is considered. If the upper switch in an SM is ON, the output of the SM is equal to the corresponding inductor current; otherwise, it is zero. Hence, each arm of the CSMMC represents a controllable current source and the desired output current is obtained by varying the number of inserted and bypassed SMs in each arm. The ac output current ia and phase voltage va are defined as

$$i_a = \hat{I}_a \sin\omega_0 t, \quad v_a = \hat{V}_a \sin(\omega_0 t + \phi).$$

Here, Iˆa and Vˆa are the peak values of the output current and voltage respectively, ω0 is the fundamental frequency and ϕ is the load phase angle. The effective inductances of upper and lower arms of phase-a, are given by

$$L_{au} = L_{SM}/N_{au}, \quad L_{al} = L_{SM}/N_{al}.$$

Here, Nau and Nal are the number of SMs inserted in upper and lower arms respectively and LSM is the SM inductance. Using KCL, the total output currents of upper and lower arm SMs of phase-a in Fig 1 can be expressed by

$$i_{Lau} = \sum_{j=1}^{N_{au}} i_{Lauj}, \quad i_{Lal} = \sum_{j=1}^{N_{al}} i_{Lalj}.$$

Note that iLauj, j = 1, .., Nau and iLalj, j = 1, .., Nal, are the currents of inserted SMs in upper and lower arm respectively. Using (3), the upper and lower arm currents iau and ial in Fig 1 are defined by

$$i_{au} = C_{arm}\frac{dv_{au}}{dt} + i_{Lau}, \quad i_{al} = C_{arm}\frac{dv_{al}}{dt} + i_{Lal}$$

where, vau and val are the upper and lower arm voltages respectively. The arm currents, iau and ial, consists of three components: 1) the dc current, Idc/3, which is responsible to keep the arm energized or to maintain the SM inductor currents around their reference value; 2) half of the ac side current; and 3) the circulating currents which circulate within the three phases of the converter. Hence, iau and ial can also be written as

$$i_{au} = \frac{I_{dc}}{3} + \frac{i_a}{2} + i_{cira}, \quad i_{al} = \frac{I_{dc}}{3} - \frac{i_a}{2} + i_{cira}$$

(5)

where icira is the circulating current in phase-a. Depending upon the switching technique, the circulating current contains any number of harmonic components. Therefore, in steady state, icira can be given by the general expression

$$i_{cira} = \sum_{n=1}^{\infty} i_{ciran} \sin(n\omega_0 t + \phi_n).$$

(6)

If the circulating currents, icirp, p = a, b, c, of the three phases have equal magnitude and phase difference of 2π/3, then,

$$i_{cira} + i_{cirb} + i_{circ} = 0.$$

(7)

Therefore, the circulating currents have no effect outside the converter either on the ac or dc side. However, they have a significant impact on the rating of converter components and the losses of the converter. Hence, they should be kept as close to zero as possible. The ac side current of phase-a can be obtained by subtracting (5b) from (5a), that is

$$i_a = i_{au} - i_{al}.$$

(8)

Using KVL, the ac voltage of phase-*a* in Fig 1 is defined by

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$$v_a = -v_{au} + V_{dc}/2 \quad (9)$$

$$v_a = v_{al} - V_{dc}/2 \quad (10)$$

$$v_a = (v_{al} - v_{au})/2. \quad (11)$$

The dc link voltage is then derived from (9) and (10)

$$V_{dc} = v_{au} + v_{al}. \quad (12)$$

Using (5a) or (5b) for all the three phases, the total dc link current in terms of I pu or ipl, p = a, b, c is expressed as

$$I_{dc} = i_{au} + i_{bu} + i_{cu} \quad \text{or} \quad I_{dc} = i_{al} + i_{bl} + i_{cl}. \quad (13)$$

$$i_a = C_{arm}\frac{d}{dt}(v_{au} - v_{al}) + i_{Lau} - i_{Lal}. \quad (14)$$

Inserting (11) in (14) gives

$$i_a = -2C_{arm}\frac{dv_a}{dt} + i_{Lau} - i_{Lal}. \quad (15)$$

It is clear from (15) that iLau and iLal should be controlled to get the desired output current. To specify the reference currents iLau and iLal, the harmonic and circulating currents are ignored. Hence, using (1a) and (4)-(5), the reference currents of the upper and lower arms of phase-a in time domain are expressed as

$$i_{Lau} = \frac{I_{dc}}{3} + \frac{\hat{I}_a}{2}sin\omega_0 t = \frac{I_{dc}}{3}[1 + m_i sin\omega_0 t] \quad (16)$$

$$i_{Lal} = \frac{I_{dc}}{3} - \frac{\hat{I}_a}{2}sin\omega_0 t = \frac{I_{dc}}{3}[1 - m_i sin\omega_0 t] \quad (17)$$

where mi is the modulation index, defined by $m_i = \frac{3\hat{I}_a}{2I_{dc}}$.

Similarly, substituting (1b) in (9) and (10), the voltages in each arm of phase-a in time domain are given by

$$v_{au} = \frac{V_{dc}}{2}[1 - m_v sin(\omega_0 t + \phi)] \quad (18)$$

$$v_{al} = \frac{V_{dc}}{2}[1 + m_v sin(\omega_0 t + \phi)] \quad (19)$$

Using (16) to (19), the instantaneous power delivered to the upper and lower arms of phase-a of the converter are derived as

$$p_{au} = v_{au} \times i_{Lau} = \frac{V_{dc}I_{dc}}{6}[1 + m_i sin\omega_0 t - m_v sin(\omega_0 t + \phi) - \frac{m_i m_v}{2}(cos\phi - cos(2\omega_0 t + \phi))] \quad (20)$$

$$p_{al} = v_{al} \times i_{Lal} = \frac{V_{dc}I_{dc}}{6}[1 - m_i sin\omega_0 t + m_v sin(\omega_0 t + \phi) - \frac{m_i m_v}{2}(cos\phi - cos(2\omega_0 t + \phi))]. \quad (21)$$

The internal energy of phase-a can be calculated by summing and integrating (20) and (21), that is,

$$E_a = \frac{V_{dc}I_{dc}}{6}[2t - m_i m_v cos\phi t + \frac{m_i m_v}{2\omega_0}(sin(2\omega_0 t + \phi))]. \quad (22)$$

In steady state, if the losses in the converter are neglected hen the dc component of the energy should not appear in the arms. Otherwise the energy in the SM inductors will increase or decrease continuously. Hence,

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$$2t - m_i m_v cos\phi t = 0 \quad \text{or} \quad m_i m_v = 2/cos\phi. \tag{23}$$

from (23) in (22), one get the alternating energy in the converter phase

$$E_a = \frac{V_{dc} I_{dc}}{6\omega_0 cos\phi} sin(2\omega_0 t + \phi). \tag{24}$$

Eq. (24) shows that the energy in the converter arms fluctuates at twice the fundamental frequency. This is in line with the2nd harmonic current in circulating current of VSMMC [27].

D. Circulating Current Analysis

The arm current of the CSMMC is coupled to the dc side of the SM by the switching actions, thereby generating ripple current in the SM inductor. This ripple current is reflected to the SM output terminal. The sum of the ripple component of all the SMs within one phase forms the circulating current.

Hence, the circulating current component in the arm current is influenced by the inductor ripple current. Since the size of the SM inductor is appropriately selected to limit the ripple current as explained in Sec. II-E, the circulating current is also limited. On the other hand, in VSMMC, the circulating current is caused due to the sum of ripple voltages of all the SMs within one phase [25]. This circulating current is limited by the arm inductors. However, the value of arm inductors should not be very large, and hence an additional control effort for

limiting the circulating current is required in VSMMC [27]. As shown in (24), the energy in the converter arms fluctuate sat twice the fundamental frequency and therefore, the most significant component in the circulating current will be the 2nd harmonic. To solve for the amplitude and phase of thisn2nd harmonic circulating current, the early assumptions of thenarm currents in (16)-(17) are revised and the 2nd harmonicncirculating component is supposed to exist in the arm currents. That is,

$$i_{au} = \frac{I_{dc}}{3} + \frac{\hat{I}_a}{2} sin\omega_0 t + \hat{I}_{2f} sin(2\omega_0 t + \phi_2) \tag{25}$$

$$i_{al} = \frac{I_{dc}}{3} - \frac{\hat{I}_a}{2} sin\omega_0 t + \hat{I}_{2f} sin(2\omega_0 t + \phi_2) \tag{26}$$

Where, I^2f and ϕ2 denote the amplitude and phase of the 2nd harmonic circulating current. Using (18)-(19) and (25)-(26), the expressions for the revised instantaneous power delivered to the upper and lower arms of phase-a are derived as

$$p'_{au} = p_{au} + \frac{\hat{I}_{2f} V_{dc}}{2} sin(2\omega_0 t + \phi_2)[1 - m_v sin(\omega_0 t + \phi)] \tag{27}$$

$$p'_{al} = p_{al} + \frac{\hat{I}_{2f} V_{dc}}{2} sin(2\omega_0 t + \phi_2)[1 + m_v sin(\omega_0 t + \phi)]. \tag{28}$$

The alternating energy in phase-a is then obtained by summing and integrating (27) and (28), and inserting (23). That is,

$$E_a = \frac{V_{dc} I_{dc}}{6\omega_0 cos\phi} sin(2\omega_0 t + \phi) - \frac{V_{dc} \hat{I}_{2f}}{2\omega_0} cos(2\omega_0 t + \phi_2) \tag{29}$$

If the upper and lower arms of CSMMC with N SMs per arm, are controlled such that at any instant Nau + Nal = N, and the SM inductor currents are balanced, then the average SM inductor current iL is expressed as

$$i_L = (i_{au} + i_{al})/N. \tag{30}$$

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average SM Since, N SMs are inserted in a phase at any instant, the total energy ELa in phase-a is given by

$$E_{La} = N\frac{1}{2}L_{SM}\,i_L^2 = \frac{2I_{dc}L_{SM}I_{dc}^2}{9N} + \frac{4L_{SM}I_{dc}\hat{I}_{2f}}{3N}sin(2\omega_0 t+\phi_2)+ \frac{2L_{SM}\hat{I}_{2f}^2}{N}sin^2(2\omega_0 t+\phi_2). \quad (32)$$

Comparing 2nd harmonic component in (29) and (32) gives

$$\frac{V_{dc}I_{dc}}{6\omega_0 cos\phi}sin(2\omega_0 t+\phi) - \frac{V_{dc}\hat{I}_{2f}}{2\omega_0}cos(2\omega_0 t+\phi_2) = \frac{4L_{SM}I_{dc}\hat{I}_{2f}}{3N}sin(2\omega_0 t+\phi_2). \quad (33)$$

By solving (33), the amplitude I^2f and the phase ϕ2 for the 2nd harmonic circulating current are obtained as

$$\hat{I}_{2f} = \frac{NV_{dc}I_{dc}}{cos\phi\sqrt{(8\omega_0 L_{SM}I_{dc})^2+(3NV_{dc})^2}} \quad (34)$$

$$\phi_2 = \phi - arctan(3NV_{dc}, 8\omega_0 L_{SM}I_{dc}). \quad (35)$$

Eq. (34) shows that under given operating condition, the 2nd harmonic circulating current is limited by the SM inductor, which is verified using the study results shown in Sec. V-A.

E. SM Inductance Selection

The stored energy EL in an inductor of each SM of CSMMC changes with time because the energy in the arm is fluctuating as shown by (24). This results in the current ripples in SM inductors. The current ripple in SM inductors depends on the size of the SM inductor LSM and the energy power ratio E(S). Here, E(S) signifies the energy storage requirements in the converter in terms of total energy storage per transferred MVA [28]. Since, E(S) is independent of the specific energy storage device [29], it can be assumed to be same as that used for SM capacitance selection for VSMMC. Typically E(S) is in the range of 10 kJ/MVA to 50 kJ/MVA depending upon the converter application [4]. The stored energy, EL, in an SM inductor is expressed as

$$E_L = \frac{1}{2}L_{SM}\,i_L^2. \quad (36)$$

Using (36), the total stored energy E in six arms of a three phase CSMMC with rated power S is obtained by

$$E = 6\,N\,E_L \quad (37)$$

$$S\,E(S) = 6\,N\,\frac{1}{2}L_{SM}\,i_L^2. \quad (38)$$

The SM inductance LSM is then calculated as follows:

$$L_{SM} = \frac{S\,E(S)}{3\,N\,i_L^2}. \quad (39)$$

Equation (39) confirms the duality in selection of SM inductance with that of SM capacitance selection given in [5]. Alternatively, LSM can also be derived as a function of inductor current ripple by considering the energy variation in the arm. Multiplying (36) with the number of SMs in an arm gives the stored energy in each arm. That is,

$$E_{arm} = \frac{1}{2}NL_{SM}\,i_L^2. \quad (40)$$

The current in each SM will vary with time as the inductors are charged and discharged. Consequently, the energy variation in each arm can be expressed as

$$E_{arm} + \frac{\Delta E}{2} = \frac{1}{2}\,N\,L_{SM}\,(i_L(1+\Delta i_L))^2 \quad (41)$$

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$$E_{arm} - \frac{\Delta E}{2} = \frac{1}{2} N L_{SM} (i_L(1 - \Delta i_L))^2. \quad (42)$$

where, ΔE represents the peak to peak energy variation in the arm and ΔiL is the per unit current ripple in SM inductor for any given operating point. The inductance of the SM inductors can then be calculated by subtracting (42) from (41) and solving for LSM . Accordingly,

$$L_{SM} = \frac{\Delta E}{2 N i_L^2 \Delta i_L}. \quad (43)$$

Equation (43) also confirms the duality in selection of SM inductance with that of SM capacitance selection given in [30].

3 CSMMC CONTROL

In CSMMC multiple SMs are connected in parallel in each arm. Hence to get the desired output current, it is required to insert or bypass a certain number of SMs in each arm at any point of time and the current through all the SMs should be balanced. This is done by using appropriate switching and balancing technique as explained below.

A. Switching Technique

To synthesize a multi-level output current waveform at the ac side of the CSMMC, the carrier phase shifted sinusoidal pulse width modulation (CPS-SPWM) scheme is used here. CPS-SPWM is most commonly used modulation strategy for modular multilevel converters as it has some distinctive features. The main feature of the CPS-SPWM is that the power handled by each SM of the same arm is evenly distributed [6]. Hence, using CPS-SPWM the inductor current balancing control can be easily achieved in CSMMC. The SM is inserted or bypassed based on the switching state produced from the intersection of sinusoidal modulating signal and triangular carrier signal. Moreover, two options exists with CPS-SPWM:

1) non-interleaved switching; and 2) interleaved switching [7]. In non-interleaved switching, converter with N SMs per arm requires N triangular carriers with a switching frequency of fsw, while each triangular carrier have phase difference of 2π/N. The triangular carriers for upper and lower arms of converter are same. The reference signals of upper and lower arms are phase shifted by π radians.

On the other hand, in interleaved switching, converter with N SMs per arm requires 2N triangular carriers with a switching frequency of fsw, while each triangular carrier have phase difference of π/N. Hence, the number of carrier signals required are twice the number of SMs per arm. However, the phase difference between two consecutive triangular carriers of the same arm will be 2π/N.

B. Inductor Current Balancing

In ideal condition, the current through each SM inductor of a CSMMC is given by (31). However, due to different electrical parameters of the SMs, the current through the SM inductors tend to be out of balance. Hence, a sorting based algorithm is proposed here for SM inductor current balancing in a CSMMC. Balancing of inductor currents in CSMMC is analogous to the balancing of capacitor voltages in VSMMC. The modulation technique, as described in Sec. IIIA, determines the number of SMs to be inserted or bypassed in the upper and lower arms of the converter. In order to keep the inductor currents balanced, a sorting based rule for inserting or bypassing of each SM is followed. The objective of the sorting strategy is to charge or discharge the

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correct SM inductor.This is possible because the output current levels generated in CSMMC depends upon the number of SMs inserted in upper and lower arms and not by the specific order the SMs are inserted. Table I describes one of the possible switching states with non-interleaved switching for each current level in phasea of three phase five level CSMMC. A block diagram of the SM inductor current balancing algorithm in a CSMMC for phase-a is shown in Fig 4.

The number of SMs to be inserted in upper and lower arms of phase-a are determined by the comparison of the sinusoidal modulating signals and triangular carrier signals, as shown in Fig 4. For the specified number of SMs to be inserted or bypassed, there are several combinations of SMs. The selection of the proper combination is done based on the values of SM inductor currents as well as the polarity of arm voltage. When the SM is inserted, the inductor current increases (decreases) if the voltage across SM is positive (negative). This fact is used for the SM inductor current balancing. The switching signals generated from this algorithm are given to the CSMMC.

Moreover, as can be observed in the diagram of Fig 4, sorting is done only when the SM is to be inserted or bypassed to reduce the switching losses

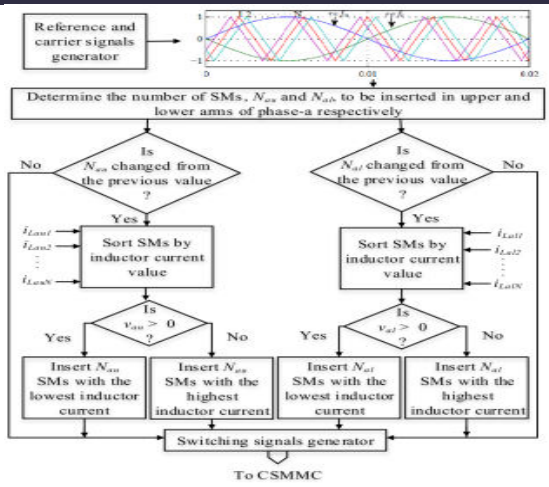

Fig 4. Block diagram of the indicator current balancing algorithm including CPS-SPWM for phase-a of a three phase CSMMC.

4 CSMMC BASED STATCOM

The circuit configuration of a CSMMC based STATCOM is shown in Fig 5. The STATCOM is connected to the grid through a coupling transformer. In Fig 5, iLau and iLal represent controllable current sources, whose instantaneous value depends on the number of inserted and bypassed SMs

TABLE I
ONE OF THE POSSIBLE SWITCHING STATES FOR EACH CURRENT LEVEL IN
PHASE-a OF A THREE PHASE FIVE LEVEL CSMMC

SM_{au1}	SM_{au2}	SM_{au3}	SM_{au4}	i_{au}	i_{al}	i_a
1	1	1	1	$2I_{dc}/3$	0	$2I_{dc}/3$
1	1	1	0	$I_{dc}/2$	$I_{dc}/6$	$I_{dc}/3$
1	1	0	0	$I_{dc}/3$	$I_{dc}/3$	0
1	0	0	0	$I_{dc}/6$	$I_{dc}/2$	$-I_{dc}/3$
0	0	0	0	0	$2I_{dc}/3$	$-2I_{dc}/3$

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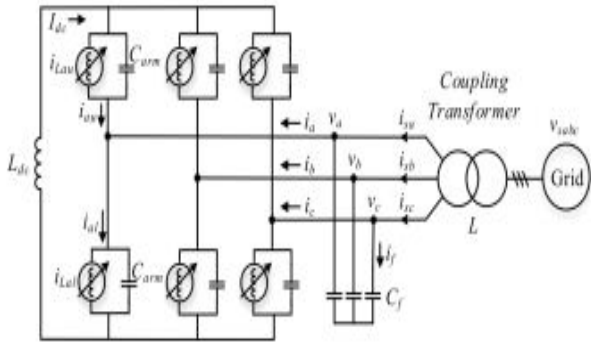

Fig 5. Configuration of CSMMC based STATCOM

In each arm. Cf is the capacitance of the harmonic filter. Ldc is the dc link reactor used to reduce the dc current ripple.

A. Controller Design

The control objectives for the system of Fig 5 are to provide the required reactive power compensation Qref to the grid and to regulate the dc-link current Idc. The controller is implemented based on current mode control in synchronous dq frame as shown in Fig 6. In this approach, the CSMMC line current is regulated by the inner current control loop. The reactive power and dc link current are controlled by the outer current control loop

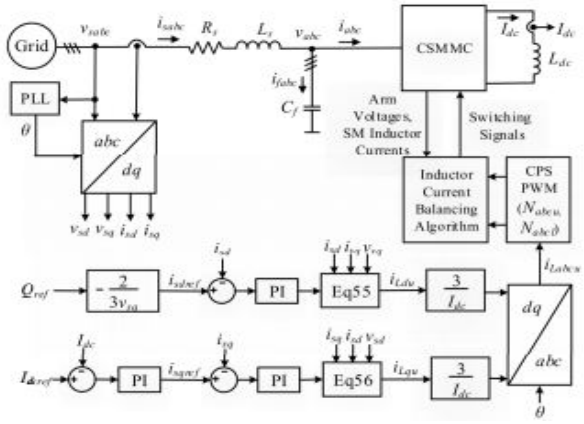

Fig 6. Diagram of CSMMC based STATCOM control system

The dynamic equations of phase-a in abc frame for the system of Fig 6 are expressed as

$$i_a = 2C_{arm}\frac{dv_a}{dt} - i_{Lau} + i_{Lal} \tag{44}$$

$$i_{sa} = i_a + C_f\frac{dv_a}{dt} \tag{45}$$

$$v_{sa} = v_a + R_s i_{sa} + L_s\frac{di_{sa}}{dt}. \tag{46}$$

Here, (44) is obtained using (15) by considering the direction of the current as shown in Fig 6. Note that Ls and Rs in (46) represent the leakage inductance and resistance of the coupling transformer. These equations are valid for all the three phases. In (44), either the upper or lower arm current is selected to be the output of the controller because the upper and lower arm currents are phase shifted by π radians. Solving (16), (17) and (44), the converter line current in terms of the upper arm current is expressed as

$$i_a = 2C_{arm}\frac{dv_a}{dt} - 2i_{Lau} + \frac{2I_{dc}}{3}. \tag{47}$$

Eqs. (45), (46) and (47) are transformed to the synchronous dq frame using the transformation T given by

$$T = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \tag{48}$$

Here, the d-axis is aligned to the grid voltage vector such that the d-axis component of grid voltage vsd = 0. The phase locked loop (PLL) is used to detect the phase θ of the grid voltage. For simplicity, a balanced grid voltage is assumed; hence the zero-sequence component is zero. Thus, the dq transformation of (47), (45) and (46) results in

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$$i_d = 2C_{arm}\frac{dv_d}{dt} + 2\omega C_{arm}v_q - 2i_{Ldu} \quad (49)$$

$$i_q = 2C_{arm}\frac{dv_q}{dt} - 2\omega C_{arm}v_d - 2i_{Lqu} \quad (50)$$

$$i_{sd} = i_d + C_f\frac{dv_d}{dt} + \omega C_f v_q \quad (51)$$

$$i_{sq} = i_q + C_f\frac{dv_q}{dt} - \omega C_f v_d \quad (52)$$

$$v_{sd} = R_s i_{sd} + L_s\frac{di_{sd}}{dt} + \omega L_s i_{sq} + v_d \quad (53)$$

$$v_{sq} = R_s i_{sq} + L_s\frac{di_{sq}}{dt} - \omega L_s i_{sd} + v_q. \quad (54)$$

In steady state, all derivatives can be set to zero. Thus, solving (49)-(54) and using the output of the inner P I controllers, dq components of the upper arm reference current iLdu and iLqu in steady state are determined as

$$i_{Ldu} = PI(i_{sdref} - i_{sd}) - \frac{1}{2}((1-\omega^2 L_s(C_f + 2C_{a}$$
$$\omega(C_f + 2C_{arm})v_{sq} + \omega(C_f + 2C_{arm})R_s i_{sq}$$

(55)

$$i_{Lqu} = PI(i_{sqref} - i_{sq}) - \frac{1}{2}((1-\omega^2 L_s(C_f + 2C_{a}$$
$$\omega(C_f + 2C_{arm})v_{sd} - \omega(C_f + 2C_{arm})R_s i_{s}$$

(56)

Note that the reference current isdref is generated based on commanded reactive power Qref in outer control loop.

With the aligned synchronous frame, d-axis component of grid voltage vsd = 0. Therefore, the reactive power output to the grid can be expressed as follows:

$$Q_{ref} = -\frac{3}{2}v_{sq}i_{sdref}. \quad (57)$$

To obtain isqref , the dc current controller is employed as shown in Fig 6. Finally, the reference arm currents iLdu and iLqu obtained from (55) and (56) are normalized within the range [−1, 1], and transformed back to the abc frame to get the upper arm reference currents iLpu, p = a, b, c, as shown in Fig 6. The lower arm reference currents iLpl, p = a, b, c in respective phase are shifted by π radians. Switching signals are then generated using CPS-SPWM and inductor current balancing technique. These switching signals are given to the CSMMC. Depending on the switching singles, the CSMMC generates the desired output current by inserting/bypassing the SMs in each arm.

IV INTRODUCTION TO FUZZY LOGIC CONTROLLER

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was developed to describe the fuzzy properties of reality, which are very difficult and sometime even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to dc-to-dc converter system. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab/Simulink simulation model is built to study the dynamic behavior of dc-to-dc converter and performance of proposed controllers. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique.

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Thus, fuzzy logic controller has been potential ability to improve the robustness of dc-to-dc converters. The basic scheme of a fuzzy logic controller is shown in Fig 5 and consists of four principal components such as: a fuzzification interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10].

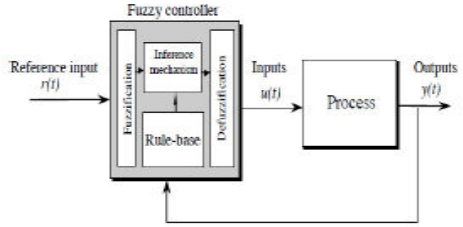

Fig.7. General Structure of the fuzzy logic controller on closed-loop system

The fuzzy control systems are based on expert knowledge that converts the human linguistic concepts into an automatic control strategy without any complicated mathematical model [10]. Simulation is performed in buck converter to verify the proposed fuzzy logic controllers.

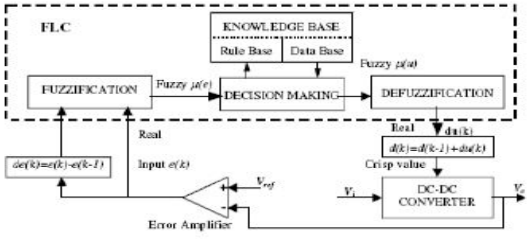

Fig.8. Block diagram of the Fuzzy Logic Controller (FLC) for dc-dc converters

A. Fuzzy Logic Membership Functions:

The dc-dc converter is a nonlinear function of the duty cycle because of the small signal model and its control method was applied to the control of boost converters. Fuzzy controllers do not require an exact mathematical model. Instead, they are designed based on general knowledge of the plant. Fuzzy controllers are designed to adapt to varying operating points. Fuzzy Logic Controller is designed to control the output of boost dc-dc converter using Mamdani style fuzzy inference system. Two input variables, error (e) and change of error (de) are used in this fuzzy logic system. The single output variable (u) is duty cycle of PWM output.

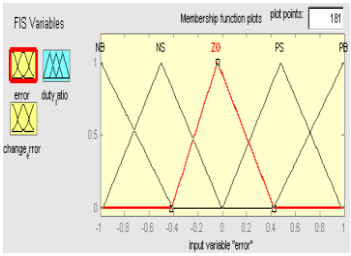

Fig. 9.The Membership Function plots of error

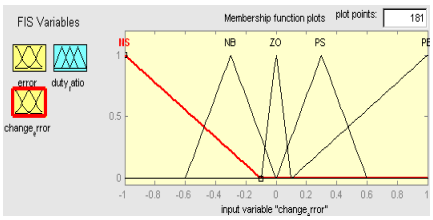

Fig.10. The Membership Function plots of change error

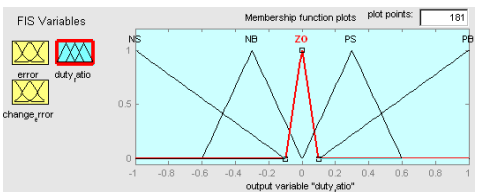

Fig Fig.11. the Membership Function plots of duty ratio

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B. *Fuzzy Logic Rules:*

The objective of this dissertation is to control the output voltage of the boost converter. The error and change of error of the output voltage will be the inputs of fuzzy logic controller. These 2 inputs are divided into five groups; NB: Negative Big, NS: Negative Small, ZO: Zero Area, PS: Positive small and PB: Positive Big and its parameter [10]. These fuzzy control rules for error and change of error can be referred in the table that is shown in Table I as per below:

Table II

Table rules for error and change of error

(de) \ (e)	NB	NS	ZO	PS	PB
NB	NB	NB	NB	NS	ZO
NS	NB	NB	NS	ZO	PS
ZO	NB	NS	ZO	PS	PB
PS	NS	ZO	PS	PB	PB
PB	ZO	PS	PB	PB	PB

VII MATLAB/SIMULATION RESULTS

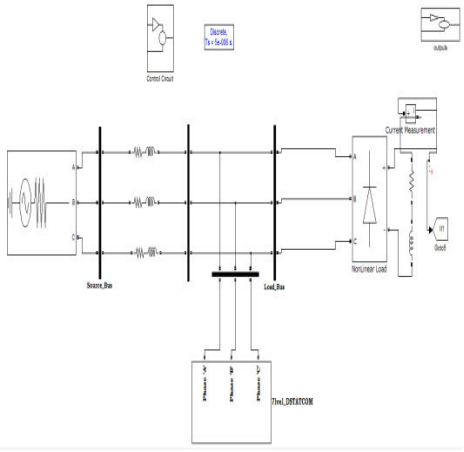
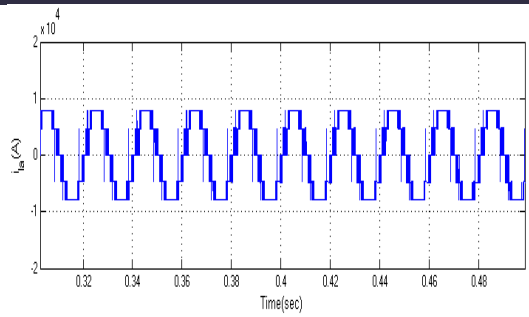
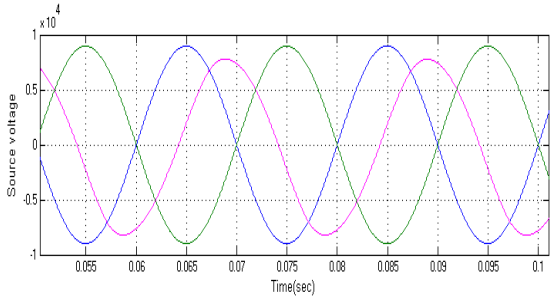


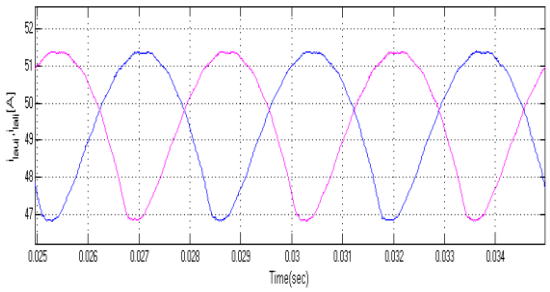
Fig 5.1 Matlab/simulink model of CSMMC based STATCOM control system



(a)



(b)



(c)

Fig 5.2 Simulation Waveforms of Phase a of a standalone CSMMC with interleaved switching for t<1 and non interleaved with t>1 (a) ila (b) source voltage (c) Inductor currents for upper and lower arms

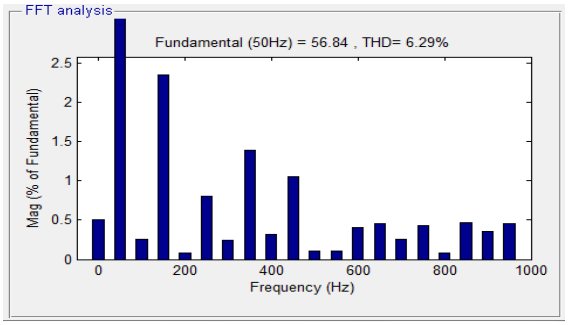


Fig 5.3 THD of Current waveform with PI controller

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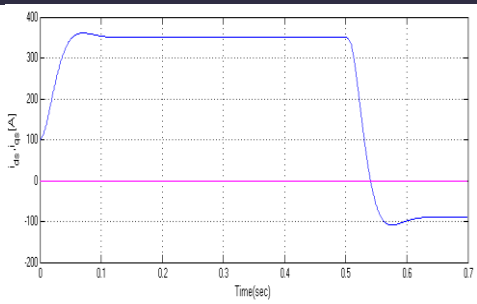
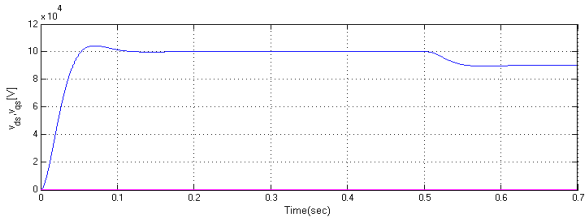


(a)



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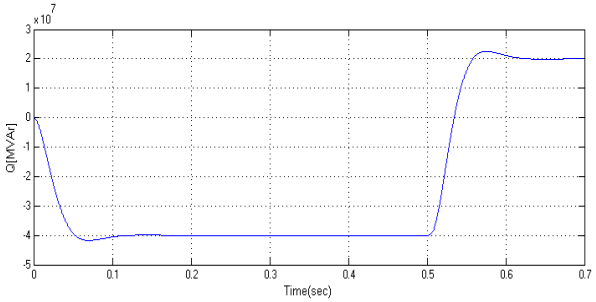

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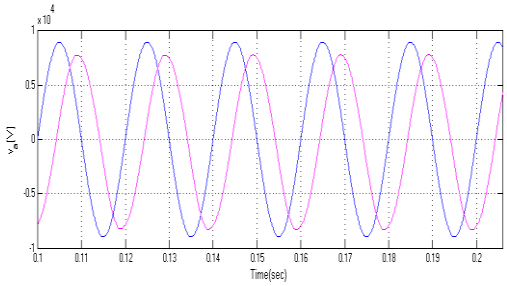

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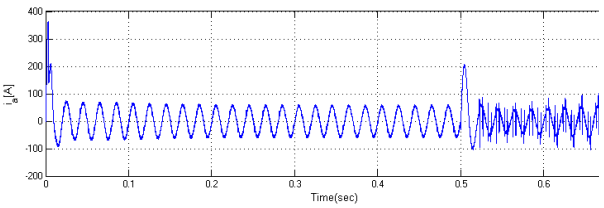

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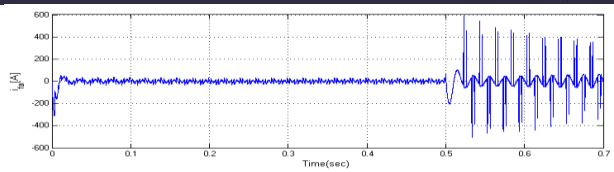
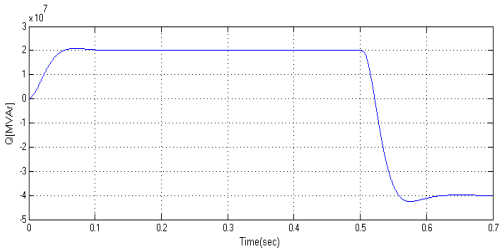


(f)

Fig 5.4Simulation results of STATCOM during transition from capacitive to inductive mode of operation at t = 5 s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage (d) Phase voltage and current (11kV side) (e) Output current of converter (before filter) (f) Filter current.



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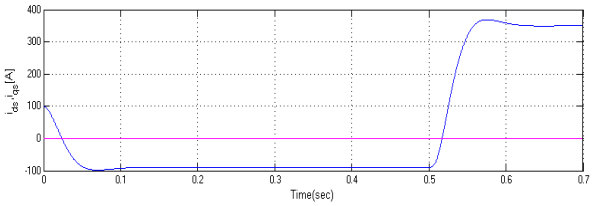

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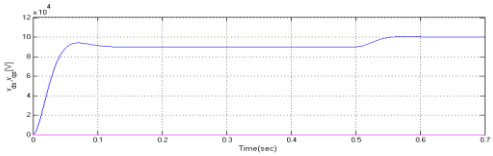

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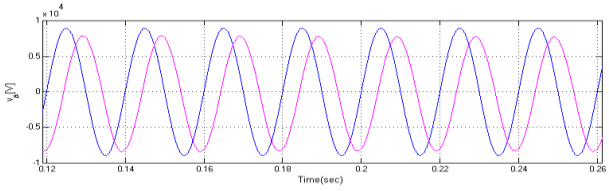

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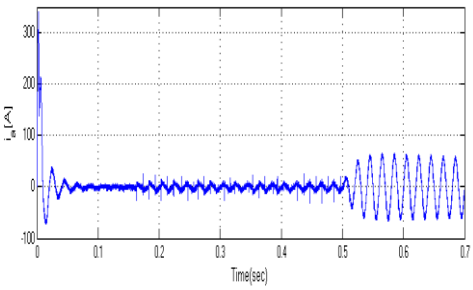

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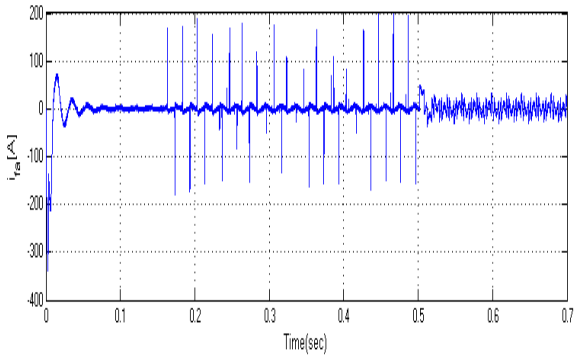
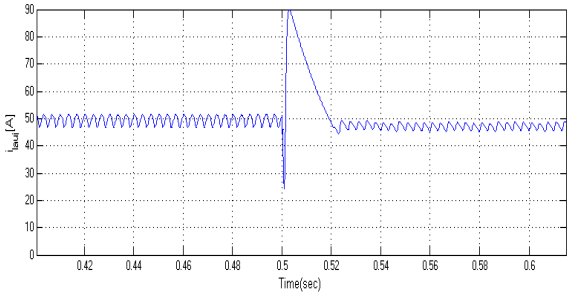


(f)

Fig 5.5 Simulation results of STATCOM during transition from inductive to capacitive mode of operation at t = 6 s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage (d) Phase voltage and current (11kV side) (e) Output current of converter (before filter) (f) Filter current.



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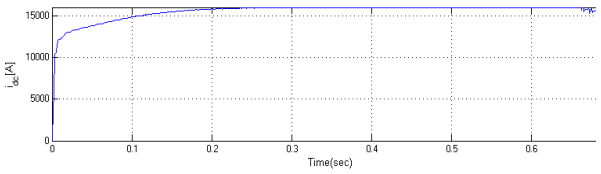
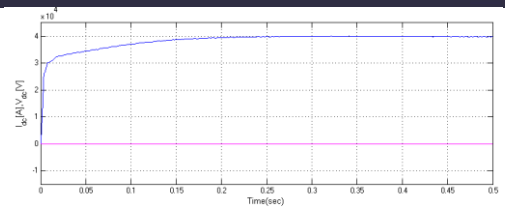


(b)

Fig 5.6 (a) SM inductor currents in upper arm during transition from capacitive to inductive mode of operation at t = 5 s. (b) DC link current.



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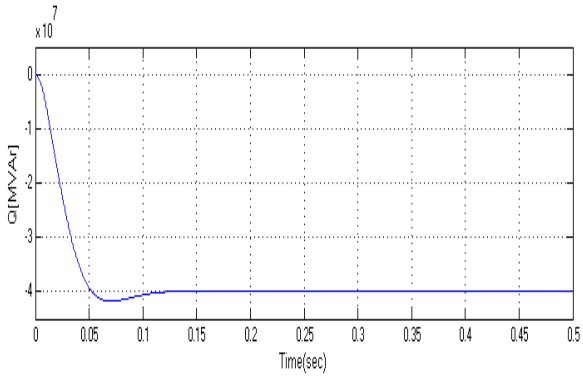

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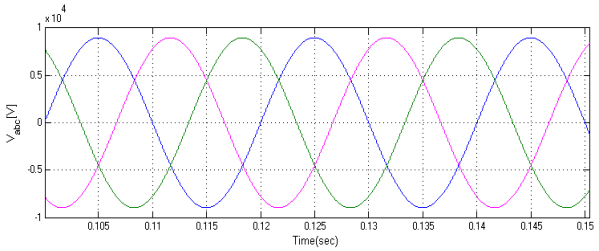

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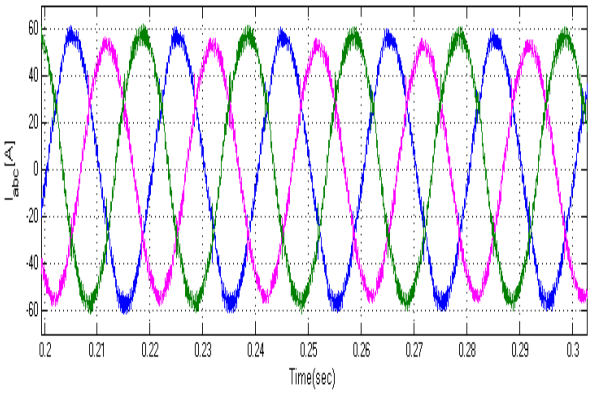

(d)

Fig 5.7 Simulation results of STATCOM during DC fault at t = 11 s, for a duration of 0.2 s. (a) DC link current and voltage (b) Active and reactive power (c) and (d) Three phase voltages and currents (11kV side) .

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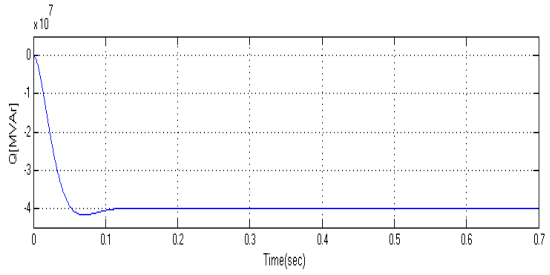
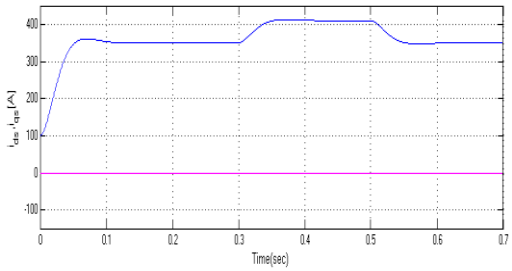


(a)



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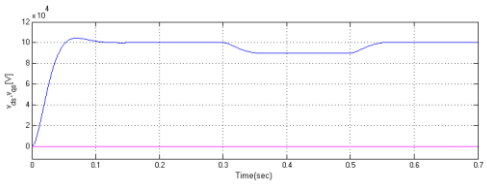

(c)

Fig 5.8 Simulation results of STATCOM during AC fault on gird side at t = 7 s, for a duration of 0.5 s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage.

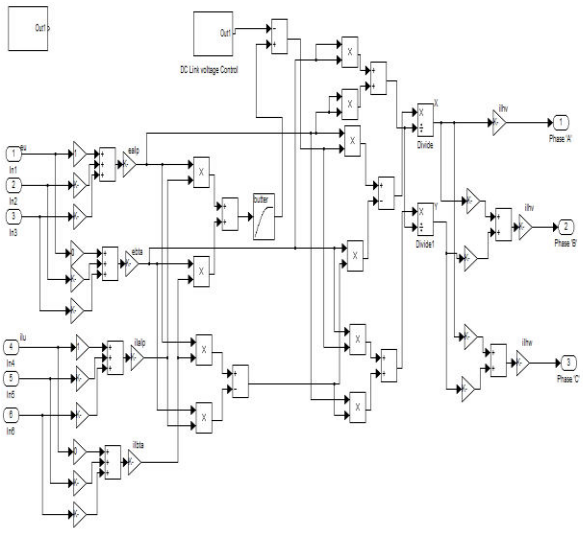

Fig 5.9 simulink diagram of fuzzy controller

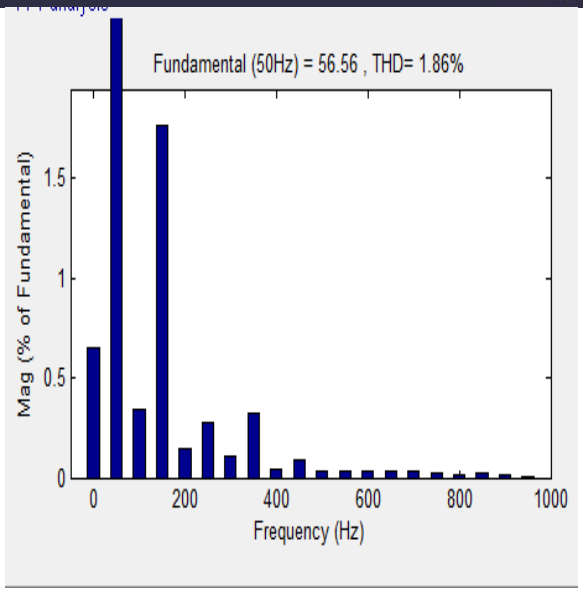

Fig 5.10 THD of Current waveform with fuzzy controller

CONCLUSION

The detailed analytical analysis of a CSMMC and its application as a STATCOM have been presented. In CSMMC, it is important to select SM inductance appropriately because it strongly influences the inductor current ripple. Hence, the method for SM inductance selection is proposed. The CSCs using fully controllable switches have many advantages than LCCs. The main features of CSCs using self-commutating devices are: 1) independent control of the active and reactive power, 2) it can be operated in weak grids or with passive loads, and 3) relatively small footprint because the ac side filters can be eliminated due to low harmonic distortion. The control strategy in dq frame is presented for the CSMMC based STATCOM. The study also shows that the proposed inductor current balancing strategy can effectively provide current balancing for the CSMMC inductors. Hence, CSMMC can be considered as the potential candidate for HVDC and FACTS applications. By using the simulation

results we can analyze the proposed method.

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