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DESIGN AND IMPLEMENTATION OF ULTRA CAPACITOR BASED DYNAMIC VOLTAGE RESTORER FOR SENSITIVE LOAD APPLICATIONS

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Abstract—This paper presents a novel system with improving the voltage quality for the application to sensitive loads from voltage sags/ swells using a dynamic voltage restorer (DVR). Because of higher active power requirement need of jump compensation caused considerable rise in cost and size of the dc link energy storage system (ESS) of DVR. Abovementioned control strategies either diminish the phase jump or progress the employment of dc link energy by, dipping the amplitude of the injected voltage or Optimizing the dc bus energy. In this manuscript, an enhanced sag/swell compensation approach is proposed, and also mitigates the phase jump in the load voltage although improving the overall sag recompense time. In accumulation to this ultra capacitor is used as dc link, which is attached to the system by means of dc-dc converter. An investigative study shows that thisanticipated method drastically increases the DVR sag/swell support time compared with the older phase jump reimbursementtechniques. This development can also be seen as a significant reduction in dclink capacitor size for latest installation. The performance ofthe proposed method is evaluated using simulation studyusing MATLAB/SIMULINK software.

Index Terms—Dynamic voltage restorer (DVR), UCAP, voltage sag compensation, voltagesource inverter (VSI).

I. INTRODUCTION

In industrialized distribution systems, the grid voltage instability (sags, swells, flickers, and harmonics) are the most universal power quality problems [1]. Sag, is typically caused by a fault at the distant bus and is all the time accompanied by a phase angle jump.The phase jump in the voltage can commence transient current in the transformers, capacitors, and motors [2]. It can also disturb the function of commutated converters and may possibly lead to malfunction in the performance of thyristor-based loads [3]. Therefore it is very important to protect sensitive loads, especially from the voltage sags with phase jump [4]. To guard sensitive loads from grid voltage sags, custom power devices are being extensively used [5]–[8]. Amongst these devices, DVR has emerged as the most cost effective and complete solution [9]–[11]. The system arrangement of a DVR is shown in Fig. 1. It consists of a dc link ultra capacitor (serving as an energy reserve), a six-switch voltage source inverter (VSI),a series injection transformer, and an LC filter for eliminating switching harmonics from the injected voltage. The major function of the DVR is to introduce a voltage with definite magnitude and phase in series with the source voltage such that the load connected always sees the pure sinusoidal voltage at its terminals.Several control strategies for DVR have been reported in the literature [12]. The prominence is on either reducing the voltage rating of DVR by aligning the injected voltage with the source voltage or

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minimizing the dc storage capacity with the help of reactive power compensation/energy-optimized approach [12]–[14]. All of these techniques, still, cannot correct the phase jump and therefore can result in early tripping of sensitive loads [15].

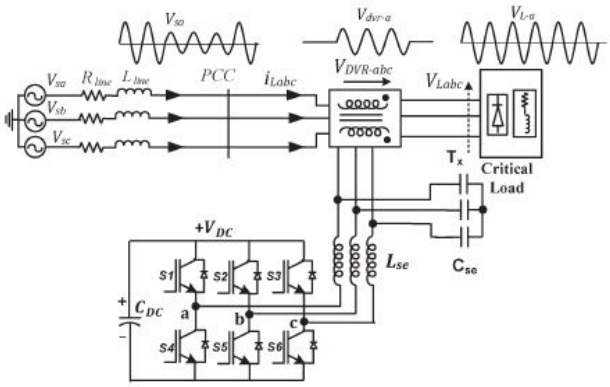

Fig. 1 Basic DVR-based system configuration

The only promising way to mitigate the phase jump is to re-establish the load voltage to the prefault value. Such astrategy is addressed as presag compensation in [13]. Nevertheless, the phase jump compensation with the help of presag method requires a considerable amount of active power from dc link capacitor. Therefore, this method will necessitate a larger size capacitor or will result in shorter sag hold up time. In [16] and [17], afascinating technique is projected to increase the compensation time while mitigating the voltage phase jump. In this technique, if the dc link voltage drops to the threshold limit, the amount of the injected voltage is decreased by synchronizing the phase-locked loop (PLL) to the grid voltage. This allows additional utilization of the dc link capacitor energy and extends the compensation time by some point. Though, it continues to consume the energy in the dc link capacitor throughout the duration of compensation and imposes restriction on compensation time improvement. This paperproposes a novel control strategy in which the main purpose is to improve the sag/swell compensation time whereas mitigating the voltage phase jump. Of all the energy storage technologiesflywheel energystorage system (FESS), super conducting magnet energy storage (SMES), battery energy storage system (BESS),and ultracapacitors (UCAPs), UCAPs are perfect for providingactive power support for actions on the distribution grid whichneed active power support in the seconds to minutes timescale like voltage sags/swells, active/reactive power support,and renewable intermittency smoothing [7].The proposed method objective is regulating the involvement of active power to the least possible value. To avoid the difficulty of over-modulation, in the case of deeper sag depth, an iterative loop is engaged in the control block. It is found that the proposed technique can result in more than 50% extra sag support time when compared with the process in [16] and [17]. The performance of the proposed technique is validated using simulation results.

II. OVERVIEW OF DVR OPERATION

In this section, different sag compensation approaches [12]–[15] are briefly discussed. The phasor representations of thesemethods are given in Fig. 2. The phasors VG and V‘G representthe rated and sagged grid voltages, respectively, whereas VLand V’L are the load voltages before and after the sag. To effectivelyhighlight the differences among these methods, PDVRand QDVR are also incorporated in the phasor diagrams. This ismainly to illustrate the amount of active and reactive powersdemanded by each method. All of the quantities are drawnconsidering the load current (IL) as reference phasor.

A. In-Phase Compensation

In this type of compensation, DVR injects the smallest possiblevoltage magnitude in phase with the sagged grid voltage.However, as seen from Fig. 2(a), this method cannot correct thephase jump. The DVR-injected voltage magnitude and angleare given as

$$V_{\mathrm{DVR}} = \sqrt{2}\,(V_L - V_G') \quad (1)$$

$$\angle V_{\mathrm{DVR}} = \theta_L. \quad (2)$$

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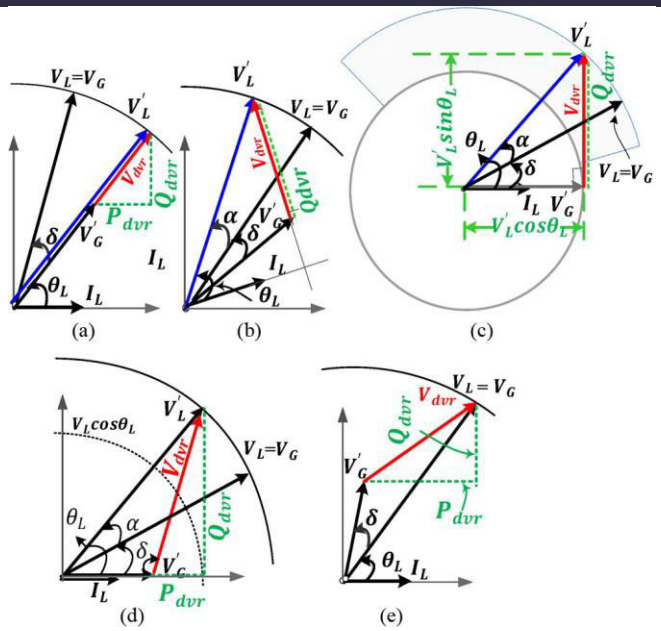

Fig. 2 Per-phase phasor representation of the basic compensationtopologies for DVR (a) In-phase injection (b) Quadrature injection (c)Quadrature injection limiting case (d) Energy-optimized injection (e) Presag injection

B. Quadrature Injection (Reactive Compensation)

In this method, the DVR injects voltage in quadrature withthe load current, i.e., it corrects the sag with only reactivepower. Using Fig. 2(b), the injected voltage magnitude andangle are given as

$$V_{\mathrm{DVR}} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\alpha + \delta)} \quad (3)$$

$$\angle V_{\mathrm{DVR}} = \frac{\pi}{2} \quad (4)$$

Where δ is the phase jump in the grid voltage due to the sag andα is the phase jump induced due to reactive power compensation.As reported in [12], the maximum sag depth (ΔVsag,max)that can be compensated using quadrature injection is closelyrelated with the load power factor and can be expressed as

$$\Delta V_{\mathrm{sag-max}} \leq (1 - \cos\theta_L). \quad (5)$$

The corresponding maximum injected voltage is given as

$$V_{\mathrm{DVR-max}} = \frac{V_G'}{1 - \Delta V_{\mathrm{sag,max}}} \sin\theta_L. \quad (6)$$

Fig. 2(c) shows the limiting case for quadrature injectionwhere DVR supports the full load reactive power while the gridoperates at unity power factor.

C. Energy-Optimized Injection

This method is developed in [15] to enhance the performanceof the quadrature injection method for the sag depth deeper thanthe limit in (5), where the DVR injects certain active power. TheDVR voltage magnitude and injection angle can be calculatedfrom Fig. 2(d)

$$V_{\mathrm{DVR}} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\theta_L)} \quad (7)$$

$$\angle V_{\mathrm{DVR}} = \tan^{-1}\left(\frac{V_L(\sin\theta_L)}{V_L\cos\theta_L - V_G'}\right). \quad (8)$$

D. Presag Compensation

In this method, both load voltage magnitude and phase arerestored to presag values. Unlike the previous methods inFig. 2(a), (b), and (d), the presag method in Fig. 2(e) cansuccessfully compensate the phase jump. However, this phasejump correction requires an additional active power from the dclink capacitor.A positive phase jump leads to an increase in angle betweenthe grid voltage and the load current, increasing the activepower burden on DVR compared to negative phase jump. UsingFig. 2(e), the injected voltage magnitude and angle can bewritten as

$$V_{\mathrm{DVR}} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\delta)} \quad (9)$$

$$\angle V_{\mathrm{DVR}} = \tan^{-1}\left(\frac{V_L\sin\theta_L - V_G'\sin(\theta_L - \delta)}{V_L\cos\theta_L - V_G'\cos(\theta_L - \delta)}\right). \quad (10)$$

III. POWER FLOW ANALYSIS ANDMAXIMUM COMPENSATION TIME

As explained earlier, the presag method is the most energyintensivemethod, and the injected power can be quite higheven for shallow sag depths. Based on the phasor diagram ofFig. 2(e) [(9) and (10)], the active power associated with thepresag method can be expressed in terms of sag depth, phasejump, and load power factor as given in the following:

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$$P_{\text{presag}} = \sqrt{3}V_L I_L(\cos(\theta_L) - (1 - \Delta V_{\text{sag}})\cos(\theta_L - \delta). \quad (11)$$

A detailed derivation of (11) is given in Appendix A. Fig. 3shows the DVR active power for a range of variation in sagdepth (0.1 ≤ΔVsag ≤0.9) and power factor (0.4 ≤cos θL ≤0.9). The phase jump δ is fixed at +25◦. As seen from the graphof Fig. 3, the active power supplied by DVR is relatively high(>0.4 p.u.) for the presag method.The theoretical power flow analysis conducted previouslyholds true as long as there is a significant amount of energyin the dc link capacitor. However, in the actual system, since ithas a finite amount of energy, the voltage across the dc linkcapacitor Vdc reduces. The following relationship should besatisfied at all time in order to achieve the adequate operationof DVR-VSI [18]:

$$\frac{V_{\text{dvr}}}{n_t} \leq \frac{m_{i-\max} V_{\text{dc}}}{2} \quad (12)$$

Where nt is the turns ratio of the series transformer and mi − maxis the maximum modulation index of VSI. Vdvr is the injectedphase to neutral voltage. Vdc is the dc link voltage. As soon asthe dc link voltage decreases below Vdc−min, i.e., the limit setby (12), the DVR controllermust stop the compensation processto avoid harmonics contamination in the load voltage.The energy stored in the dc link capacitor is equal to

$$E_{c-\text{dc}} = \frac{1}{2} C_{\text{dc}} V_{\text{dc}}^2. \quad (13)$$

The power flow out of the dc link capacitor in the steady stateis given as

$$P_{c-\text{dc}} = \frac{1}{2} C_{\text{dc}} \frac{d}{dt} V_{\text{dc}}^2. \quad (14)$$

Considering a lossless DVR system, the dc power in (14) canbe equated with the ac power of (11) to find the capacitor size.However, owing to the flow of active power, the dc link voltagedrops, and the limit in (12) can be violated. This limitationrestrains the DVR operation even though there is sufficientamount of stored energy in the dc link capacitor as shown inFig. 4. Furthermore, the gradient of the dc link voltage dvdc/dtis directly proportional to the DVR-injected active power, i.e.,Pdvr. The lower the value of Pdvr, the smaller is the slope ofthe dc link voltage and the higher will be the time for whichVdvr/nt ≤(mi−maxVdc)/2. This leads to the following twohypotheses.

1) The energy stored in the dc link capacitor can further beutilized.

2) The rate of change (fall) of the dc link voltage can furtherbe optimized.

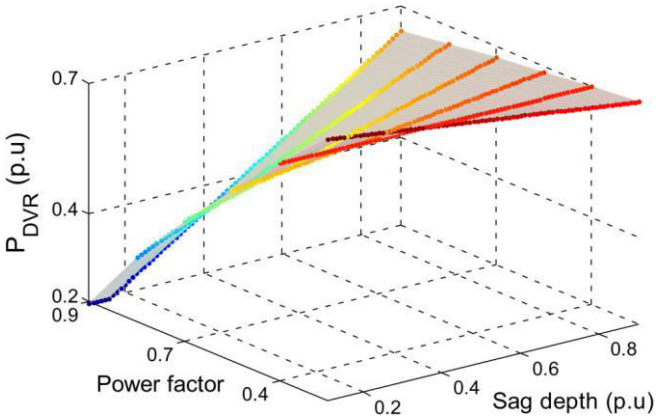

Fig 3 Active power associated with the presag compensation methodfor different sag depths (phase jump = 25◦).

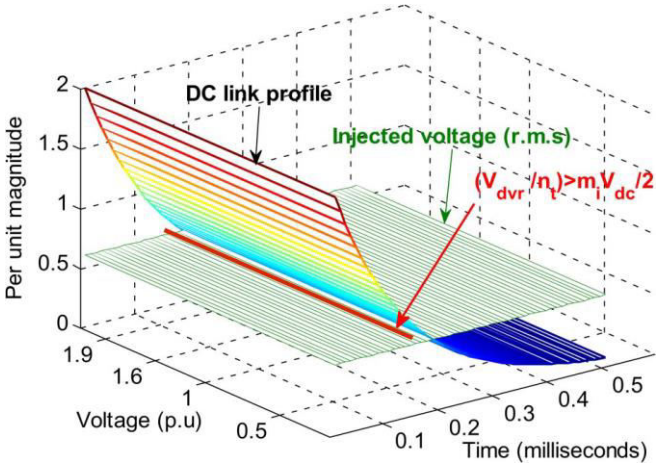

Fig 4 DC link capacitor voltage profile during presag injection

This brings another important variable in the power flowanalysis which is the "maximum compensation time tc − max."It is the direct measure of "useful" stored charge/energy inthe dc

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link capacitor. The tc−max can be determined from theboundary condition of (12) and (14) as given in the following:

$$t_{c-\max} = \frac{C * \left[V_{\rm dc}^2 - \left(\frac{2*V_{\rm dvr}}{m_{i-\max}*n_t}\right)^2\right]}{2 * P_{\rm dvr}}. \qquad (15)$$

A detailed derivation of (15) is given in Appendix B. Toincrease tc−max, Meyer et al. suggested a method in [16] and[17] which decrease the injected voltage magnitude once thedc link voltage dropped to the threshold limit of (12) and allowsfurther utilization of the dc link stored energy. However, asdiscussed in the introduction section, this method has no controlon the injected active power and therefore is not the best choicefor getting the maximum compensation time [18].

IV. PROPOSED COMPENSATION SCHEME

The work presented in this paper proposes an enhanced sagcompensation method to extend the DVR compensation time.It optimizes the gradient of the dc link voltage (dvdc/dt) byregulating the amount of active power injected by DVR. Inthe proposed method, the controller restores both phase andamplitude of the load voltage to the presag value and theninitiates a transition toward the minimum active power (MAP)mode. The overall operation sequence and implementation ofthe proposed compensation method is discussed in the followingsubsections.

A. Phase Jump Detection and Presag Restoration

For detecting the phase jump, two PLLs are employed (oneover the load voltage and another over the source voltage), givingθV L and θV g, respectively. As soon as the sag is detected,the first step is to determine the DVR initial injection angle thatavoids the phase jump at the load side. This is done by freezingthe load voltage PLL that gives the presag angle (θV Lp). Onthe other hand, the unrestricted grid voltage PLL gives the gridvoltage phase (θV g). The difference between these two anglesgives the initial angle of injection

$$\left.\begin{aligned}\theta_{\rm init} &= \theta_L + (\theta_{VLp} - \theta_{Vg}) \\ &= \theta_L + \delta\end{aligned}\right\}. \qquad (16)$$

Note that, in the steady state, both angles will be identical,and thus, the difference will be zero. For sag detection, theabsolute difference between the reference load voltage (1p.u.)and the actual grid voltage (p.u.) in synchronous referenceframe is calculated as follows [7], [19]–[22]:

$$\Delta V_{\rm sag} = \left|1 - \sqrt{V_{gd}^2 + V_{gq}^2}\right|. \qquad (17)$$

As soon as ΔVsag >0.1, it is recognized as voltage sag [23].

B. Controlled Transition toward the MAP Mode

Once the presag voltage is successfully restored, after onecycle, a smooth transition toward the MAP mode is initiated andcompleted over the next one to two cycles. The final injectionangle of DVR (θfin) is given as

$$\theta_{\rm fin} = \left\{\begin{aligned}&\tfrac{\pi}{2}+\gamma, && \text{if } \Delta V_{\rm sag} \le (1-\cos\theta_L) \\ &\pi - \tan^{-1}\left(\tfrac{V_L(\sin\theta_L)}{V_L\cos\theta_L - V_g'}\right), && \text{if } \Delta V_{\rm sag} > (1-\cos\theta_L)\end{aligned}\right\}. \qquad (18)$$

A detailed derivation of (18) is given in Appendix C. The firstpart of (18) represents the self-supporting mode of operationin which the DVR absorbs active power (relatively very smallamount) from the grid to overcome the system losses and thusmaintains a constant voltage across the dc link capacitor. Theterm γ indicates the reduction in θfin due to loss component andis determined by the dc link (PI) controller. The second part of(18) represents a case where the self-supported dc link cannotbe maintained due the constraint in (5). To ensure a smoothchangeover, a transition ramp is defined between the initial andfinal operating points, as given in the following:

$$\theta_{\rm trans} = \theta_{\rm init} + \frac{\theta_{\rm fin} - \theta_{\rm init}}{\Delta T}(t) \qquad (19)$$

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Where ΔT determines the slope of the transition curve and ischosen as 30 ms.

C. Iterative Decrement in Injection Angle

In self-supporting mode, the DVR can compensate the sagfor an indefinitely long time. However, for deeper sag depths,there is certain nonzero active power injected by DVR. Thiscauses a reduction in the energy stored in the dc link capacitor,and consequently, its voltage reduces (gradually). To maintainthe required voltage at the inverter output side, the controllerincreases the modulation index mi until it reaches mi−max.This is the limiting case as explained by (12), beyond whichthe controller goes into over-modulation and cannot maintain therated load voltage. To avoid this over-modulation condition, aniterative control loop is used, which constantly monitors the dclink voltage and decreases θfin in (18) to keep Vdc > Vdc−minand is given as

$$\theta_{\text{fin}} = \theta_{\text{fin}} - \epsilon \qquad (20)$$

Where ϵis chosen as 0.01 rad.

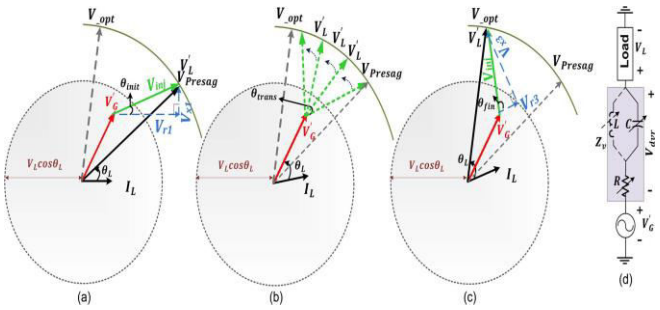

Fig 5 Phasor diagram for the proposed sag compensation method (a) Presag restoration, (b) intermediate transition, (c) final load voltage withMAP injection, and (d) DVR visualization as the variable virtual impedance changes from resistive to dominant capacitive (sag) or inductive (swell)

D. Operation Sequence

Fig. 5(a)–(c) depicts the overall operation sequence of theproposed phase jump compensation scheme. The transitionfrom high active power mode (presag) to MAP mode is shownin three steps. The illustration is for the case where the sag depthis more than the limit in (5) and there is a positive phase jumpassociated with the sag. As discussed previously and shownin Fig. 5(a), DVR initiates the compensation by supplyinghigh active power to the load (Vr1 >> Vx1) and restores bothmagnitude and phase of the load voltage to presag values. Afterone cycle, the transition toward the MAP mode is initiated, andDVR gradually increases the contribution of reactive power. Asseen from Fig. 5(b) and (c), the injected voltage magnitudeand its phase angle are gradually increasing until V'L reachesVL−opt. Note that at the final operating point Vr1<<Vx1.The aforementioned DVR operation can be viewed as anequivalent variable impedance Zv where the operation beginswith dominant resistive impedance Zv = R (high active power)and completes as dominant capacitive impedance Zv ≈ XC(high reactive power).

V. ANALYTICAL STUDY ON COMPENSATION TIME WITH DIFFERENT APPROACHES

In this section, a comparative study is presented to determinethe maximum compensation time achieved using the aforementionedphase jump compensation methods. These includethe following: 1) the presag; 2) the method given in [16],named as presag–in-phase in this paper; and 3) the proposedmethod. Table I shows the various design parameters used forthe comparison. The maximum compensation time of 200 ms(10 cycles) with a phase jump of +45◦is taken as reference.Using (15), the value of the dc link capacitor is obtained as9000 μF.The sag depth is varied over a range of values from 10%to 80% of nominal grid voltage, keeping the power factorand phase jump fixed at 0.7 lagging and +45◦, respectively.Analytically computed DVR-injected magnitude and maximumcompensation times are provided in Fig. 6. Note that the DVRvoltage magnitudes are shown after the first one cycle ofcompensation as all of the three methods

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perform identicallyfor the first cycle. As seen from Fig. 6(b), both the presage and proposed methods have the same VDVR magnitude for asag depth greater than the limit in (6), i.e., 30%. However,as noticed from Fig. 6(a), tc−max is highest for the proposedmethod for all values of sag depths. For the designed range of50% sag depth, it can be seen that the presag–in-phase methodimproves the compensation time from 10 to 16 cycles over thepresag method. The proposed method further improves it to22 cycles. Moreover, for the sag depth lower than 30%, theproposed method can withstand any sag duration by operatingin the self-supporting mode. The significant improvement inthe compensation time is due to the least possible utilization ofdc link active power, thus resulting in the slowest dischargingof the dc link capacitor. Note that the proposed method doesnot result in higher injection voltage magnitude than the designlimit of 0.7 p.u., which is clear in Fig. 6(b).Fig. 7 depicts the scenario where the phase jump is variedfrom −90◦to +90◦for a sag depth of 0.5 p.u. and otherboundary conditions from Table I. As seen from the graph,the maximum compensation time is highest for the proposedmethod. It can also be noted that the presag method becomesunable to correct the phase jump beyond −60◦and +60◦due toviolation of (12).

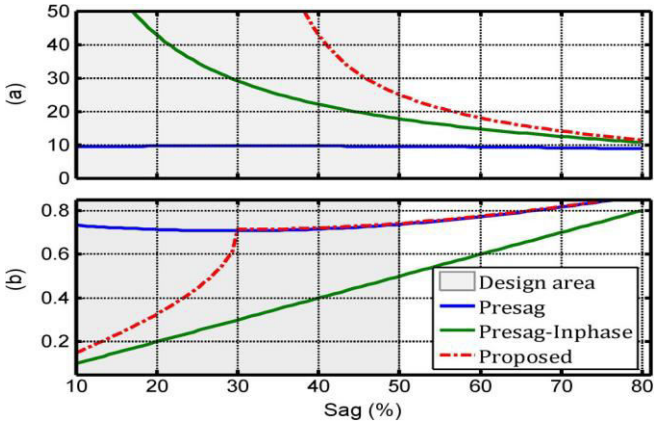

Fig 6 Maximum compensation time and DVR-injected voltage forvarious sag depths with different methods. (a) Compensation timecycles. (b) VDVR p.u.

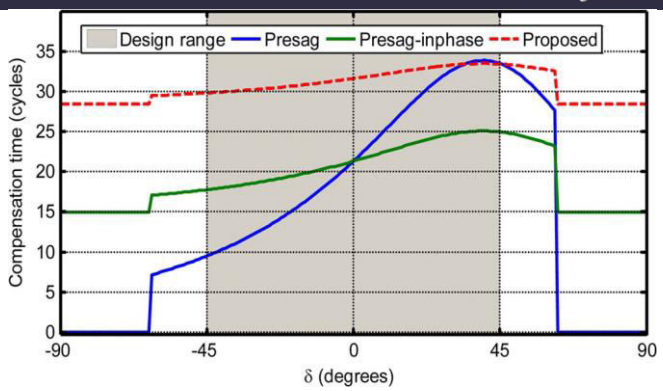

Fig 7 Maximum compensation time for a range of variation in phasejump

TABLE I
DVR SYSTEM PARAMETERS (BOUNDARY CONDITIONS)

Parameter	Value
Grid voltage (L-L) (rms) V_{base}	415 V
Line frequency	50 Hz
Nominal Power (Base kVA)	10 kVA
Nominal Load power factor	0.7 Lagging
Maximum compensation time	10 cycles
Maximum sag depth	0.5 p.u
Maximum phase jump	$\pm 45^0$
Maximum injected voltage	0.7 p.u
Transformer turns ratio	1:1
DC link Capacitance value	9000 μF

VI.UCAP AND BIDIRECTIONAL DC–DC CONVERTER

A. UCAP

Of all the energy storage technologiesflywheel energystorage system (FESS), superconductingmagnet energy storage (SMES), battery energy storage system (BESS),and ultracapacitors (UCAPs), UCAPs are perfect for providingactive power support for actions on the distribution grid whichneed active power support in the seconds to minutes timescale like voltage sags/swells, active/reactive power support,and renewable intermittency smoothing [7].

Bidirectional DC–DC Converter and Controller

A bidirectional dc–dc converter is required as an interfacebetween the UCAP and the dc-link, since the UCAP voltagevaries with the amount of

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energy discharged, while the dc-linkvoltage has to be stiff. The dc–dcconverter should operate in Discharge mode, while providingactive/reactive power support and voltage sag compensation.The dc–dc converter should also be able to operate in bidirectionalmode to be able to charge or absorb additional powerfrom the grid during intermittency smoothing. In this paper,the bidirectional dc–dc converter acts as a boost converter,while discharging power from the UCAP and acts as a buckconverter while charging the UCAP from the grid.Average current mode control, which is widely explored inliterature [19], is used to regulate the output voltage of the bidirectionaldc–dc converter in both Buck and Boost modes whilecharging and discharging the UCAP bank. This method tendsto be more stable when compared with other methods likevoltage mode control and peak current mode control. Averagecurrent mode controller, where the actualoutput voltage Vout is compared with the reference voltageVref and the error is passed through the voltage compensatorC1 (s) that generates the average reference current Iucref.

VII. SIMULATION RESULTS

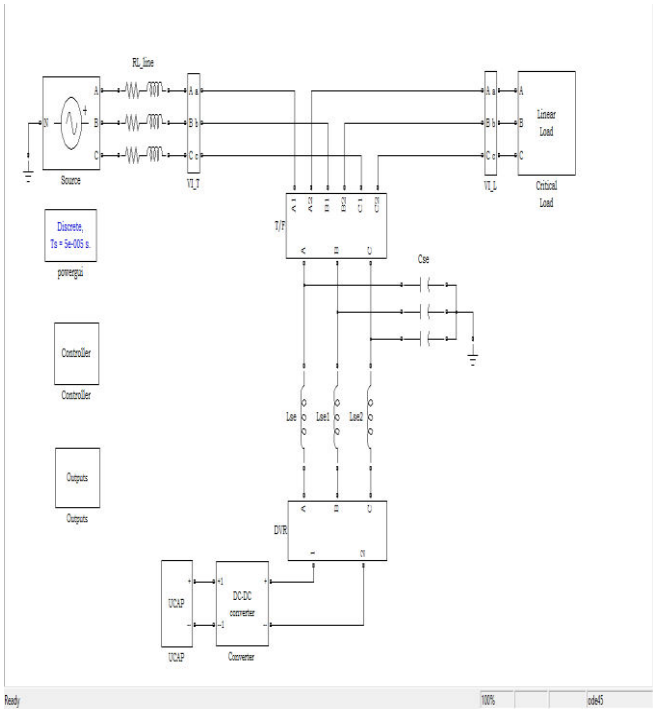

Fig 8 simulation diagram of Proposed DVR system with UCAP and DC-DC converter

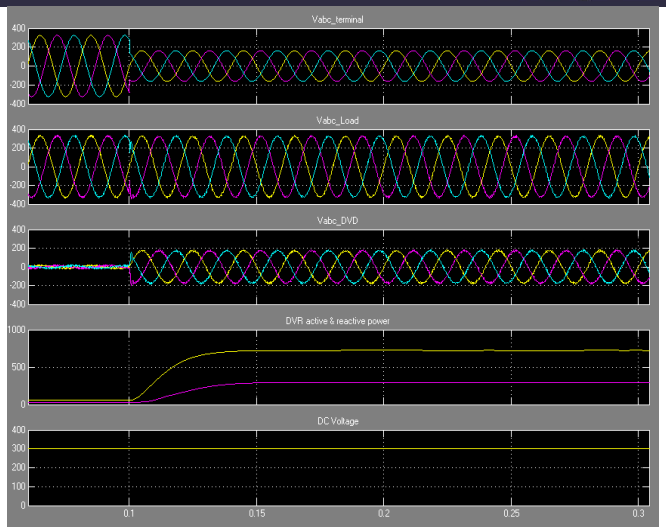

Fig. 9 Simulation results for the proposed sag compensation methodfor 50% sag depth. (a) PCC voltage. (b) Load voltage. (c) DVR voltage.(d) DVR active and reactive power. (e) DC link voltage.

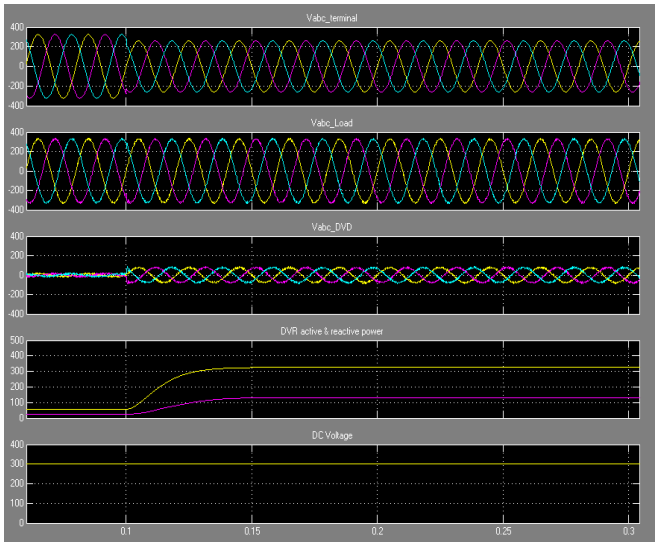

Fig 9 Simulation results for the proposed sag compensation methodfor 23% sag depth. (a) PCC voltage. (b) Load voltage. (c) DVR voltage.(d) DVR active and reactive power. (e) DC link voltage.

VIII. CONCLUSION

Aforementioned control strategies either diminish the phase jump or progress the employment of dc link energy by, dropping the amplitude of the injected voltage or Optimizing the dc bus energy. In this manuscript, an enhanced sag/swell compensation approach is proposed, and also

mitigates the phase jump in the load voltage although improving the overall sag recompense time. In addition to this ultra capacitor is used as dc link, which is attached to the system by means of dc-dc converter. So this paper presents the system with improving the voltage quality for sensitive loads from voltage sags and swells using a dynamic voltage restorer (DVR). Because of higher active power requirement need of jump compensation caused considerable rise in cost and size of the dc link energy storage system (ESS) of DVR. An investigative study shows that this proposed method drastically increases the DVR sag/swell support time compared with the older phase jump compensation techniques. The performance of the proposed method is evaluated using simulation study using MATLAB/SIMULINK software.

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