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Volume 07, Issue 12, Pages: 200–204.

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A NOVEL INTERLEAVED DUAL BUCK FULL-BRIDGE THREE-LEVEL INVERTER (IDBFTI) IS PROPOSED FOR THE GRID-CONNECTED SYSTEM

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Abstract—The technology of interleaved parallel inverter is one of the major ways to solve the above problems. It retains the advantages of interleaved parallel technology for inverter as follows: reducing the output ripple current and the total harmonic distortion of the output current, increasing the power density of system, and reducing the current stress and thermal stress of power devices. Besides, it can solve the problem of zero sequence circulation current (ZSCC) in interleaved inverter system by the circuit structure, and it also has the advantages of no shoot-through problem, no reverse recovery of the body diode, and three-level output. The interleaved inverter circuits share two power-frequency switches, which are resized for each specific application, and it is easier to extend the system by improving current capability of the two switches. The working principle of this system is introduced in detail. Test results verify the principle and the excellent performance of IDBFTI.

Keywords:THREE-LEVEL INVERTER, ZERO SEQUENCE CIRCULATION CURRENT (ZSCC), POWER DENSITY.

INTRODUCTION

A novel interleaved dual buck full-bridge three-level inverter (IDBFTI) is proposed for the grid-connected system in this project.The multiply interleaved technology can increase the equivalent switching frequency and decrease switching frequency of each parallel inverter. Besides, the voltage stress of power devices, the switching loss, and the conduction loss can also be reduced. As the power of single inductor reduces by $N2$, where N is the number of parallel inverters, the volume and weight of system can be reduced and its dynamic property is improved.In recent years, there are a lot of research works and applications about interleaved parallel inverter. For example, the interleaved half-bridge inverter was used for grid-connected power generation with inductor filter. By interleaved switches, soft switching was realized and losses of body diode reverse recovery were eliminated. Interleaved modulation strategy was then used in cascade multilevel inverter, which decreases the output ripple and filter. The interleaved control strategy was used in buck/boost converter with double tube, which reduces the magnetic components. In order to further reduce the current ripple, or achieve the goal of optimizing the magnetic parts, the magnetic integration technology and matrix transformation technology of interleaved inverter were studied. Modulation strategies of interleaved inverters include: phase shift, phase disposition (PD), phase opposite disposition, and alternate phase opposite disposition. In view of the nonlinear link for the digital control, a new control method was proposed in the three-route

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interleaved fixed-frequency quasi-sliding mode control method was proposed for the inverter parallel system to realize zero output ripple (called zero average dynamics in the project) and three phase decoupling control. In [19], the method of optimized space vector modulation for interleaved parallel inverter was proposed to minimize ripple current. The disturbance processing method of interleaved inverter with coupled inductor based on a discrete-time decoupling network was proposed the repetitive control was used for interleaved parallel inverters in Yet, there still exists some issues about the inverter interleaved parallel technology to be discussed. Pan and Liao demonstrated that there was a flow path for ZSCC in the parallel inverter system. In some interleaved inverter systems with inductive magnetic coupling, the current of each leg are coupled, and the systems are actually complex multiinput and multioutput systems, so the problem of ZSCC becomes more complex.

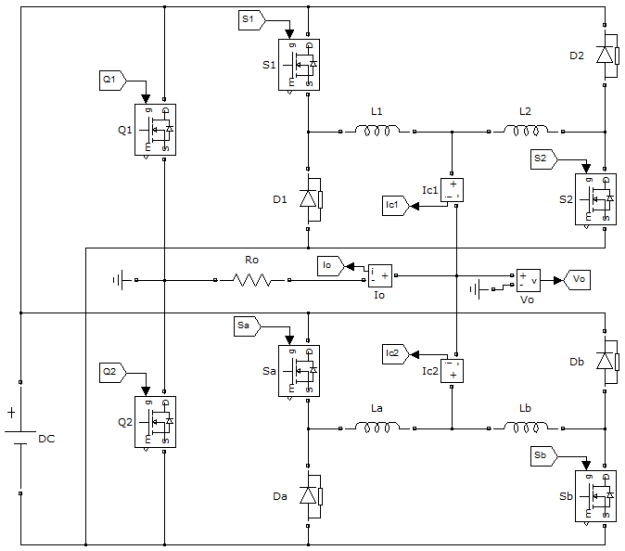

Fig.1. Dual buck full-bridge three-level inverter sim

DUAL BUCK FULL-BRIDGE THREE-LEVEL INVERTER (IDBFTI)

Fig. 1 shows the topology of DBFTI. The specific system operation is described as follows: The driving signals of power switches $Q1$ and $Q2$ are produced by the over zero comparing circuit based on the grid voltage. When the grid voltage is greater than zero, $Q2$ is turned ON and $Q1$ is turned OFF, when it is less than zero, $Q2$ is turned OFF and $Q1$ is turned ON. The inverter works in half-cycle mode. It means that the buck circuit 1 consisting of power switches $S1$, $Q1$, $Q2$, freewheeling diode $D1$, filter inductor $L1$, and filter capacitor Cfstarts to work when the output current $io$is in the positive half-cycle. While in the negative half cycle, the buck circuit 2 composed of power switches $S2$, $Q1$, $Q2$, freewheeling diode $D2$, filter inductor $L2$, and filter capacitor Cfworks.The proposed IDBFTI is constructed on the basis of the circuit in Fig. 1 by adopting interleaved parallel technology. The inverter adopts the unipolar frequency doubling SPWM for dual buck circuit to guarantee the waveform of output current, and PI controller is used as the closed-loop control strategy. As shown in Fig. 2, the part 1 is the first inverter circuit I, the part 2 as the second inverter circuit II. The duty cycle of switches $Sa$and $Sb$are the same with that of corresponding switches $S1$ and $S2$ in one switching cycle, but the driving signals of Sa and Sbhave half-switching cycle lag, so the ripple frequency of total current is doubled and the total output ripple current is reduced. In addition, the two circuits share two power frequency switches $Q1$ and $Q2$, which can be resized for each specific application, and it is easy to extend the system by improving current capability of the two switches. The decrease of the current through switches $S1$,$S2$, Sa , Sb, reduces the conduction loss of the switches and further increases the power levels of the inverter.

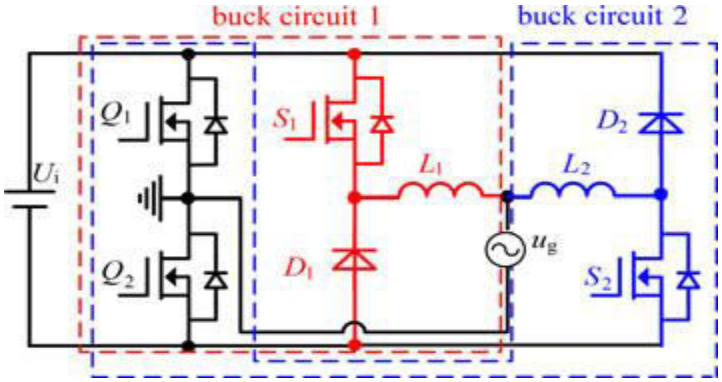

Fig. 1 Dual buck full-bridge three-level inverter

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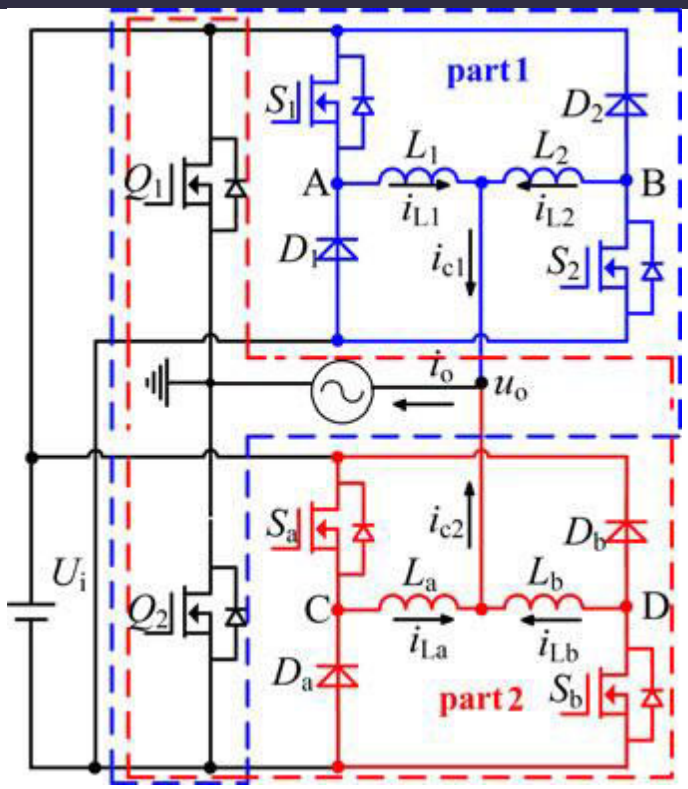

Fig. 2 Interleaved dual-buck full-bridge three-level inverter

ANALYSIS OF WORKING CONDITION OF IDBFTI

Key waveforms of IDBFTI are shown in Fig. 3.

1) Stage $t0 \sim t1$:During this stage, the grid voltage and grid current are both greater than zero, and $Q2$ is turned ON, $Q1$ is turned OFF, inductive current $iL2 = iLb = 0$, $ic1 = iL1$, $ic2 =$ follows:

Mode 1:As shown in Fig. 4(a), power switches $S1$, $Sa$and $Q2$ are turned ON and $S2$, $Sb$and $Q1$ are turned OFF, so current $iL1$, iLa rises linearly.

Mode 2:As shown in Fig. 4(b), power switches Sa,$Q2$ are turned ON and $S1$ is turned OFF. Current $iL1$ flows through $D1$ and decreases linearly. Current iLa rises linearly.

Mode 3:As shown in Fig. 4(c), power switches $S1$, $Q2$ are turned ON and $Sa$is turned OFF. Current iLa flows through Da and decreases linearly. Current $iL1$ rises linearly.

Mode 4:As shown in Fig. 4(d), power switches $Q2$ is turned ON and $S1$ and $Sa$are turned OFF. Current $iL1$ flows through $D1$ and decreases linearly. Current iLa flows through Da and decreases linearly.

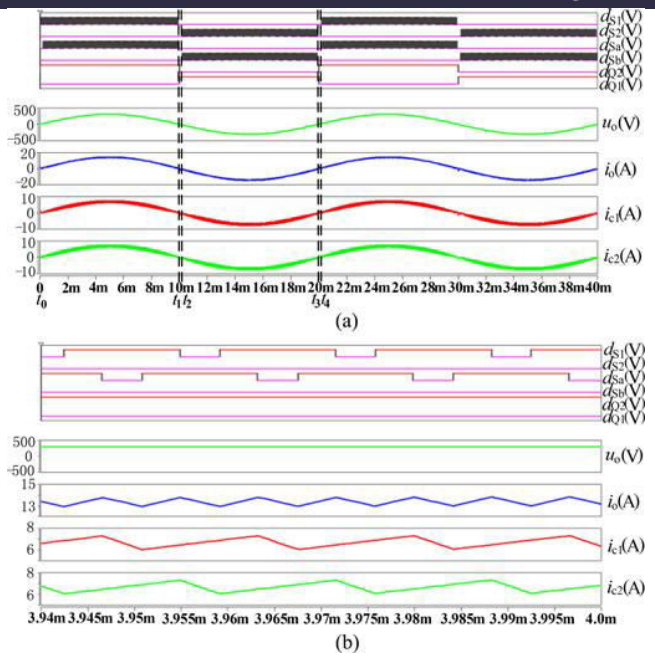

Fig. 3 Key waveforms of IDBFTI at full load

2) Stage $t1 \sim t2$ *:*This stage is the dead time between the drive signals of switches$Q1$ and$Q2$. The dead time is set to avoid shoot-through problem of switches$Q1$ and$Q2$. The switches are just turned ON and OFF once in a power frequency cycle, so the influence of dead time can be ignored. The shoot-through problem of low frequency legs has only a small impact on the output current. During this stage, $Q2$ is turned OFF and $Q1$ is not already turned ON. At the time $t1$, the inductive current $iL1$and iLa are also greater than zero. The circuit contains two working modes as follows:

Mode 5:As shown in Fig. 4(e), power switches $S1$,Sa , $Q2$, $S2$, Sb, $Q1$ are turned OFF. $u0>0$, $iL1$ >0, $iLa>0$. Current $iL1$ flows through $D1$ and decreases linearly. Current iLa flows through Da and decreases linearly. Output current ioflows through the body diode of $Q1$ and decreases.

Mode 6:As shown in Fig. 4(f), power switches $S1$,Sa , $Q2$, $S2$, Sb, $Q1$ are turned OFF. $uo>0$. Currents $iL1$ and iLa fall down to zero. The inverter does not operate during this time.During the stage $t2 \sim t4$, the grid voltage is in the negative half-cycle. The switch $Q1$ is turned ON and $Q2$ is turned OFF, and the working process of inverter is symmetrical with the process in the

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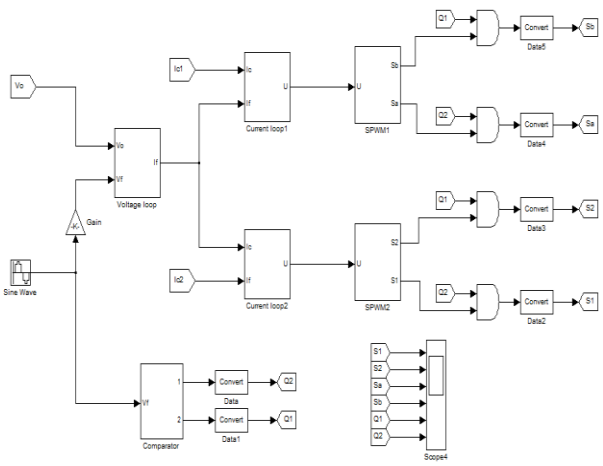
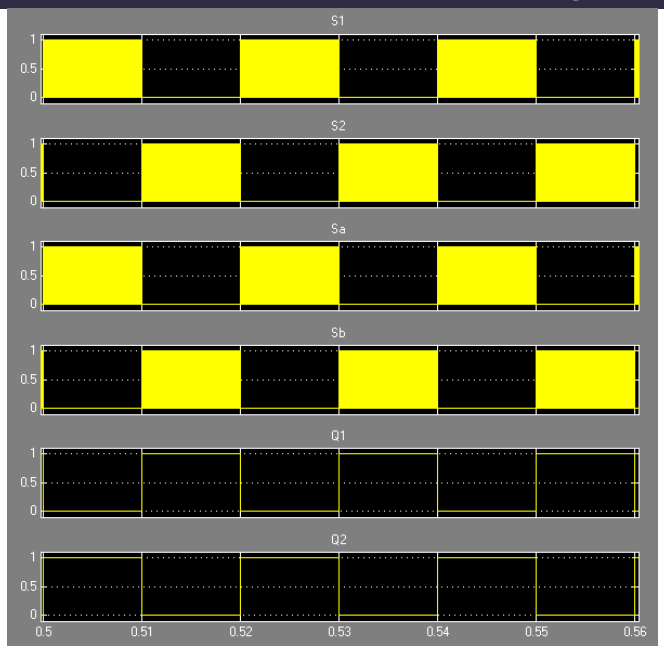
positive half-cycle, which is shown in Fig. 5. Pan and Liao [22] demonstrate that there is a flow path for zero sequence circulation current (ZSCC) in the inverter parallel system. Here, the interleaved half-bridge inverter is taken for example to analyze the path of circulation current. As shown in Fig. 6, when the interleaved parallel strategy is used, switch *S*1 of half-bridge inverter A and the switch *S*4 of half-bridge inverter B can conduct during the interval [*t*0, *t*1] in Fig. 7. When working in discontinuous current mode, the inverter will generate circulation current *i*bias(*i*bias = *iL*2), which flows through two half-bridge inverters, and the current *iL*2 of half-bridge inverter B is reversed, so the current flowing through the load *io*(*io*= *iL*1 + *iL*2) will be reduced relatively. Consequently, there will be several problems such as additional power losses, lower efficiency, and increased device stress. However, switch *S*1 of IDBFTI just works in the positive half-cycle of output current and switch *Sb*of IDBFTI is opposite, so they will not be turned ON at the same time and the circulation current will also not be generated. Fig. 8 shows the working modes of the interleaved dual buck inverter, while the top switches are not turned-on simultaneously. The freewheeling current flow through diode, which prevents the reverse current to flow, so there is no circulation current and the polarity of current *ic*2 is the same with that of current *ic*1.

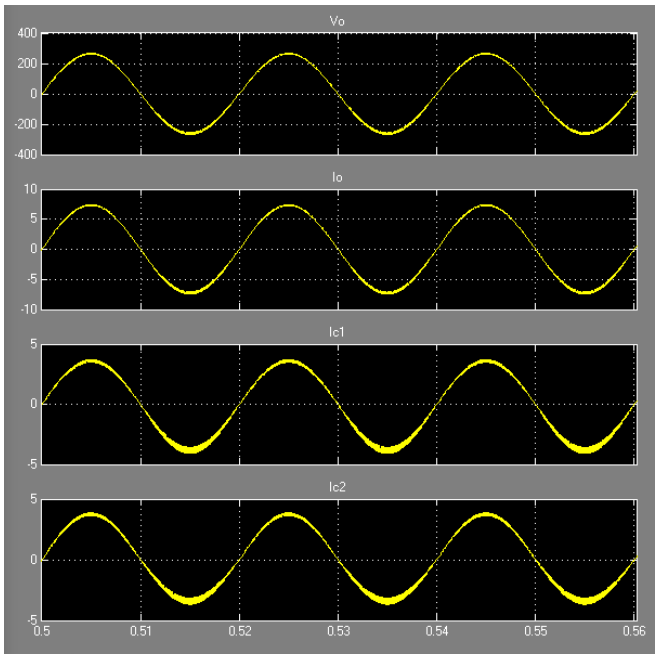
SIMULATION RESULTS



Control method of IDBFTI sim



waveforms of IDBFTI at full load 1



waveforms of IDBFTI at full load 2

CONCLUSION

In this project, a new IDBFTI is proposed, circuit operation is analyzed in detail, and the simulation and experimental verification are conducted. By the theoretical analysis and the simulation results, the proposed topology has the following advantages:

1) It retains the advantages of interleaved parallel technology as follows: promoting the equivalent switching frequency, reducing the switching frequency of parallel unit, reducing the output

current ripple, decreasing the total harmonic distortion of the output current.

2) It retains the advantages of dual buck full-bridge three level inverter as follows: high conversion efficiency, no shoot-through problem, no reverse recovery of body diode. And there is also no circulation current in the inverter, solving the problem of ZSCC in inverter interleaved system by the circuit structure.

3) The interleaved circuits share two power-frequency switches, which can be resized for each specific application, and it is easier to extend the system by improving current capability of the two switches.

The IDBFTI effectively solves the contradiction between the inverter power level and the conversion efficiency, the ripple, the filter of the system, which makes it an excellent candidate in high-reliability and high-efficiency applications, such as grid connected inverters and new energy power generation.

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