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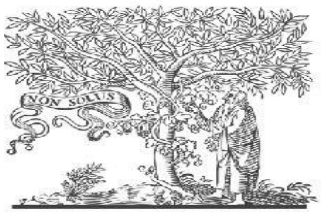

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DESIGN A AREA EFFICIENT RECURSIVE VERY LARGE MULTIUSER COMMUNICATION IN MIMO SYSTEMS

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ABSTRACT: Design a Area Efficient Recursive very large multiuser communication in MIMO Systems is implemented in this project. Initially, multiple inputs are given to the pre iterative block. This pre iterative block will save and control the data in control registers and process the data using processing element array. Now the obtained data will be transferred to the memory unit. CRC (Cyclic Redundancy Check) will check if errors occurred or not. If there are any errors occurred then CRC will detect and correct those errors and again update that data in memory unit. Hence multiple outputs are obtained at last. In this work, implementing 4-bit MIMO system for improving to compile the data at higher rate with Maximum-a-Posterior(MAP) algorithm using Xilinx software, which may be improve Bit Error Rate (BER), reduced area and delay. The system is implemented and correlated in Application Specific Integrated Circuit (ASIC). Time series analysis has been done and output file has been formed

KEY WORDS: CRC (Cyclic Redundancy Check), MIMO (Multiple Inputs Multiple Outputs), control registers, Pre Iterative Block, Memory unit, Minimum Mean Square Error (MMSE).

I. INTRODUCTION

Massive multiple-input multiple-output (MIMO), a key technology, can be used in next-generation wireless communication systems, such as 5G. However, massive MIMO still faces various challenges, and one such challenge exists in uplink massive system signal detection. Data detection in MIMO generally involves low parallelism and high computational complexity, particularly when the number of antennas increases; thus, data detection is a challenging task and computational complexity is extremely high [1]. Consequently, an efficient signal detection

algorithm that satisfies the requirements of low complexity, High parallelism, and high accuracy is considerably important. Maximum likelihood (ML) detection is an optimal detection algorithm.

Nonetheless, the computational complexity notably increases with the number of users and modulation orders, thus preventing the practical application of the ML algorithm. Other nonlinear algorithms, such as K-best, sphere decoding (SD), expectation-propagation detection (EPD), message-passing detector (MPD), and triangular approximate semi definite relaxation (TASER), can achieve near-optimal ML detection performance. However, K-best and SD involve QR decomposition when the channel matrix is large, and these two algorithms are difficult to implement because of their high computational complexities [2-3].

In addition, there are complex low-parallelism iterations in the EPD, MPD, and TASER algorithms. These nonlinear algorithms also require abundant area and power for hardware implementation. Various linear detection algorithms have been proposed to reduce the computational complexity and can be employed in a massive MIMO system with a large but finite number of antennas and a comparatively small number of users. These linear methods can achieve near-optimal performance with relatively low

computational complexity compared with nonlinear methods [4].

Among these linear algorithms, the minimum mean square error (MMSE) is one of the most effective algorithms in reducing computational complexity with minimal detection accuracy loss; consequently, it has significant potential for use in practical massive MIMO systems. However, considering the hardware architecture, MMSE detection involves complicated matrix inversions and multiplications, as well as low parallelism, causing difficulties for hardware implementations with an increasing number of users. This issue limits the application of hardware architectures (detectors) in massive MIMO systems.

Consequently, many methods have been proposed to further reduce computational complexity, improve the parallelism of MMSE and optimize hardware architectures. However, the throughput is limited, and the architecture requires a significant amount of hardware resources. Neumann series approximation (NSA)-based architectures have been proposed to achieve high throughput for massive MIMO detection [5] To achieve a reasonable balance of detection accuracy, throughput, and hardware resource consumption, architectures based on approximation methods, such as the Gauss-Seidel (GS) successive over-relaxation (SOR) weighted Jacobi iteration (WeJi) and Monte Carlo tree search (MCTS) methods, have also been proposed.

However, the computations in the GS, SOR, WeJi, and MCTS methods are difficult to parallelize due to high correlations when estimating each symbol from users. To explore the parallelism between each step, implicit methods have been proposed, including optimized coordinate descent (OCD), parallelizable Chebyshev iteration (PCI) and intra iterative interference cancellation (IIC). However, these implicit methods ignore the unique properties of massive MIMO systems (e.g., channel hardening). Therefore, the same Gram matrix needs to be calculated multiple times, which means that implicit method architectures suffer from higher energy consumption and latency than explicit method.

II. MIMO BACKGROUND

The history of wireless communication started in the late 19th century, with the work of Marconi, Lodge, Popov, Tesla, Hertz and others. With the groundbreaking technology of radio transmissions, it was possible to transmit signals without cables, e.g., between ships or other moving objects. Furthermore, messages could be broadcasted to many people at the same time, in the form of radio and later TV transmissions. During the 20th century, wireless communication has gone through a remarkable development, which has gone hand in hand with the progress in electronic circuit design. Today, there is a large number of wireless communication systems, both public, military and commercial, sharing the available radio resources.

Over the last few decades, there has been an exponential increase in the amount of information being transmitted over the air. Looking at the first commercial mobile wireless networks, they were only providing analog voice services requiring relatively small portions of the radio spectrum. The breakthrough of personal computers, and more importantly the Internet revolution, has dramatically changed the way people use wireless services. Today, consumers are expecting high-speed Internet access in their

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mobile devices, wherever they are, which comes at an increased use of radio spectrum.

The wireless industry foresees that the mobile data traffic will increase by 35 times. In order to support this rapid growth, larger chunks of radio spectrum need to be made available, and at the same time more efficiently used. The challenge of making more efficient use of the radio spectrum has been taken on by researchers at companies and research institutions around the world, and large improvements have been obtained over the last few decades.

A significant breakthrough came in late 1980's when the adaptive use of multiple-input multiple-output antenna (MIMO) systems was proposed. By using multiple antennas at both transmitter and receiver side, it was shown that parallel channels can be created, all using the same radio spectrum. In theory, the channel capacity increases linearly in the minimum of the number of receive and transmit antennas. Another important breakthrough occurred around the same time, which was the invention of turbo codes and iterative decoding. With these new codes, performance close to the Shannon limit can be obtained. The decoding of these codes could be performed iteratively, with several decoding units exchanging information between iterations.

The obtained performance was shown to be close to optimal decoding, but with a realizable complexity as compared to optimal algorithms. Since the discovery of turbo codes, the "turbo principle" has been used to reduce complexity of other tasks in the wireless receiver, e.g., equalization, channel estimation and multi-user detection. These methods have further improved the performance and efficiency of wireless receivers. In the last decade there has been intensive research performed on iterative receivers of various kinds, both for single and multiple antenna systems. The research has provided improvements, and additional understanding, of this type of receivers in various system settings. Furthermore, iterative receivers are already being used in the latest wireless networks being deployed. Never the less, there are still things that have not been fully investigated, e.g., aspects related to low-complexity channel estimation and iterative receiver processing.

III. PROPOSED SYSTEM

The below figure (1) shows the block diagram of proposed system. Initially, multiple inputs are given to the pre iterative block. This pre iterative block will save and control the data in control registers and process the data using processing element array. Now the obtained data will be transferred to the memory unit. CRC (Cyclic Redundancy Check) will check if errors occurred or not. If there are any errors occurred then CRC will detect and correct those errors and again update that data in memory unit. Hence multiple outputs are obtained at last.

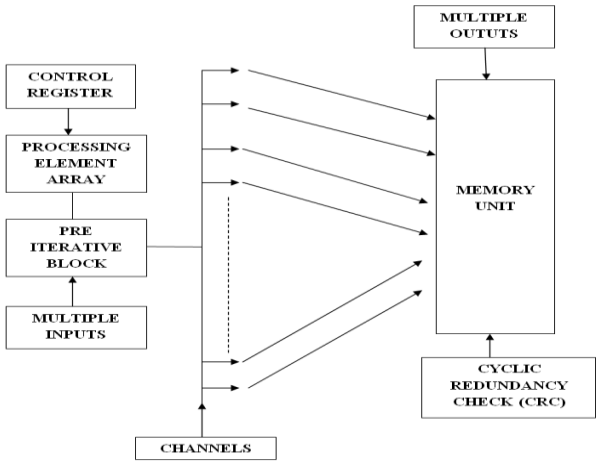

Fig. 1: BLOCK DIAGRAM OF PROPOSED SYSTEM

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A control register is a processor register which changes or controls the general behavior of a CPU or other digital device. Common tasks performed by control registers include interrupt control, switching the addressing mode, paging control, and coprocessor control.
A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data.

Blocks of data entering these systems get a short check value attached, based on the remainder of a polynomial division of their contents. On retrieval, the calculation is repeated and, in the event the check values do not match, corrective action can be taken against data corruption. CRCs can be used for error correction (see bit filters).

CRCs are so called because the check (data verification) value is a redundancy (it expands the message without adding information) and the algorithm is based on cyclic codes. CRCs are popular because they are simple to implement in binary hardware, easy to analyze mathematically, and particularly good at detecting common errors caused by noise in transmission channels. Because the check value has a fixed length, the function that generates it is occasionally used as a hash function.

CRCs are based on the theory of cyclic error-correcting codes. The use of systematic cyclic codes, which encode messages by adding a fixed-length check value, for the purpose of error detection in communication networks, was first proposed by W. Wesley Peterson in 1961. Cyclic codes are not only simple to implement but have the benefit of being particularly well suited for the detection of burst errors: contiguous sequences of erroneous data symbols in messages. This is important because burst errors are common transmission errors in many communication channels, including magnetic and optical storage devices. Typically an *n*-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than *n* bits, and the fraction of all longer error bursts that it will detect is $(1 - 2^{-n})$.

Specification of a CRC code requires definition of a so-called generator polynomial. This polynomial becomes the divisor in a polynomial long division, which takes the message as the dividend and in which the quotient is discarded and the remainder becomes the result. The important caveat is that the polynomial coefficients are calculated according to the arithmetic of a finite field, so the addition operation can always be performed bitwise-parallel (there is no carry between digits).

IV. RESULTS

The below figure (2) shows the RTL schematic of proposed system. Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

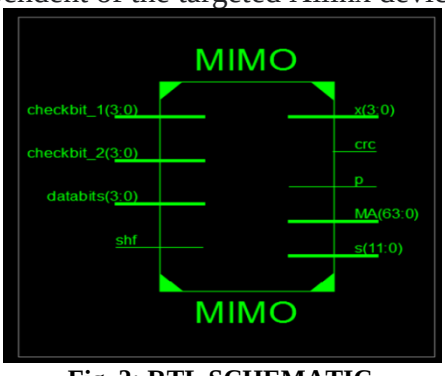

Fig. 2: RTL SCHEMATIC

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The below figure (3) shows the technology schematic of proposed system. Viewing a Technology schematic opens an NGC file that can be viewed as an architecture-specific schematic. This schematic is generated after the optimization and technology targeting phase of the synthesis process. You should always refer to technology schematic for synthesized result.

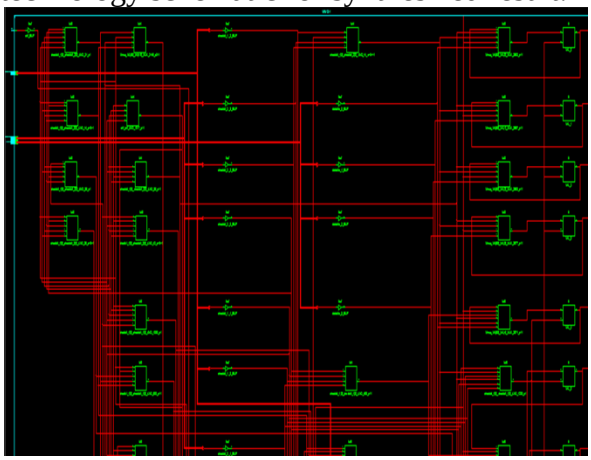

Fig. 3: TECHNOLOGY SCHEMATIC

The below figure (4) shows the output waveform of proposed system.

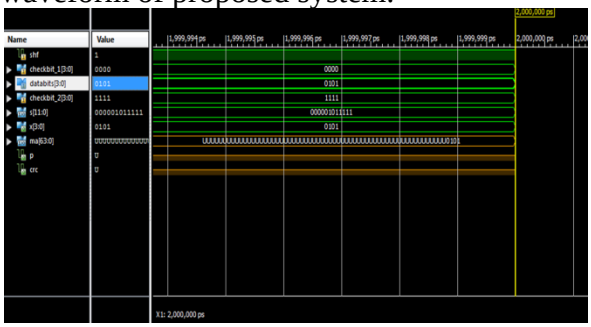

Fig. 4: OUTPUT WAVEFORM

V. CONCLUSION

Hence in this project, design a Area Efficient Recursive very large multiuser communication in MIMO Systems was implemented. By using MIMO there will be increasing number of user. Hence the proposed structure will produces best reliability and area when compared to existed system In future we can extend this project to 128,256,512,1024, etc the number of bits. This project can be implement in backend tools like Tanner tools, Mentor Graphics by using GDI(Gate diffusion input) Technology and as well as in hardware technology also.

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