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**Paper Authors** 

### CH.PALLAVI, C.PADMA

Sri Venkateswara Engineering College for Women, A.P., India





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# A NOVEL APPROACH FOR DESIGN & IMPLEMENTATION OF TRAFFIC LIGHT CONTROLLER SYSTEM USING FPGA

CH.PALLAVI<sup>1</sup>, C.PADMA<sup>2</sup>

<sup>1, 2,</sup> Assistant Professor, Department of ECE, Sri Venkateswara Engineering College for Women, A.P., India

<sup>1</sup>Pallavi.ch@svcolleges.edu.in, <sup>2</sup>padmasekhar85@gmail.com

#### **Abstract:**

Growing numbers of road users and the limited resources provided by the current infrastructures lead to cause more accidents in urban cities. Traffic light control systems are widely used to monitor and control the flow of vehicles through the junction of many roads. The Traffic Light Controller is designed to generate a sequence of digital data called switching sequences that can be used to control the traffic lights of a typical four roads junction in a fixed sequence [2]. It is also proposed to implement the day mode and night mode operations. It plays more and more important role in modern management and control of urban traffic to reduce the accident and traffic jam in road. Therefore this paper mainly focuses on the aspect of traffic lights control in order to reduce the congestion and thereby reducing the negative impact of transport facilities in urban environment. The methods that are used in this project are design the circuit, write a coding, simulation, synthesis and implement in hardware. In this project, XILINX Software was chosen to design a schematic using schematic edit, writes a coding using Verilog HDL (Hardware Description Language) text editor and implemented the circuit on Field Programmable Gate Array [FPGA] Device.

Key words: Congestion, Traffic light controller, XILINX, Verilog, FPGA.

#### 1 INTRODUCTION:

Now a days Traffic congestion is a severe problem in many modern cities around the world. Traffic congestion has been causing many critical problems and challenges in the major and most populated cities. To travel to different places within the city is becoming more difficult for the travelers in traffic. Due to these congestion problems, people lose time, miss opportunities, and get frustrated. Traffic congestion directly impacts the companies. Due to traffic congestions there is a loss in productivity from workers, trade opportunities are lost, delivery gets delayed, and thereby the costs goes on increasing. To solve these congestion problems, we have to build new facilities & infrastructure but at the same time make it smart. Therefore many

countries are working to manage their existing transportation systems to improve mobility, safety and traffic flows in order to reduce the demand of vehicle use. Therefore, many researches about traffic light system have been done in order to complicated overcome some phenomenon but existent research had been limited about present traffic system in well-travelled traffic scenarios. The time of allocation is fixed from east to west or opposite way and from north to south way in cross roads [1]. Field Programmable Gate Arrays (FPGAs) are extensively used in rapid prototyping and verification of a conceptual design. FPGA implementation advantageous over **ASIC** microcontroller; number of IO ports and performance compared to microcontroller



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and implementation with FPGA is less expensive compared to ASIC design. The design flow of FPGA is given in the following flow diagram. Fig 1.1 shows the simplified version of FPGA design flow.

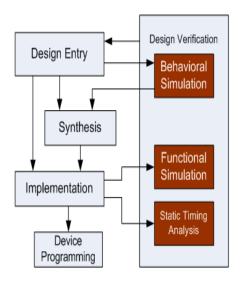


Fig 1.1 FPGA Design Flow

## 2. DESIGN OF TRAFFIC LIGHT CONTROLLER:

Traffic Light Controller can be designed starting with some arbitrary assumptions. At first the North traffic will be allowed to move and then traffic in the East, South and West direction will be allowed to move in sequence. The advantage of writing Traffic Light Controller program is that in a program, modifications as per requirements can be done easily i.e., suppose the traffic on main road should be allowed for more time and for side roads the traffic should be allowed for less time; then the clock is divided in such a way that for main road the clock period will be more and for side roads the clock period will be less, this is because the main road traffic is heavy when compared to the side road traffic[5]. In general TLC System will be having three lights (red, green and yellow) in each direction where red light stands for traffic to be stopped, green light stands for traffic to be allowed and yellow light stands for traffic is going to be stopped in few seconds[4]. The fig. 2.1 shows the flow chart for traffic light controller system.

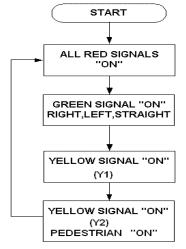


Fig 2.1 TLC (Traffic Light Controller)
Flow Chart

## 2.1 EXPLANATION OF TRAFFIC LIGHT CONTROLLER

The Fig 2.2 shows the Traffic Signals at Junction. In this structure, there are four traffic signals, represented by R1, R2, R3 and R4 to be controlled. All the four signals have same priority as they all are main roads.

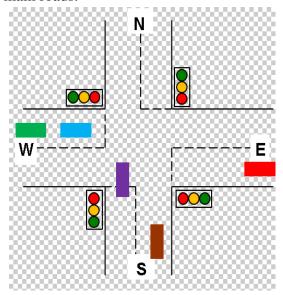


Fig 2.2 Traffic Signals at Junction



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First of all the signal controller is in the reset mode where in the signal of road (R1) is green whereas all the other roads R2, R3 and R4 are red. This state we have assigned as S0. Later the controller sends the control to state S1 where the R1 is yellow whereas all the other signals are still red only. In this state the controller checks whether the sensor at road R2 which is X2 is low or not. If the sensor gives a low signalling that there is no traffic on that road, then that signal on road R2 is skipped transferring control to the state S4 where signal on road R3 is turned whereas rest of the signals are showing red. On the hand if the traffic is present on the road R2 then the control is sent to state S2 which switches on the signal on road R2 to green and rest of the signals are red only when the control is with state S2 after showing the green signal the signal light changes from green to yellow for signal on the road R2 while all the other signals continue to be in red light mode only which is the operation of state S3.Again when the controller is in state S3 it checks for the response of sensor X3 on road R3. If the output of sensor is low the control of the system will be transferred to state S6 skipping the the on working of signal R3 otherwise the control is given to corresponding next state S4. When in S4 the traffic signal of road R3 turns green on the other hand the signals of roads R1, R2 and R4 remain red itself. The control is then transferred to state S5. When the control is with state S5 it checks for the output of the sensor X4 on the road R4. Depending on the output of X4 the further state change takes place accordingly. If low then the control is transferred to state S0 skipping the operation of the signal on

road R4 otherwise the control is with the S6. When the controller is in state S5 there is change of signal on road R3 from green to yellow. When the control is with state S6 the signal of road R4 turns green whereas all the signal turn or remain in red signal only. Thee control is then shifted to state S0. In state S7 the signal of road R4 from turns green to yellow. Simultaneously the sensor on the first road R1 which is X1 is checked for its output. If the signal is low then the control is shifted direction directly to state S2 otherwise the control is shifted to default state S0. These states are not mandatory. The number of states, the order of the lights and the delay can be specified by the user. This is one of the most advantages in this project [3&6].

#### 2.2 TLC STATE DIAGRAM

The TLC state diagram shown in Fig 2.3 illustrates that whenever count=00 and direction=00,then green light in north direction will be ON for few seconds and red signal light in all other directions namely west, south and east will be ON[8]. When count=01 and direction=00 then yellow light (y1) will be ON for few seconds and when count=01 yellow light (y2) and pedestrian north will be ON and then direction is incremented by one and count is assigned to zero. So when count=00 and direction=01, the green light in east direction will be ON for few seconds and all red lights in other direction Whenever be ON. count=01 direction=01 then yellow light (y1) will be ON for few seconds and when count=01 yellow light (y2) and pedestrian east will be ON and then direction is incremented by one and count is assigned to zero.



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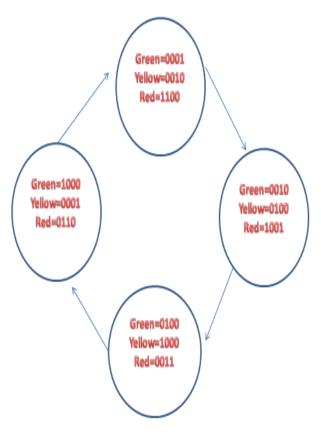


Fig 2.3 TLC State Diagram

So whenever count=00 and direction=10, the green light in south direction will be ON for few seconds and all red lights in other directions will be ON. Whenever count=01 and direction=10 then yellow light (y1) will be ON for few seconds and when count=01 yellow light (y2) and pedestrian south will be ON and then direction is incremented by one and count is assigned to zero. So whenever count=00 and direction=11, the green light in west direction will be ON for few seconds and all red lights in other directions will be ON. Whenever count=01 and direction=11 then yellow light (y1) will be ON for few seconds and when count=01 yellow light (y2) and pedestrian west will be ON and then direction is assigned to 00 and count is assigned to zero. This sequence repeats and the traffic flow will be controlled by assigning time periods in all the four directions [7].

## 3. SIMULATION RESULTS: 3.1 RTL SCHEMATIC

The below figure shows the RTL Schematic of the Traffic Light Controller.

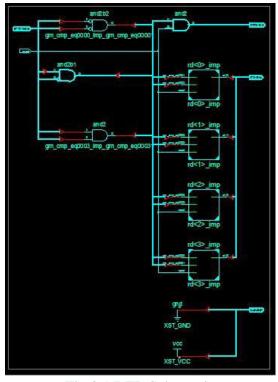


Fig 3.1 RTL Schematic

#### 3.2 TECHNOLOGY SCHEMATIC

The below figure shows the Technology Schematic of the Traffic Light Controller.

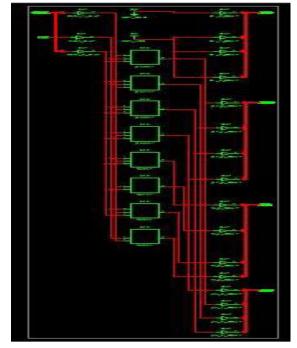


Fig 3.2 Technology Schematic



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#### 3.3 WAVE FORM

The below figure shows the Wave form of the Traffic Light Controller when the test bench is applied to the source code.

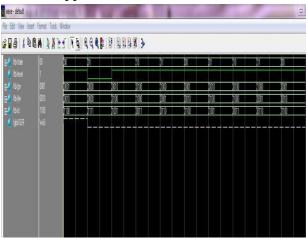


Fig 3.3 Wave Form

#### 4. HARDWARE IMPLEMENTATION

Fig. 4.1 depicts a general four road structure which consists of north, east, west and south directions each with a set of three lights namely green, yellow and red. Green light in a direction will be ON when left, straight and right side is set to be free for traffic in that direction.

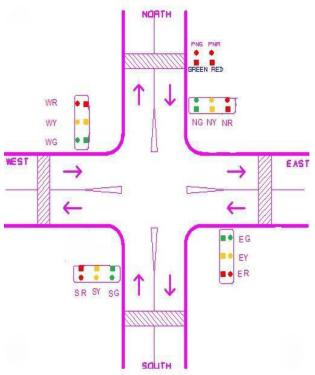


Fig 4.1 Structure of Road

The figure shows the design of traffic light model. To distinguish each lane and the traffic signal lights, they are labeled separately with North, East, South and West. Signal lights at each lane have their set of traffic light signal "Red, Yellow, and Green". Operation of this signal light is similar to common traffic light signal. Along with these specifications, each lane has a light to represent a sensor of the corresponding road. Linear sensor or electromagnetic sensor is suitable for design of a real traffic light system. The first sensor detects the presence of vehicles and the second sensor determines the volume of the traffic corresponding to that lane [9]. Through the two sensors, we will know the expected time for green signal ON and when the signal light at each lane should be changed to green. The state machine is coded using the Hardware Description Language, Verilog. Spartan-3E trainer kit is shown in Fig. 4.2.



Fig 4.2 Spartan-3E trainer kit



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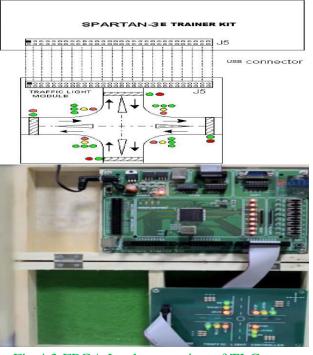


Fig 4.3 FPGA Implementation of TLC

Fig. 4.3 shows the FPGA Implementation of TLC. Using Xilinx ISE tool, this code is dumped into Spartan-3E FPGA trainer kit and the outputs here we considered are more than the LEDs on the FPGA.

#### 5. IMPLEMENTATION RESULTS

The Traffic Light Controller was designed using Verilog HDL and was implemented using FPGA. The output of the TLC is verified with NEXYS 2 FPGA. Fig 5.1 shows the following were the results taken by us after the implementation.



Fig 5.1 Display output for the symbol Red

## 6. CONCLUSION AND FUTURE SCOPE:

The modern ways of multi-way traffic management improves the traffic condition up to a large extent. Advanced signaling controllers contribute to the improvement of the urban traffic; which is proportional to the complexity of the controller. These more complex controllers can be well handled using states machines. Methods to reduce the states in the state machine also help in reducing the required hardware thus leading to low power and area efficient design. The future scope of this project is it can be directly applied in real time by employing more number of such circuits. This work can be further extended to further FPGA families to implement speed grade and with aurdino processors and raspberry pi for improvement of parameters like speed for better performance.

#### **REFERENCES:**

[1] Swetha, G. sai priyanka "prathyusha Mahesh shetkar "Design of Real-Time Traffic Control System using Verilog" 2017 ISSN 2322-0929 El-Medany, W.M., & Hussain, M.R. (2007) FPGA-Based Advanced Real Traffic Light Controller System

[2] Design. Proceeding of 4th IEEE International Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications, ISBN: 978-1-4244-1347-8, pg. 100 − 105.
[3] Chan, S.S., Deshpande, R.S. & Rana, J.G. (2009) Design of Intelligent Traffic Light Controller Using □Embedded System. □Proceeding of 2nd International Conference on Emerging Trends in Engineering and Technology, ISBN: 978-1-4244-5250-7, pg. 1086-1091 [4] Liu, Y. & Chen. X. (2009) Design of Traffic



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Lights Controlling System Based on PLC and Configuration Technology. □Proceeding of International Conference on Multimedia Information Networking and Security 2009, ISBN: 978-0-7695-3843-3, pg. 561-563.

- [5] Kulkarni, G.H. & Waingankar, P.G.
  (2007) Fuzzy logic based traffic light controller. Proceeding of International Conference on Industrial and Information Systems 2007, ISBN: 978-7-4244-1151-1.
  [6] Norhuzaimin, J. & Maimun, H.H.
- [6] Norhuzaimin, J. & Maimun, H.H. (2005) The Design of High Speed UART. Proceeding of Asia Pacific Conference on Applied Electromagnetics, ISBN 0-7803-9431-3, pg. 306-310. [7] STEPHEN BROWN, JONATHAN ROSE, "FPGA and CPLD architectures: A Tutorial," Design & Test of Computers, IEEE, Volume 13, Issue 2, summer 1996 Page(s):42 57.
- [8] Parasmani, Shri Gopal Modani, "FPGA-Based Advanced Traffic Light Controller Simulation", International Journal of Scientific & Engineering Research, Volume 4, Issue 9, September-2013.
- [9] B. Dilip, Y. Alekhya, P. Divya Bharathi, "FPGA Implementation of an Advanced Traffic Light Controller using Verilog HDL" International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 1, Issue 7, September 2012.

[10]Parag K. Lala, "Digital System Design Programmable Logic Devices", Page15-17, Chapter 1, B S Publications