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Volume 07, Issue 12, Pages: 17–25.
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# DESIGN OF LOW POWER HIGH SPEED HYBRID CMOS FULL ADDER

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## Abstract
In this paper, a proposed 1-bit hybrid full adder design employing both transmission gate logic and complementary metal–oxide–semiconductor (CMOS) logic is reported. The design is implemented for 1-bit Ripple Carry Adder and then is extended for 64-bit Ripple Carry Adder. The circuit is implemented using Mentor Graphics tools 130nm technology. The performance parameters such as delay, area, total power dissipation and power delay product (PDP) were compared with the existing designs such as Conventional CMOS full adder (CMOS), Complementary pass transistor logic (CPL), Transmission function full adder (TFA), HPSC full adder and Low Energy HPSC full adder with proposed 1-bit hybrid full adder and modified 1-bit hybrid full adder. For 1V supply at 130-nm technology, the average power consumption is found to be extremely low with moderately low delay resulting from the deliberate incorporation of very weak CMOS inverters coupled with strong transmission gates. The design is further extended for 32-Bit and 64-bit full adder also, and is found to be working efficiently with less delay and less power dissipation at 130-nm technology for 1V Supply voltage. In comparison with the previous full adder designs, the hybrid adder offers significant improvement in terms of power, area and speed.

**Keywords** XNOR, Hybrid Adder Design, Ripple Carry Adder, Low power, Power Delay Product (PDP).

## I. Introduction
The adders play an important role in complex arithmetic and computational circuits such as multiplier, comparator and parity checkers. In recent years, many approaches have been proposed to implement a low power full adder. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector. Adder is the basic building block of complex arithmetic circuits like addition,

multiplication, division, exponentiation and so forth. The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths) and the intra cell wiring capacitances. Circuit size depends upon the number of transistors, their sizes and on the wiring complexity. Some use one logic design for the whole full adder while the other uses more than one logic design for their implementation. Power is one of the vital resources, hence the designers try to reduce the power while designing a system. Power dissipation depends upon the switching activity, node capacitances (made up of gate, diffusion, and wire capacitances), and control circuit size. By selecting proper W/L ratio can be minimize the power dissipation without decreasing the supply voltage. Different logic designs tend to favor one performance aspect at the expense of others. In this paper, a proposed 1-bit and modified 1-bit hybrid full adders are designed. The proposed hybrid full adder consists of XNOR and Carry generation module. The XNOR module is responsible for most of the power consumption of the entire adder circuit. For the proposed hybrid full adder, 6 transistor XNOR circuit and for modified hybrid full adder, 4 transistor XNOR circuit is used. Comparing with the existing adders CMOS, TFA, HPSC and LEHPSC the characteristics of the proposed and modified hybrid full adder shows that the design has the best delay, PDP, total power dissipation and area. Due to the minimum delay, the adder core greatly improves the overall performance for a large scale of a multi-bit adder. This paper is organized as following: Section-II describes the previous full adder designs. Section-III describes the design of proposed and modified hybrid full adder and the implementation of 64-bit Ripple carry adder. Section-IV shows the simulation results in mentor graphics tools (130nm). Finally, in section-V conclusions are presented.

## II. Previous Work

Various low-power full adders with output driving capability have been presented in literature [2]-[7]. By applying the principle of mirror, the conventional CMOS full adder (denoted as CMOS) is realized as shown in Fig. 1 [2]. In this design, the PMOSnetwork is fully identical to the NMOS-network rather than being the conduction dual. The fully symmetric schematic topology significantly simplifies the layout design. This configuration consumes smaller power, yet its drawback comes from slower speed due to the node C0 having to drive heavy load. The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers.

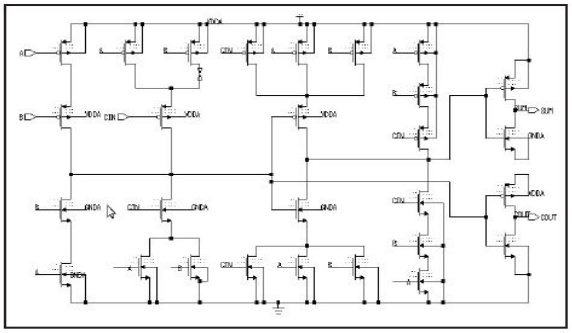

Fig. 1: Conventional CMOS Full Adder

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Based on transmission gates, Fig. 2 shows a full adder with driving capability [2], since the transmission full adder, denoted as TFA has simpler schematic than the conventional CMOS full adder shown in Fig. 1. The TFA needs fewer MOS transistors in comparison with the previous one. The transistor count of TFA is 26, while the conventional CMOS full adder requires 28 transistors. TFA provides buffered outputs of the proper polarity for both sum (S) and carry-out (Co). Its disadvantage is slow speed and high power consumption.

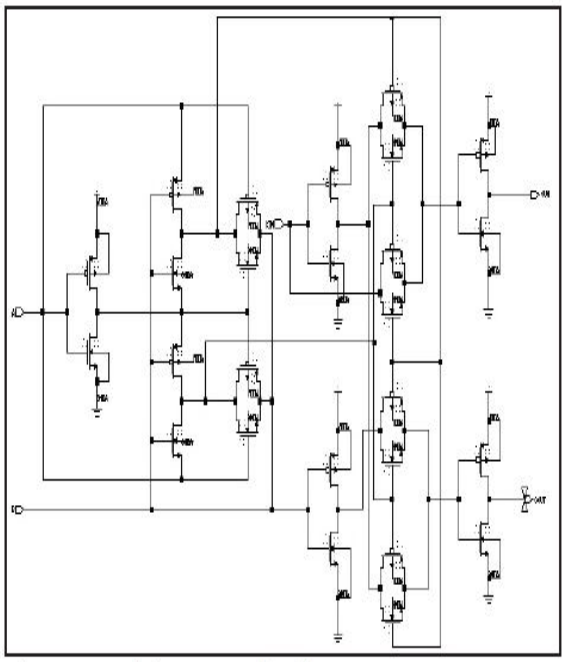

Fig. 2: Transmission Gate Full Adder

Fig. 3 shows pass transistor logic (PTL) full adder [3]. Here the use of exclusive-OR and exclusive-NOR (XOR/XNOR) with the full voltage swing output, the PTL-based full adder (PTLA) could operate at full-swing signal voltage and needs less MOS transistors. However, the pull-up and pull-down transistors in XOR/XNOR module cause too much delay and drive too much loading. As a result, the whole full adder is slower down and consumes more power.

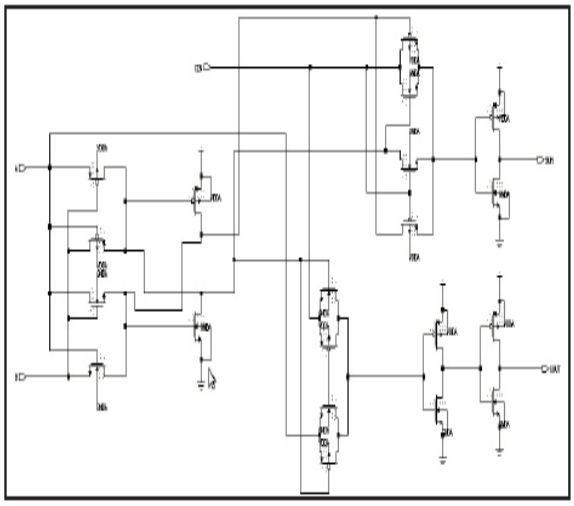

Fig. 3: PTL Based Full Adder

Its advantage is that one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function, which results in lower number of transistors and smaller input load. Moreover, direct -to-ground paths, may lead to short-circuit energy dissipation. The complementary pass-transistor logic (CPL) full adder has 32 transistors and is based on the CPL logic. A CPL logic full adder circuit is shown in Fig. 4. In this circuit, there are two small pull-up PMOS transistors for swing restoration in the Sum output signal and the complementary Sum output signal and another two small pull-up PMOS transistors for swing restoration in the Carry output signal and the complementary Carry output signal [2]. CPL full adder provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors. Due to the presence of lot of internal nodes and static inverters, there is

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large power dissipation [3].

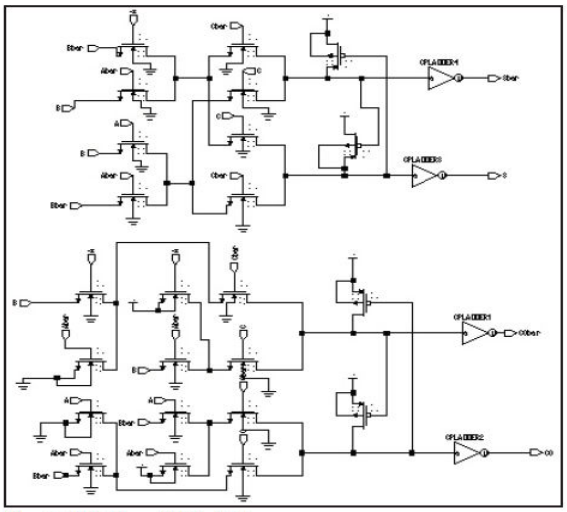

Fig. 4: CPL Based Full Adder

A hybrid pass-logic with static CMOS output drive full adder (HPSC) is proposed to feature hybrid CMOS logic style, as shown in Fig. 5 [2]. In HPSC circuit, XOR and XNOR functions are simultaneously generated by pass-logic module with only six transistors, and propagated to the successive CMOS module to produce full-swing outputs. Two complementary transistors form the feedback loop to overcome the weak signals caused by pass transistors, they restore the non full-swing output by either pulling it up through PMOS to supply voltage or down through NMOS to ground.

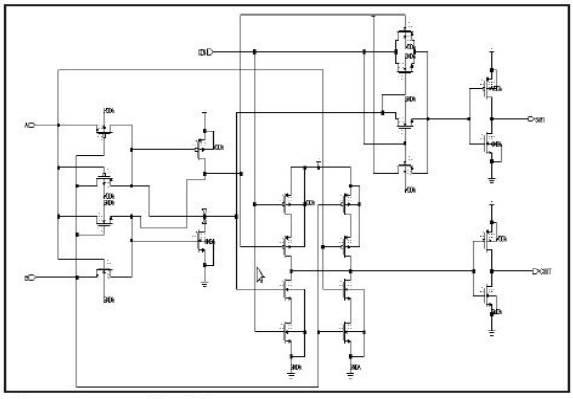

Fig. 5: HPSC Full Adder

Due to the need of restoring and driving both modules for sum and carry-out, the pass-logic module eliminate the whole propagation delay of the full adder. The circuit is shown in Fig. 6 [2] and similar to Fig. 5 circuit architecture except for a XOR-XNOR design. The characteristics of Fig. 1 to Fig. 6 will be compared with the proposed hybrid full adder and modified hybrid full adder for reference.

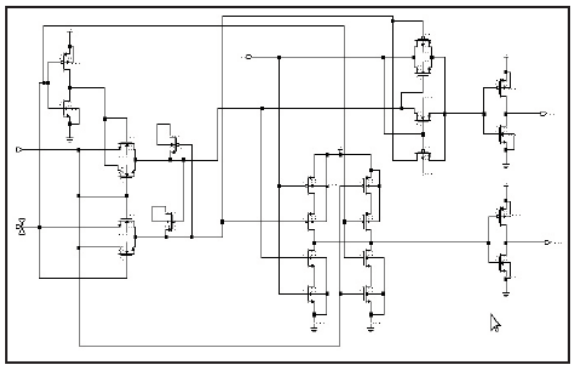

Fig. 6: Low-Energy Hybrid Full Adder

## III. Hybrid Adder

The proposed full adder circuit is represented by three blocks as shown in Fig. 7(a). Module 1 and module 2 are the XNOR modules

that generate the sum signal (SUM) and module 3 generates the output carry signal (Cout). Each module is designed individually such that the entire adder circuit is optimized in terms of power, delay, and area. These modules are discussed below in detail.

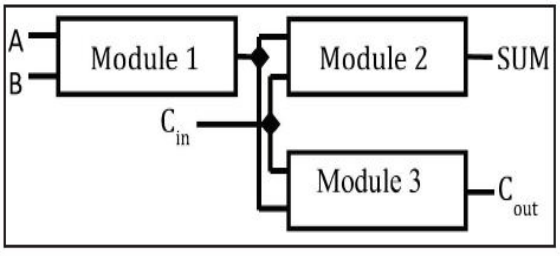


Fig. 7(a): Schematic Structure of Proposed Hybrid Full Adder

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### A. Modified XNOR Module

In the proposed full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extent with avoiding the voltage degradation possibility. Fig. 7(b) shows the modified XNOR circuit where the power consumption is reduced and full swing of the levels of output signals is guaranteed by level restoring transistor. Various XOR/ XNOR topologies have already been reported. To the contrary, the XOR/XNOR uses six transistors to get better logic swing compared with previous XOR/XNOR circuits. The modified XNOR presented in this paper offers low-power and high-speed (with acceptable logic swing) compared with the existing XOR/ XNOR circuits.

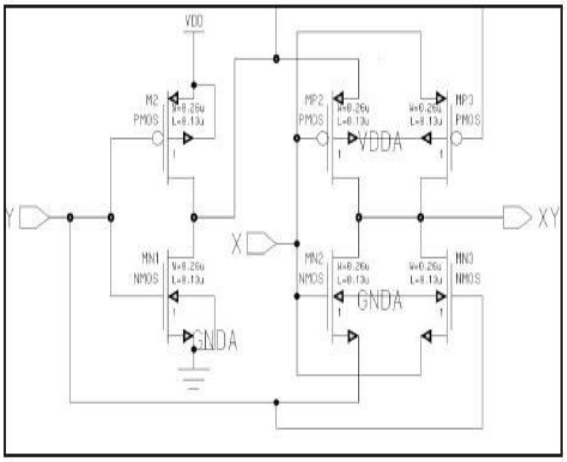


Fig. 7(b): XNOR Module

### B. Carry Generation Module

Here, the output carry signal is implemented as shown in Fig. 7(c). The input carry signal (Cin) propagates only through a single transmission gate, reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates guaranteed further reduction in propagation delay of the carry signal.

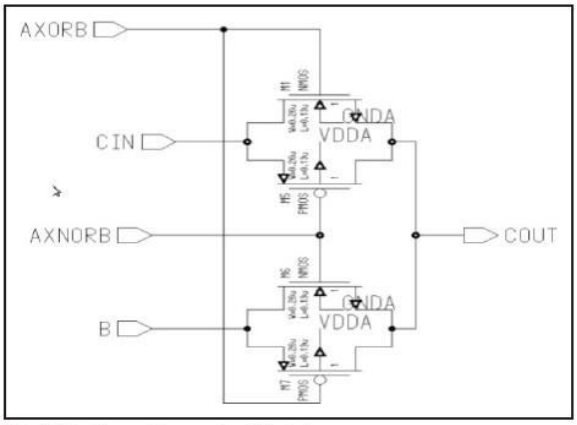


Fig. 7(c): Carry Generation Module

### C. Operation of the Proposed Full Adder With Simulation Wave Forms

Fig. 8 shows the detail diagram of the proposed full adder. The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B, which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2.

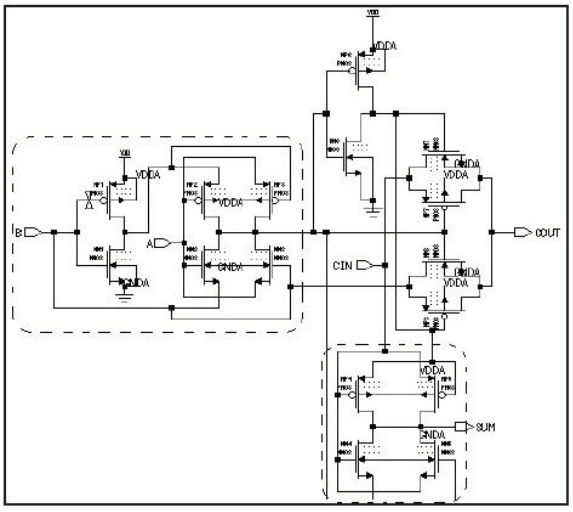


Fig. 8: Proposed 1-Bit Hybrid Full Adder

Output of this controlled inverter is basically the XNOR of A and B, but it has some

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voltage degradation problem which has been removed using two pass transistors Mp3 and Mn3. PMOS transistors (Mp4, Mp5, and Mp6) and NMOS transistors (Mn4, Mn5, and Mn6) realize the second stage XNOR module to implement the complete SUM function. Analyzing the truth table of a full adder, the condition for Cout generation has been deducted as follows:

If A=B, then Cout= B else, Cout= Cin. The parity between inputs A and B is checked by A⊕B function. If they are equal, then Cout is same as B which is implemented using the transmission gate, realized by transistors Mp8 and Mn8. Otherwise, the input carry signal (Cin) is reflected as Cout which is implemented by another transmission gate consisting of transistors Mp7 and Mn7. It is likely that a single bit adder cell designed for optimum performance may not perform well under deployment to real time conditions. This is because when connected in cascaded form, the driver adder cells may not provide proper input signal level to the driven cells. The cumulative degradation in signal level may lead to faulty output and the circuit malfunction under low supply voltages. The simulated wave form of the proposed 1-bit hybrid full adder is shown in Fig. 8(a).

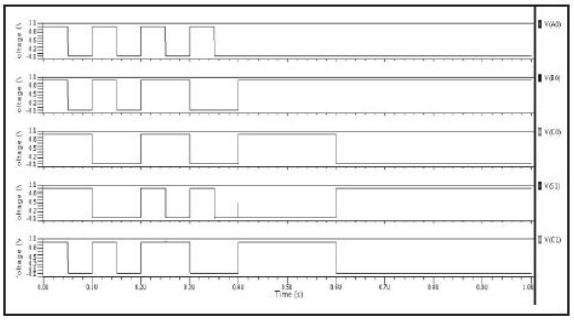

Fig. 8(a): Simulated Output Waveforms of Proposed 1-bit Hybrid Full Adder

**D. Performance Analysis of the Proposed Full Adder**

The simulation for the proposed full adder is carried out using 130-nm technology and compared with the other potential adder designs. With an aim to optimize both power and delay of the circuit, the power-delay product (PDP) that is, the energy consumption has been minimized in the proposed case. It is observed that in the present design, the power consumption could be minimized by mainly sizing the transistors in inverter circuits while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates present between the paths from Cin to Cout. Power consumption, propagation delay and PDP of the proposed full adder are compared along with that of previous full adders respectively. The proposed hybrid full adder is also been compared with other hybrid full adders reported in [2]-[4]. The circuits of the hybrid full adder reported were simulated in Mentor Graphics tools in 130nm technology. The proposed hybrid adder [1] requires only 16 transistors whereas the other hybrid adders [2] require more than 20 transistors. The average power consumed by the proposed full adder is significantly lower than that of other hybrid full adders. The use of less number of transistors improves the speed of the circuit. Because of reduction in average power consumption and propagation delay, the PDP of the proposed hybrid full adder is significantly improved in comparison with the earlier hybrid adders.

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**E. Calculation of Area of 1-bit Adder**

Fig. 8(b) shows the layout of the proposed full adder in mentor graphics tool 130-nm technology.

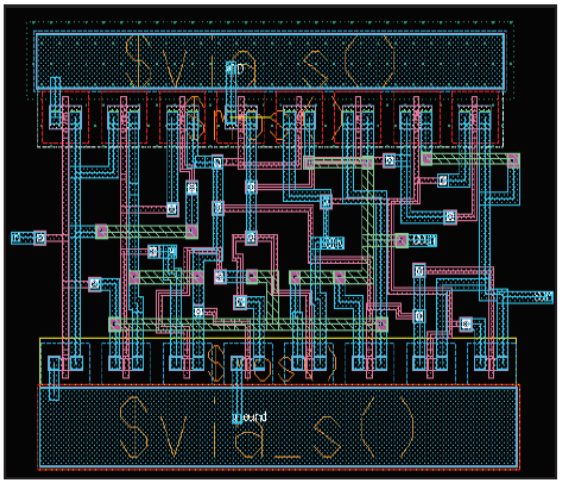

Fig. 8(b): Layout of Proposed 1-Bit Hybrid Full Adder

The area for proposed 1-bit hybrid full adder is 13.69 µm × 9.70 µm in 130-nm technology. The number of transistors for the proposed hybrid full adder is 16. With an aim to enhance the performance of the proposed full adder in terms of power consumption and delay, the design requires strong transmission gates and weak inverters. The main concern of the proposed adder design was minimization of PDP.

**F. Modified 1-bit Hybrid Full Adder**

Full adder has been derived with various structures previously to reduce the power dissipation, delay, PDP and area reduction. To analyze the different parameters of the adders a structure of a hybrid full adder is modified by reducing two transistors in XNOR circuit because XNOR module is responsible for most of the power consumption of the entire adder circuit. In the proposed hybrid adder the 6 transistors XNOR module is replaced with 4 transistors XNOR module, which gives better performance than the previous hybrid adders.The modified hybrid 1-bit full adder is shown in Fig. 9 and the corresponding output wave forms and layout are shown in Fig. 9(a) and Fig. 9(b).

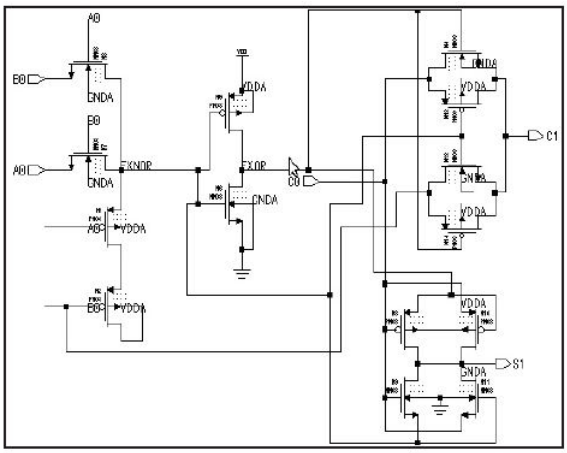


Fig. 9: Modified 1-Bit Hybrid Full Adder

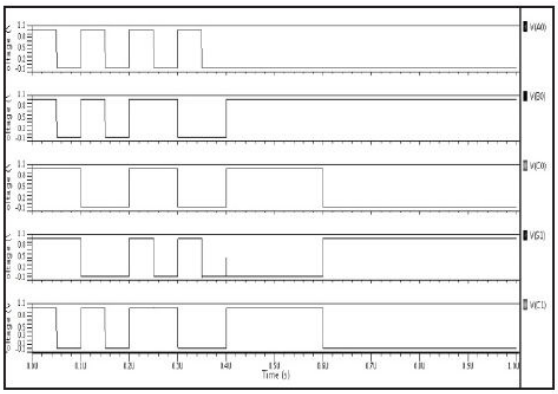

Fig. 9(a): Simulated Output Waveforms of Modified 1-Bit Hybrid Full Adder

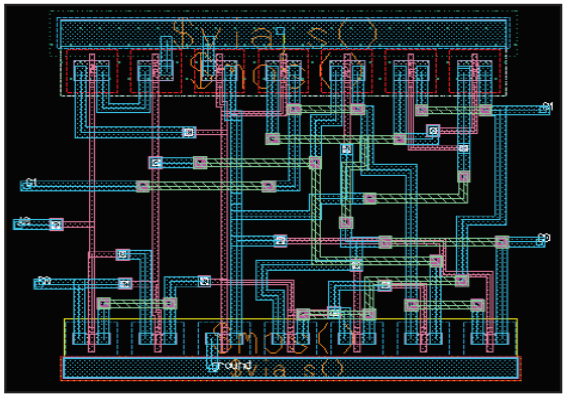

Fig. 9(b): Layout of Modified 1-Bit Hybrid Full Adder

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The area for modified 1-bit hybrid full adder is 12.46 µm × 9.60 µm in 130-nm technology, which is less than the area of the proposed 1-bit hybrid full adder.

## IV. Simulation Results

Table 1: Simulation Results for Proposed Hybrid Full Adder Model using Ripple Carry Adder in 130nm Technology with 1 V Supply Voltage

| Proposed Hybrid adder | Total Power Dissipation | Delay | PDP | Area | No. of Transistors |
|---|---|---|---|---|---|
| 1-bit | 302.97 PW | 196.455PS | 59.52 ZS | 13.69 µm × 9.70 µm | 16 |
| 4-bit | 1.211 NW | 449.44 PS | 544.27 ZS | 75.09 µm × 9.63 µm | 64 |
| 8-bit | 2.424 NW | 1.038 NS | 2.52 AS | 159.46 µm × 9.82 µm | 128 |
| 16-bit | 4.848 NW | 3.671 NS | 17.80 AS | 160.41 µm × 10.05 µm | 256 |
| 32-bit | 9.695 NW | 12.262 NS | 118.90 AS | 162.34 µm × 51.72 µm | 512 |
| 64-bit | 19.390 NW | 24.26 NS | 470.40 AS | 163.34 µm × 111.26 µm | 1024 |

Table 2: Simulation Results for 1-Bit Full Adders in 130nm Technology with 1 V Supply Voltage

| Design | Total Power Dissipation | Delay | PDP | No. of Transistors |
|---|---|---|---|---|
| CPL | 10.45 NW | 0.365 NS | 3818.12 ZS | 32 |
| CCMOS | 4.53 NW | 0.457 NS | 2071.48 ZS | 28 |
| TFA | 5.196 NW | 0.352 NS | 1830.07 ZS | 26 |
| PTL | 3.879 NW | 0.416 NS | 1616.85 ZS | 20 |
| HPSC | 3.853 NW | 0.376 NS | 1450.35 ZS | 22 |
| LEHPSC | 5.022 NW | 0.378 NS | 1899.89 ZS | 24 |
| Proposed Hybrid adder | 0.302 NW | 0.196 NS | 59.52 ZS | 16 |
| Modified Hybrid adder | 0.165 NW | 0.104 NS | 17.31 ZS | 14 |

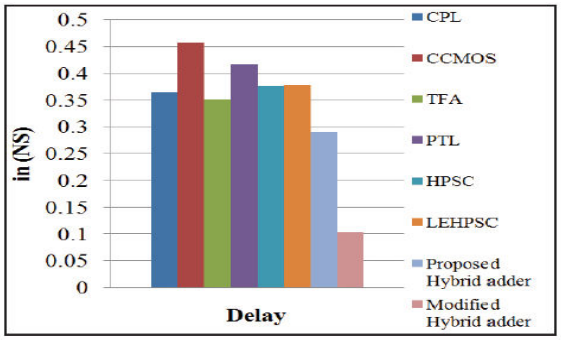


Fig. 10: Comparison of Delay of various full adder designs

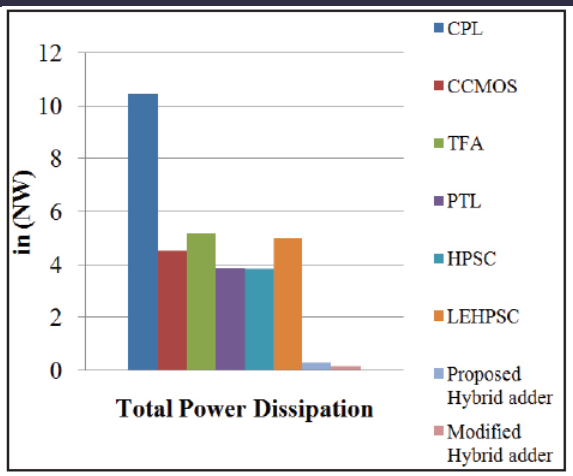


Fig. 11: Comparison of Total Power dissipation of various full adder designs

## V. Conclusion

In this Project, a low-power 1-bit hybrid full adder has been proposed and the design has been extended for 64-bit Ripple Carry Adder (RCA). The simulations are carried out using Mentor graphics tools with 130-nm technology and are compared with other standard design approaches like CMOS, CPL, TFA, HPSC and LEHPSC designs. The simulation results shows that the proposed adder offers improved PDP compared with the earlier reports. The efficient coupling of strong transmission gates driven by weak CMOS inverters lead to fast switching speeds. The proposed full adder offered improvement with respect to the existing design in terms of PDP (130-nm technology at 1 V). The Modified Hybrid adder has achieved 98.42% of power reduction and 71.50% of delay reduction compared to the adder designed by CPL.

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