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SIGN MAGNITUDE ENCODING FOR EFFICIENT VLSI REALIZTION OF DECIMAL MULTIPLICATION

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ABSTRACT
This paper proposes a low power technique, called SBR (Sign Bit Reduction) which may reduce the switching activity in multipliers as well as data buses. Utilizing the multipliers based on this scheme, the dynamic power consumption of some digital systems such as digital filters based on CMOS logic system can be reduced considerably compared to those based on 2's complement implementation. To verify the efficacy of the SBR, a 16-bit multiplier was implemented by this scheme. The results for voice data show an average of 29% to 35% switching reduction compared to the 2's complement implementation. For 16-bit random data, this scheme decreases the switching of 16-bit multipliers by an average of 21%. Finally, the application of the technique to a 16-bit data bus leads up to 14.5% switching reduction on average.

Keywords: Switching Activity, Low Power, Signed Multiplier, Bus Encoding, Sing Extension.

1. INTRODUCTION
Decimal math equipment is exceptionally requested for quick preparing of decimal information in money related, Web-based, and human intelligent applications. Quick radix-10 increase, specifically, can be accomplished by means of parallel halfway item age (PPG) and incomplete item decrease (PPR), which is, in any case, profoundly territory expending in VLSI usage. Along these lines, it is wanted to bring down the silicon cost, while keeping the rapid of parallel acknowledgment. Let P = X × Y speak to a n × n decimal augmentation, where multiplicand X, multiplier Y , and item P are ordinary radix-10 numbers with digits in [0 , 9].

Such digits are regularly spoken to by means of double coded decimal (BCD) encoding. In any case, middle halfway items (IPPs) are spoken to by means of a decent variety of frequently repetitive decimal digit sets and encodings (e.g., [0 , 10] convey spare (CS), [0 , 15] over-burden decimal, [− 7 , 7] marked digit (SD), twofold 4, 2, 2, 1, and [− 8 , 8] SD). In the recent years, the rapid increase in the complexity of chips and the popularity of portable and mobile devices has caused the power/energy consumption to become one of the main design criteria. Major parts of this energy are consumed in the charging and discharging of the device and

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interconnect/bus capacitances. This component is called the dynamic power and is given by:

$$P_{dynamic} = \sum_{i=0}^{N-1} C_{load,i} \cdot V_{dd} \cdot V_{swing} \cdot f \cdot \alpha_i$$

Where the summation is over all the N nodes of the circuit, C_{load},i is the load capacitance at node i, V_{dd} is the power supply voltage, V_{swing} is the node high-to-low voltage difference, f is the clock frequency, and αi is the probability of the switching activity (SA) at node i. Therefore, for reducing the power consumption in CMOS circuits, the number of node switching from high to low must be decreased. In this paper, our objective is to reduce the number of switching. In DSP systems, a SA reduction in the arithmetic blocks and buses have an important effect on dynamic power consumption. The data encoding scheme may have a significant impact on the SA in the modules. Two's complement (2'sc) number representation is the most commonly used encoding in DSP applications [1]. This is due to ease of performing arithmetic operations such as additions and subtractions [1]. A major drawback of the representation, however, is the sign extension, which causes the MSB sign-bits to switch when signals transition from positive to negative or vice-versa, leading to an increase in the power overhead [1].

2. PREVIOUS WORK

In this segment, we quickly consider a few past pertinent works by aggregating their PPG and PPR qualities. The section acronyms MR, ME, DN, #OP, PPDS, and PPDE remain for multiplier recoding, various encoding, dynamic invalidation of IPPs, number of operands to be included (i.e., number of initially created non-redundant decimal numbers, or SD fractional items), halfway item digit set, and incomplete item digit encoding, individually. Some different chips away at decimal increase with coasting point operands, particular plans for Field Programmable Gate Array (FPGA), or digit-by-digit iterative approach are not recorded, since they depend on one of the organized works, or utilize implanted FPGA segments, which are out of the extent of this paper.

Consecutive multiplier, ease back PPG through BCDto-[−5,5] SMSD recoding of multiplier's and multiplicand's digits, trailed by digit-by-digit increase prompting [− 6, 6] PPDS with moderate halfway item amassing. Parallel multiplier, [− 5 , 5] SMSD recoding of multiplier, quick convey free X - various age through repetitive portrayal of products including 3 X, 5:1 multiplexing with dynamic refutation. This nullification cost is reproduced n times for parallel n × n augmentation. In addition, the n embedded 1s for 10's complementation in and n × (n + 1) 1s for digit insightful two's complementation in negatively affect territory and power sparing. The same is valid for the rectification consistent, and more mind boggling recoding because of zero taking care of, for [0, 15] fractional items. One approach to spare these cost, is to create the SD pre-computed X products with sign size arrangement, in order to diminish the XOR entryways to one for each digit

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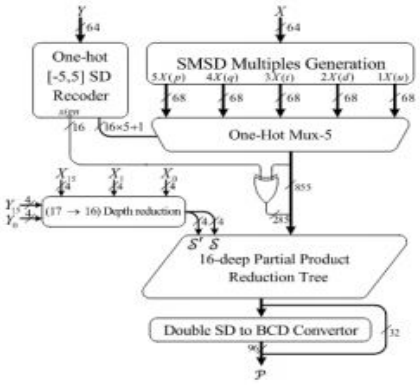

Fig 1: Block diagram of the proposed multiplier.

All the required decimal multiplicand products, aside from the 3X various, are gotten in a couple of levels of combinational rationale utilizing distinctive digit recorder's and performing diverse settled m-bit left moves (Lmshift) in the bit-vector portrayal of operands. The structure of this digit recorders Fig. 1 demonstrates the square graph for the age of the positive multiplicand products {X, 2X, 3X, 4X, 5X} for the SD radix-10 recoding

3. SBR REPRESENTATION

Since the sign extension is composed of repeated sign bits, the information contained in the sign extension is redundant and its switching can dissipate some power. For example, let us assume a small number, e.g. 00000010 (+2), on the bus in a clock period. Now, if in the next clock period, a negative small number, e.g. 11111101 (-3), is transmitted through this bus, there occur 8 transitions on the bus. Since these numbers can be shown by 3 bits and, hence, 5 of 8 transitions are not necessary,in our method, these extra transitions are compressed to one transition. The same transition saving may be applied to a multiplier where the number of redundant transitions is higher. In a multiplier, regardless of the multiplicand, if the multiplier is 11111101 (-3), then there are 7 partial products which equals to 6 additions and 1 subtraction. Because, this number has 6 sign bits, 5 of 7 partial products are unnecessary. As is explained next, the scheme proposed here eliminates these extra partial products. In this paper we propose a new representation for signed numbers where all sign bits are changed to zero except the first xM-1 from the LSB side. Here, an extra sign bit is added to the left side of the number to indicate the first sign bit.

Note that most DSP systems have a regular structure which makes the use of this approach more suitable for them. It consists of two memory blocks for storing the coefficients and the input data samples, two register for holding the coefficient and the input data, an output register, the controller along with the MAC (Multiply and Accumulate), an SBR encoder, and an SBR decoder. The multiplier in MAC is an SBR multiplier which will be explained in the next section. The filter coefficients in the coefficient memory are in SBR format. If the input data samples are in SBR format, we do not need an SBR encoder.

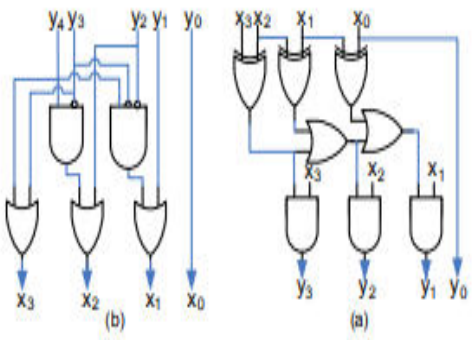

Fig 2: a) 2'sc to SBR encoder (4 bit)
b) SBR to 2'sc decoder (4 bit)

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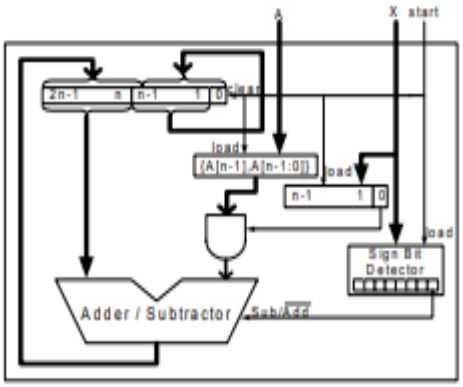

Fig 3: Multiplier block diagram with SBR input

As mentioned above, usually one of two inputs of multipliers in FIR filters is input data that coming from a digital signal such as voice or video, and the second input is a coefficient vector. If the input data is coded by SBR representation, the power consumption in the buses and computational blocks will be reduced. In this section, we explain a shift/add multiplier which is suitable for SBR inputs. Figure 3 shows our multiplier called shift/add SBR multiplier. In this architecture, X is multiplier with SBR representation while A is multiplicand with 2'sc representation. In an FIR filter, X can be input data and A is a coefficient.

A 2'sc number in the range of [-2N-1, +2N-1) requires N-bit for the representation while the same number in SBR encoding should be shown with N+1 bits. If X∈[-2N-2, 0], number of 1s in SBR code (except redundant bit) is less than the 1s in the 2'sc code. Thus, in a shift/add SBR multiplier, the number of partial products will be less than a shift/add 2'sc multiplier. Figure 6 shows an example of the multiplication of two numbers in 2'sc and SBR multipliers. In this figure, 00001101 (+13) are multiplied by 11111101 (-3). In SBR multiplier, the sign bit is the third bit and there are only 2 partial products. In Figure 5, at the first clock of every multiplication, the sign-bit-detector block detects the sign bit location of SBR input data and then set the corresponding bit to 1 and the rest of the bits to zero. For the above example, after detecting the sign bit, it contains the pattern "00000100". For the following clocks, this block only shifts right this pattern bit by bit where its LSB controls sub/add input of adder. This explanation indicates that this block does not affect the critical path.

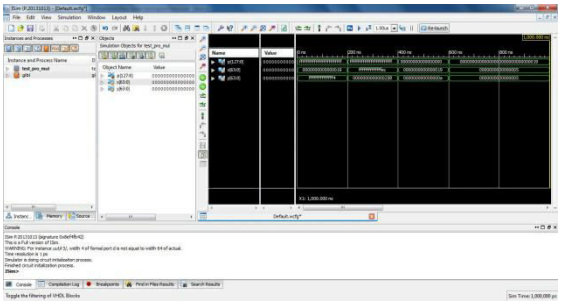

Fig 4: Simulation result for the proposed system

4. CONCLUSION

In this paper, we proposed a new data encoding techniques, named SBR (Sign Bit Reduction) to decrease the switching activity on a data bus and a signed multiplier. The effect of our techniques in reducing switching activity (SA) in multiplier is more than SA in buses. Experimental results of the simulated multiplier circuit (including encoder) show that our techniques can achieve up to 35% reduction in switching activity for the multiplication and up to 14.5% reduction in switching activity for the data buses.

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