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Volume 07, Issue 12, Pages: 452–456.

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DESIGN AND IMPLEMENTATION OF HIGH SPEED AND LOW POWER ERSFQ DECODER FOR MEMORIES

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Abstract: We have designed and tested at high speed and low power RSFQ-decoder, the critical component of an 8-bit RSFQ processor data path. The memory design is based on an asynchronous wave-pipelined approach scalable for wide datapath processors. We report on the development of energy-efficient decoders for memory and register file. To reduce the pitch, area, and energy, our decoder employs scalable binary tree architecture. We implemented these decoders using ERSFQ logic controlled by magnetically coupled address lines. These lines are driven by energy-efficient drivers based on the current-stirring technique. We experimentally confirmed the functionality of the circuits achieves better performance compared to the previous designs.

Index Terms: energy-efficient logic, random access memory, RSFQ

1. INTRODUCTION

A high-performance arithmetic-logic unit (ALU) is a fundamental building block for any special- or generalpurpose processor. The reported ALU is a key processing component for the RSFQ-based [1] 8-bit processor datapath [2]. This is the first attempt to build a superconductor parallel processor in contrast to the bit-serial approaches [3, 4]. The ALU design is based on Kogge-Stone adder (KSA) [5]. A set of logic operations is integrated into the adder structure. The ALU is switched between arithmetic and logic operations by control signals. A similar approach to build an adder-based ALU was reported in [6]. However, that ALU was based on a simple ripple-carry adder and, therefore, was hardly scalable to a large number of bits. The current ALU employs a wave-pipeline synchronization approach [7].

According to this approach, a pipeline stage is allowed to start its operation on two independent data operands as soon as both operands arrive. There is no clock pulse used to advance the computation from one stage to another. Instead, a clock pulse that follows data is used to reset cells in the stage to make it ready to process the next data wave. This type of synchronization makes it different from the previous RSFQ-based pipeline ripple-carry adder [6] and KSA [8], where a co-flow timing technique was used to clock data throughout the entire adder requiring a clock distribution tree for every stage. We have already reported low-frequency functionality test results of the 8-bit ALU in [9]. This paper focuses on high-speed test results.Typically RAM and register file are organized as a memory cell matrix

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addressable using n-to-2 n address decoders, where n is a number of address bits. For the efficient design, the decoder has to be low power and match dimensions (pitch) of that of memory cell rows or columns as close as possible. There are several known decoder design types implemented using superconducting circuits: loop decoders, tree decoders, NOR and NAND decoders [11]-[22]. The first decoder based on energy-efficient ERSFQ logic [1] was described in [23]. This 4-to-16 bit decoder was implemented using Hypres 4- layer process with 4.5 kA/cm2 critical current density, occupied 0.7 x 1.8 mm2 and dissipated ~70 aJ per one address decode operation. In this paper, we present a new ERSFQ decoder based on a binary tree architecture featuring 2 n scaling and with significantly more compact layout enabled by advanced fabrication processes developed at Hypres and at MIT-LL.

2. DESIGN

2.1 Decoder with Binary Tree Architecture

Fig. 1 shows a block diagram of the n-to-2 n bit address decoder with a binary tree architecture. It consists of n address line drivers. In contrast to our previous decoder design with n2 n decoder cells [23], the binary tree architecture requires only 2 n - 1 decoder cells. With energy efficiency being one of the primary goals of this design, the binary tree approach has a significant power scaling advantage (~ factor of n) comparing to the previous matrix design

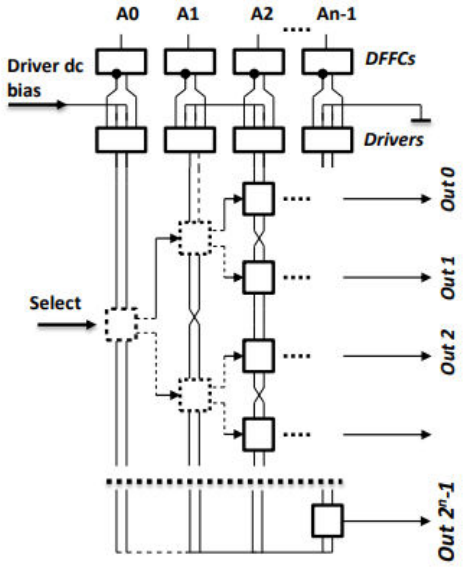

Fig. 1: Block diagram of the binary tree decoder.

An address line driver [23] comprises an ERSFQ D flip-flop with complementary outputs (DFFC) that generates SFQ control signals for the dc-powered current steering loop driver [22]. For each column of the decoder, two complementary superconductive lines (An andĀn) traverse the entire vertical dimension of the decoder (Fig. 1). Each cell of the decoder cell tree is magnetically coupled to one of the complementary lines. By commutating an and a lines in the proper order, a unique combination of control currents can be achieved to address all 2n outputs. This addressing allows for the select signal to propagate to the appropriate output, thus performing address decoding. Similarly to the earlier demonstrated decoder [23], once the address is set, the decoder settings do not change until another address is applied, allowing this circuit to be used also as a switch.

2.2 Decoder Cell

Fig. 2 shows a decoder cell based on SFQ switches controlled by dc currents via magnetic coupling. Each decoder cell (Fig. 2) consists of two dc-current driven SFQ

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switches. Each switch is magnetically coupled to one of two complementary lines. When the current is present in the line, the switch is in ON position - the incoming SFQ pulse can propagate through the switch. On the contrary, the absence magnetically induced current puts the switch in the OFF position, and the SFQ pulse escapes via the buffer junction. Thus, the decoder cell commutates its input to one of two outputs. When the corresponding address bit is "1" (line A is carrying current), the cell sends the input SFQ pulse to its output Out1. And when the address bit is "0" (line $\bar{A}$ is carrying current), the cell sends the input SFQ pulse to its output Out0.Each decoder output from Out0 to Out2n -1 has a unique combination of true and complement address lines, thus connecting it to the input of the tree.

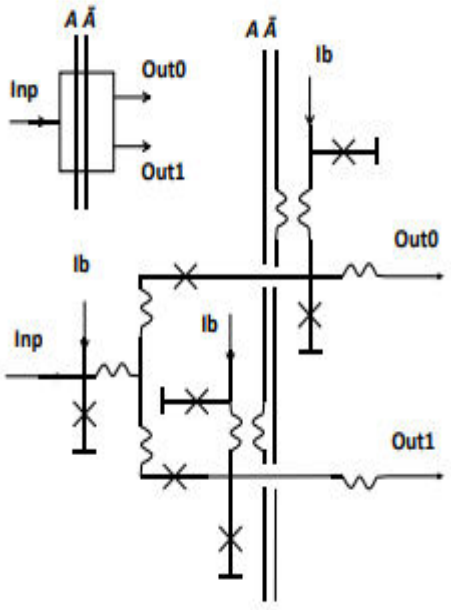

Fig. 2: Decoder cell symbol and schematics.

The addressing time of the decoder (i.e., time of address setting) is the time to charge/discharge current from control lines, that is estimated as ~100 ps [23]. The select time is the time delay for SFQ pulse propagating from input to output. For n = 4 and at 10 kA/cm2 process, it can be estimated based on our simulations as 30 ps at nominal bias.

2.3 Low-Speed Functionality Test

We have performed functionality testing of the decoder matrix fabricated using MIT-LL process. The fabricated chips were mounted in flip-chip cryoprobe. The chip was measured at 4.2 K temperature with multilayer mu-metal providing necessary magnetic shielding. Evaluation of 4-bit decoder functionality and dc bias current margins measurements were performed with multifunctional test system OCTOPUX [31].

For the ERSFQ circuitry the dc bias is provided by Josephson transmission line through large superconducting inductors. We estimate that FJTL should exceed ~25% of total dc bias current [32]. The decoder with the larger FJTL has already been designed for HYPRES 10 kA/cm2 6-layer process with HKI NbN layer. Although, the introduction of the feeding JTL reduced the overall energy-efficiency of the stand-alone decoder by raising the required bias current with ~30% of total bias being drawn by FJTL; it is also resulted in improvement of the operational bias margins. When decoder is integrated into a larger circuit, e. g., into MRAM or register file, the role of FJTL will be taken by other circuits such as a clock distribution network.

2.4 High-speed test

In order to perform high-speed test, we employed a similar to one demonstrated in [33], [34] technique. We apply a highspeed select signal from the high-frequency generator, while the address switch was applied at fairly low speed. The output data stream is monitored on toggling-type SFQ/dc converters.

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3. SIMULATION RESULTS

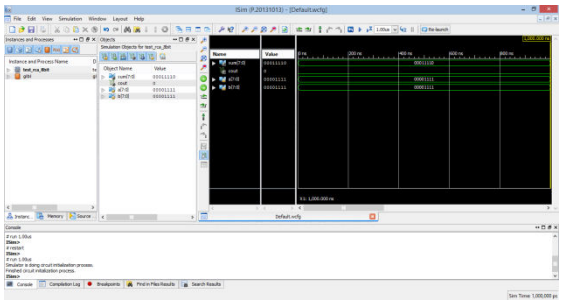

Fig 3: Simulation result for the proposed system

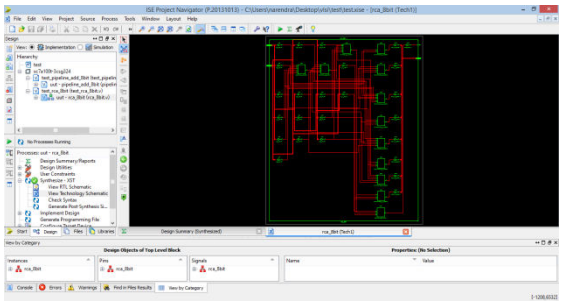

Fig 4: Technology schematic of the proposed system

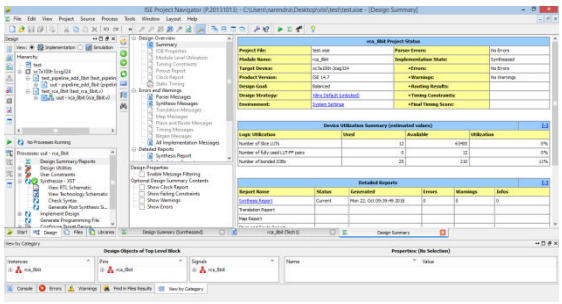

Fig 5: Summary report of the proposed system

4. CONCLUSION

We have developed new decoder circuits using a scalable binary-tree architecture optimized for perspective register file applications. We implemented two different decoder designs using this architecture. The first design was implemented using HYPRES Integrated Memory Process and optimized to have a small vertical pitch of output decoder rows to match dimensions of the word rows in MRAM. The second design was implemented for MIT-LL process and optimized for integration with a register file in a microprocessor. The common objective of both designs was to minimize energy consumption. This was achieved using a spaceefficient current-steering addressing scheme dissipating no power in static regime and requiring relatively small power for the address change. The address decoding is done by the controlled SFQ pulse propagation with power dissipation typical for any ERSFQ circuit. 5.

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