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IMPLEMENTING THE LOW POWER AND HIGH SPEED FULL ADDER USING GDI MULTIPLEXER

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Abstract— this paper proposes a new method for implementing a low power full adder by means of a set of Gate Diffusion Input (GDI) cell based multiplexers. Full adder is a very common example of combinational circuits and is used widely in Application Specific Integrated Circuits (ASICs). It is always advantageous to have low power action for the sub components used in VLSI chips. The explored technique of realization achieves a low power high speed design for a widely used subcomponent- full adder. Simulated outcome using state-of-art simulation tool shows finer behavioral performance of the projected method over general CMOS based full adder. Power, speed and area comparison between conventional and proposed full adder is also presented.

Keywords— Low power full adder, 2-Transistor GDI MUX, ASIC (Application Specific Integrated Circuit), 12-TFA, CMOS (Complementary Metal Oxide Semiconductor)

I. INTRODUCTION

With the tremendous progress of modern electronic system and the evolution of the nanotechnology, the low- power & high speed microelectronic devices have come to the forefront. Now a day, as growing applications (higher complexity), speed and portability are the major concerns of any smart device it demands small-size, low-power high throughput circuitry. So, sub circuits of any VLSI chip needs high speed operation along with low-power consumption. Now a day logic circuits are designed using pass transistor logic techniques. In PTL based VLSI chips MOS switches are used to propagate different logic values in various node points, as it reduces area and delay as compared to any other switches typeIt reduces the number of MOS transistors used in circuit, but it suffers with a major problem that output voltage levels is no longer same as the input voltage level. Each transistor in series has a lower voltage at its output than at its input. In order to minimize sneak paths, charge sharing, and switching delays of the circuit all the sub-circuit component has to be arranged obeying the VLSI design rules. Ensuring this simulation of circuit schematics provides a platform to verify circuit performance.

II. Logical Implementation of FA

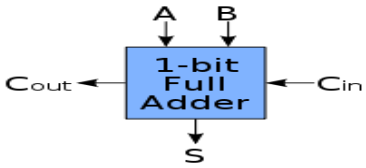

Fig. block Diagram of 1-bit Full Adder

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While taking account of full adder the sum and carry outputs are represented as the following two combinational Boolean functions of the three input variables A, B and C.

$$Sum = A \oplus B \oplus C \text{-------eqn.1}$$

$$Carry = AB + AC + BC \text{-------eqn.2}$$

Accordingly the functions can be represented by CMOS logic as follows in fig. 1,

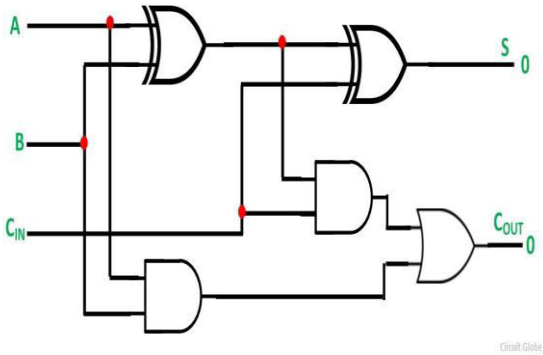

Fig. 1-bit Full Adder using CMOS Style:

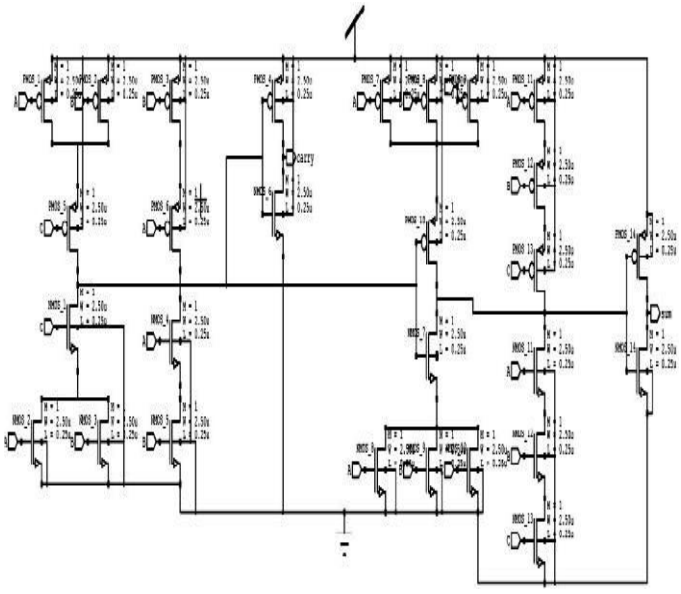

Fig: Conventional 28-T CMOS 1 bit full adder

GDI technique based full adder have advantages over full adder using pass transistor logic or CMOS logic and is categorized by tremendous speed and low power. The technique has been described below.

A. Gate Diffusion Input (GDI) Technique

The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low-power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top- down approach by means of small cell library [5]. The basic cell of GDI is shown in Fig.2.

1) The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.

2) It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal).

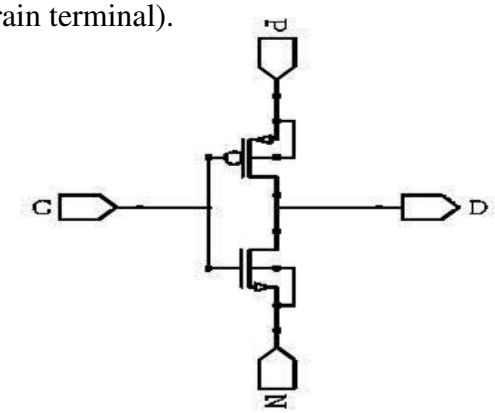

Fig 2 GDI basic cell consisting of pMOS and nMOS

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GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design.We can realize different Boolean functions with GDI basic cell. Table I shows how different Boolean functions can be realized by using different input arrangements of the GDI cell.

N	P	G	Output	Function	Transistor Count
0	1	A	A’	Inverter	2
0	B	A	A’B	F1	2
B	1	A	A’+B	F2	2
1	B	A	A+B	OR	2
B	0	A	AB	AND	2
C	B	A	A’B+AC	MUX	2
B’	B	A	A’B+B’A	XOR	4
B	B’	A	AB+A’B’	XNOR	4

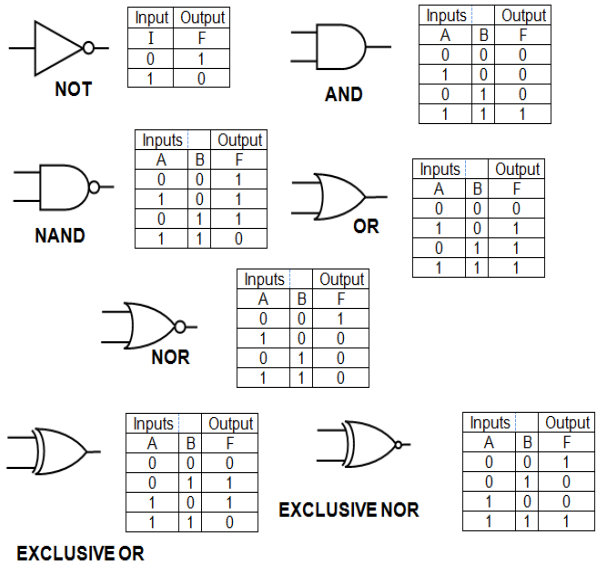

Fig Logic Diagrams and Truth tables

III. ARCHITECTURE OF PROPOSED GDI FULL ADDER

The basic architecture of the 2:1 MUX using GDI method is shown in fig. 3. In this configuration we have connected PMOS and NMOS gate along with a SEL line ‘A’, as in MUX. As we know that PMOS works on ACTIVE LOW and NMOS works on ACTIVE HIGH. So, when the SELECT input is low (0) then the PMOS get activated, and show the input ‘B’ in the output and due to low input (0) the NMOS stands idle, as it is activated in high input.

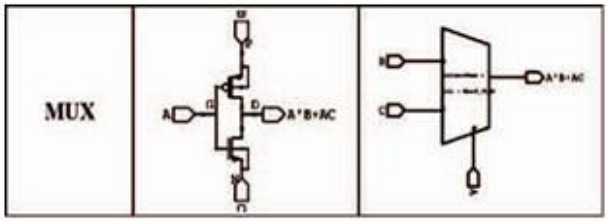

Fig.3 Basic view of 2T MUX using GDI technique

Same for the case, while the G input is high (1) then the NMOS get activated, and show the input ‘C’ at the output. Thus this circuitry behaves as a 2-input MUX using ‘A’ as SEL line, and shows the favorable output as 2:1MUX.

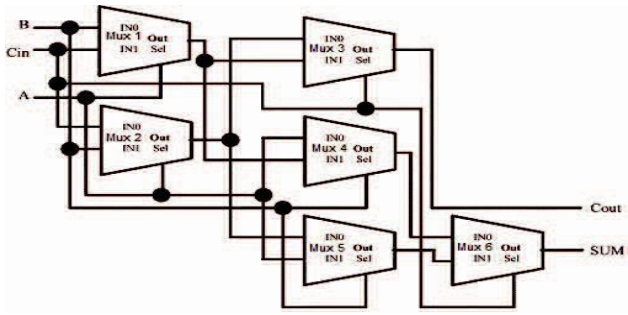

Fig.4 Block Diagram of Low Power Proposed Full Adder using 2T MUX

Now we are implementing the low power full adder circuit with the help of 2T MUX, made by

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GDI technique. It requires total 6 numbers of 2T MUX having same characteristics to design a 12T full adder and connected as above in fig.4.
The truth table for the above circuit taking each MUX as consideration are shown table II, and from there it generates 6 various outputs of various MUX.

IV. LOGIC ANALYSIS

The digital circuit shown in the fig. 4 can be analyzed logically with the help of simple Boolean algebra. The outputs of each MUX can be analyzed to get the sum & carry.

$$MUX1 = (B\bar{A}+CA)$$

$$MUX2 = (C\bar{A}+BA)$$

$$MUX3 = [(C\bar{A}+BA)\bar{C}+(B\bar{A}+CA)C]$$

$$= AB\bar{C}+\bar{A}BC+AC$$

$$= AB\bar{C}+\bar{A}BC+AC(B+\bar{B})$$

$$= AB\bar{C}+\bar{A}BC+ABC+A\bar{B}C$$

$$= AB\bar{C}+ABC+\bar{A}BC+ABC+A\bar{B}C+ABC$$

$$= AB(C+\bar{C})+BC(A+\bar{A})+AC(B+\bar{B})$$

$$= AB+BC+CA = Cout$$

$$MUX4 = \bar{A}\bar{B}+(\bar{A}B+AC)B$$

$$MUX5 = (C\bar{A}+BA)\bar{B}+AB$$

$$MUX6 = [\bar{A}\bar{B}+(\bar{A}B+AC)B]\bar{C}+[(C\bar{A}+BA)\bar{B}+AB]C$$

$$= A\bar{B}\bar{C}+\bar{A}B\bar{C}+\bar{A}\bar{B}C+ABC = A \oplus B \oplus C = Sum$$

Logic transition, short-circuit current and leakage current are the three main sources of power dissipation in CMOS VLSI circuits. During the transition of output from one logic level to other both the NMOS and PMOS transistors become active and provide a short circuit path directly between supplies to ground which increases the power consumption of the circuit. As the proposed 12-T full adder is made of GDI based MUX , it does not provide direct connections between supply and ground, so the probability of a getting short circuit current during switching can be considerably reduced; i.e., the power consumption due to short circuit current is considerably small. Again, in the proposed 12T full adder, all the select line of the MUX i.e. the G nodes of the GDI cells are directly connected with the input signals, results a much faster transition (less delay) in its output signals. As a result, the power consumption of the final pad out stage is low and it can provide faster Sum and Cout outputs.

V. SIMULATION

The platform of simulator generally provides outputs on behalf of certain input characteristics or behaviors of a selected object or abstract system. Simulation can be used to get or verify the behavioral and timing analysis of the circuit models. Here conventional FA & proposed 12-T full adder circuits are analyzed in standard simulator using 250 nm technologies. We implement the conventional full adder using 28T (transistor) & simulate out its power consumption & timing delays. Then we again design & simulate out the low power full adder using the concept of GDI logic & thereby implementing the design with 2-T MUX. First 2T GDI MUX and then the conventional and proposed circuits are simulated in schematic editor by providing various input logic combinations.

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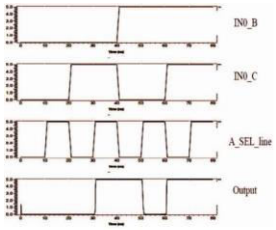

Fig.6. 2T GDI based 2:1 MUX transient response.

VI. SIMULATION RESULTS AND ANALYSIS

The schematics shown in fig. 7 & fig.8 are simulated with the help of standard simulator tool to get the timing, power analysis. The transient responses of these schematics are shown below in fig.9 & fig. 10.

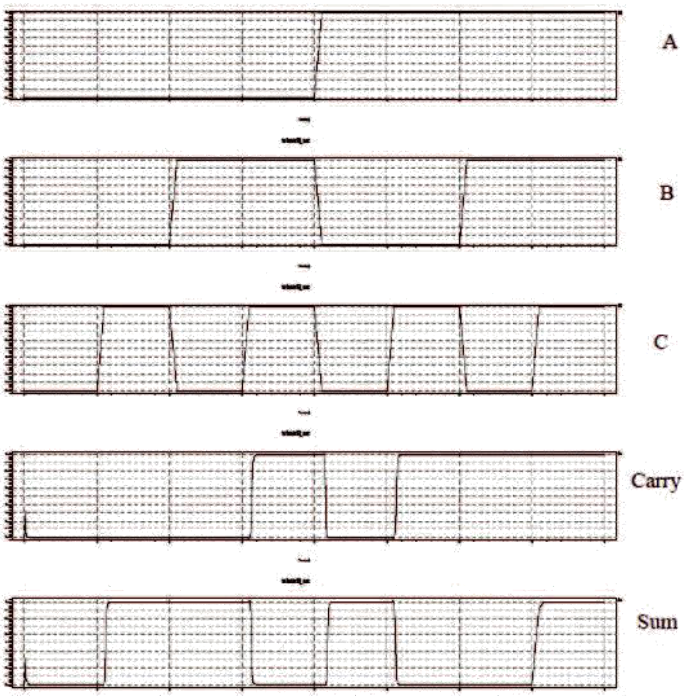

Fig. 9 Transient response of conventional 28-T F

From the fig. 9 and fig.10 it can be easily understood that the proposed 12 -T full adder is having the same transient response as like the conventional 28-T FA. The power & timing analysis is tabulated in the table below,

VII. CONCLUSION

From the above results it can be concluded that our proposed full adder has got better performance in delay, power and area consideration in comparison with conventional full adder. It shows that in contrast to other conventional techniques, this approach is better and it will be more appropriate for industrial practice in complex process technologies.

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