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Paper Authors

N.KRISHNA PRIYA, K.MADAN MOHAN
Intell Engineering College , Anantapur

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LOW-POWER HIGH SPEED 1-BIT FULL ADDER CIRCUIT DESIGN IN HYBRID TECHNOLOGY

N.KRISHNA PRIYA[1],K.MADAN MOHAN [2]
[1]PG Scholar, ECE Department, Intell Engineering College , Anantapur
[2] Associate Professor, ECE Department, Intell Engineering College , Anantapur

ABSTRACT: The general objective of our work is to investigate the power and delay performances of low-voltage full adder cells in different CMOS logic styles for the predominating tree structured arithmetic circuits. A new hybrid style full adder circuit is also presented. The sum and carry generation circuits of the proposed full adder are designed with hybrid logic styles. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to over- come the switching delay problem. As full adders are frequently employed in a tree structured configuration for high - performance arithmetic circuits, a cascaded simulation structure is introduced to evaluate the full adders in a realistic application environment. A systematic and elegant procedure to scale the transistor for minimal power-delay product is proposed. The circuits being studied are optimized for energy efficiency at 180nm, 90nm and 45nm CMOS process technology. With the proposed simulation environment, it is shown that some survival cells in standalone operation at low voltage may fail when cascaded in a larger circuit, either due to the lack of drivability or unsatisfactory speed of operation. The proposed hybrid full adder exhibits not only the full swing logic and balanced out- puts but also strong output drivability. The increase in the transistor count of its complementary CMOS output stage is compensated by its area efficient layout. Therefore, it remains one of the be st contenders for designing large tree structured arithmetic circuits with reduced energy consumption while keeping the increase in area to a minimum. In this report the 1-bit proposed full adder circuit is designed and also it is also extended to 4-bits and the results of power and delay were also tabulated.

1. INTRODUCTION

It is time we explore the well-engineered deep submicron CMOS technologies to address the challenging criteria of these emerging low-power and high-speed communication digital signal processing chips. The performance of many applications as digital signal processing depends upon the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation, and digital filtering. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. However, the critical concern in this arena is to reduce the increase in power consumption beyond a certain range of operating frequency. Moreover, with the

explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, higher speed, longer battery life, and enhanced reliability. Adder is the core element of complex arithmetic circuits like addition. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector. There are standard implementations with various logic styles that have been used in the past to design full-adder cells [1–4] and the same are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the transistor count is varied. Different logic styles tend to favor one performance aspect at the expense of others. Standard static complementary metal–oxide–semiconductor (CMOS) , dynamic CMOS logic , complementary pass-transistor logic (CPL) and transmission gate full adder (TGA) , are the most important logic design styles in the conventional domain. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation .These designs exploit the features of different logic styles to improve the overall performance of the full adder.There are four basic arithmetic operations. Addition is one of them. Addition of two or more numbers is broadly utilized in numerous applications of VLSI, for example in application-specific DSP architectures and microprocessors. The numbers that are added in VLSI applications are usually in the form of binary digits that is in the form of 0's and 1's. Addition is the core of many other operations like subtraction, multiplication, division and address calculation. In VLSI field, an architecture called "Adder" is used to add two or more binary digits. Adder can be either a FA or a HA. This project concentrates on FA. Thus the main objective of this project is enhancing the performance of the available one-bit FA cell. The requirement for low-power VLSI systems is constantly increasing because of the endless applications emerging in mobile communication and compact devices. Today's compact devices are usually battery operated for example, mobile phones, PDA's, which demands VLSI with less power consumption. So designers and developers are facing more problems regarding high performance, rapid speed, low-power consumption and narrow silicon space. Thus constructing a high performance low-power adder cells are having enormous importance. Therefore in this project, a well-organized approach for understanding the adder construction and working is given. It is focused on splitting the entire FA into several smaller modules. Every single module is constructed, optimized, and tested individually. Multiple FA cells are formed by joining these smaller modules.

II. LITERATURE SURVEY

In our literature survey, different abstraction levels for power optimization in CMOS circuits are studied. Also the three main components responsible for power

dissipation are studied and the different techniques/ methods used to minimize these components in various research papers are reviewed. In this research we also surveyed the different transistor level techniques used to design low power CMOS digital circuits. Several research have been done in this area in last decades and we found that the recently proposed GDI technique is emerging as promising alternative of CMOS logic style for low power design with less number of transistors [9-11]. In digital circuit design. Survey includes the different power optimization methods at various level of digital circuit design process from system level to physical level. Different sources responsible for power dissipation in CMOS circuits are also reviewed. Techniques to reduce the effect of such sources in different research articles are discussed here. ArkadiyMorgenshteinet. al.,2009, presented a new technique for low-power digital combinatorial circuit design called Gate Diffusion Input technique. Basic GDI technique suffers from low threshold voltage that degrades the performance of digital circuits. Problem of low swing threshold voltage drop in GDI is discussed and how it is removed in proposed Hybrid GDI technique is explained. Thedetailed analysis of GDI/ Hybrid GDI technique- its cell structure design, operational and transient analysis, switching characteristics, fan-in and fan-out bounds, swing restoring buffer analysis are discussed.An 8-bit CLA adder was fabricated using GDI and CMOS. Simulation result shows 45% reduction of power-delay product in the test chip in GDI over CMOS and significant improvements in performance, as well as decreased number of transistors and area in most simulated GDI circuits over CMOS and PTL. Adarsh Kumar Agrawalet. al.,2009, presented a design of full adder using Mixed Gate Diffusion Inputstopology based on static CMOS inverter. For this, in the long chain of full adders, the GDI full adders are followed by inverters to improve the performances with respect to conventional single full adder chain. The propagation delay, dynamic and leakage power dissipation can be optimized by changing the number of full adders between two consecutive inverters. HSPICE simulation using TSMC 0.35µm and 0.18µm CMOS technologies evaluated propagation delay and average power for minimum power design. Their proposed circuit is 18 to 48% and 7 to 26% faster than the previous circuits at 0.35µm and 0.18µm CMOS technologies respectively. Subsequently the average dynamic power of their proposed circuits is 8 to 12% and 14% to 28% lower than the previous circuits at 0.35µm and 0.18µm CMOS technologies respectively.

1.2 PROBLEM DEFNITION

The problem being faced is designing of a Hybrid FA using Cadence virtuoso 180-nm, 90-nm and 45-nm technology is to reduce delay, area and power of a circuit. In the literature survey it is evident that the CCMOS logic utilizes28-Transistors, similarly in the CPL and TGA Logic uses 32T and 20T. These structures are not suitable for a suitable choice for low-power applications because of various limitations as discussed in the literature survey. The main drawbacks of these structures are

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voltage degradation in the output voltage levels and slow response, high power utilization and high area occupied. Therefore with the concern on power, area and speed, design and develop a hybrid full adder structure and validation of these structure in different technologies that is 180nm, 90nm and 45nm using cadence tool.

2. PROPOSED METHODOLOGY

The suggested FA circuits were prescribed by 3 blocks is represented in Fig-1. Module-1 and module-2 were XNOR modules, that will produce a sum signal (SUM) and module-3 creates the C(output carry signal). Each module is composed separately with the end goal that the whole adder circuit is upgraded in terms of power, area and delay

Fig-1: Schematic structure of proposed full adder

2.1 Altered XNOR-Module

In the suggested FA circuit, XNOR-module is in charge of the majority of the power utilization of the whole adder circuit. Subsequently, this module is intended to limit the power to the most desirable extend with by passing the voltage degeneration probability.

Fig-2: XNOR module.

The Modified XNOR circuit as demonstrated in a Fig-2 has a power utilization is decreasing remarkably by careful utilization of a weak inverter framed by Mp1 and Mn1 transistors. Moving faster into the levels of a output signals is ensured by level restoring of Mp3 and Mn3transistors. Different topology of XOR/XNOR is already being described. The XOR/XNOR utilizes 4T's at the price of a low logic swing. Contrarily, the XOR/XNOR described in utilizes a 6T's to obtain preferred logic swing equated to a 4T XOR/XNOR circuit. Here the XNOR module houses 6T, but having distinctive transistor organization than that of 6T XOR/XNOR. The XNOR circuit introduced in this work is having a low power and high speed when compared with the 6T XOR/XNOR circuit.

2.2 Carry Generation Module

The transistors Mp7, Mp8, Mn7, and Mn8 are depicted in Fig-3 represents a output carry signal. Through a TG's (Mn7 and Mp7), the input carry signal (Cin) is being propagated. This will causes a reduction in a overall carry propagation path. The intentional utilization of strong TG's ensured further decrease in propagation delay of a carry signal.

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Fig-3: Carry generation module.

The CMOS and TGA logic developed a new concept of Hybrid Adder in different CMOS technologies using Cadence and compare the different technology results and analyze the Adder performance of the area, power and delay

2.1.1 Operation of the proposed FA.

Fig-4: The circuit representation of proposed FA.

The Fig-4 demonstrates the detail outline of the proposed FA. The "sum" is being a output of a FA is formed by the 2-XNORmodules. The transistors Mp1 and Mn1 of the inverter will generate B, it is successfully utilized to plan the controlled inverter utilizing a transistor pair Mp2 and

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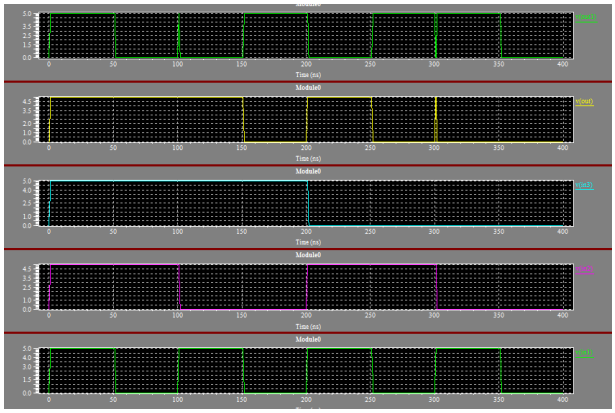
Mn2. However, it is having some voltage degeneration issue, which is being removed by utilizing a 2 pass transistors Mp3 and Mn3. pMOS transistors(Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5,and Mn6) comprehend to a second stage XNOR module to form a total Sum operation. Looking at a truth table of a FA, the action for $Cout$is being generated and abstracted as follows:

If, A = B, then$Cout$= B; else$Cout$=Cin.

The unity between inputs A and B is analyzed by AʘB operation. In the event that they are same, at that point$Cout$ is equal to B, it is achieved by utilizing the TG acknowledged by transistors Mp8 and Mn8. Contrarily, the input carry signal$Cin$is emulated as $Cout$which is achieved by other TG comprising of transistors Mp7 and Mn7.

3.SIMULATION RESULTS



4. CONCLUSIONS

In this work, a low power hybrid 1 bit and 4 bit FA has been presented. The simulation is done by utilizing standard Cadence Virtuoso tools with 180nm, 90nm and 45nm technologies and results of another standard design approaches are compared. In the previous work they are using a TGA Logic for both carry and sum block. But the proposed 1-bit FA combining the two different structures that is TGA for carry block and CCMOS for Sum block. Therefore the proposed structure of 1-bit FA uses only 16T's instead of 20T's compared with the previous work. The proposed 1-bit FA is compared with the different technologies with different parameters(Propagation delay and power dissipation). The comparison statements are briefly discussed in result section. The Transmission Delay of 1-bit FA in 180nm is 86.39ps, 90nm is 81.62ps and 45nm is 25.99ps. Similarly Power dissipation of 1-bit FA in 180nm is 12.1901µw, for 90nm is 0.8490 and 45nm is 0.0709µw. The 1-bit proposed FA circuit is extended to 4-bit and the results compared with the same technologies. The operating voltages required are decreases when technology shrinks. Similarly the power consumption reduces with the technology shrinks. Thus we can say that area can be reduced with the decrease in transistors widths and length.

The Transmission Delay of 4-bit FA in 180nm is 112ps, 90nm is 103.3ps and 45nm is 92.93ps. Power dissipation of 4-bit FA in 180nm is 43.1506 µw, 90nm is 3.2341µw and 45nm is 0.31159µw. Finally this method improved scheme is proposed. This method compared with different technologies saves more hardware resources. For the further reduction of hardware we can perform the ASIC design flow by doing this we can greatly reduce the number of logics hence we can reduce the hardware utilization and also we can reduce the area gate and power.

4.1 FUTURE WORK

As a future scope, enhancing the execution of 1 bit FA's can be executed by changing the value of W/L proportions. Utilizing the design of 1 bit proposed FA blocks, we can implement a 2 bit, 4 bit, 8 bit, 16 bit, 32 bit, 64 bit Subtractor/Adder circuits. These adders can also be design and differentiate using different possible nm technologies like 180nm, 90nm, 65nm, 32nm, 22nm, and so on.

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