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RELIABILITY ENHANCEMENT OF LOW POWER TSPC FLIP FLOP

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Abstract: Flip flop are basic storage elements used extensively in digital system designs, which adopt intensive pipelining techniques and employ several FF-rich modules such as register files, shift registers, and FIFO. The power consumption of the FFs employed in a typical digital system design, along with that of clock distribution networks In this project, an ultralow-power true single-phase clocking flip-flop (FF) design achieved using only 19 transistors is proposed. The design follows a master–slave-type logic structure and features a hybrid logic design comprising both static-CMOS logic and complementary pass-transistor logic. In the design, a logic structure reduction scheme is employed to reduce the number of transistors for achieving high power and delay performance. Despite its circuit simplicity, no internal nodes are left floating during the operation to avoid leakage power consumption. In this design, a virtual *VDD* design technique, which facilitates a faster state transition in the slave latch, is devised to enhance time performance. In circuit implementation, transistor sizes are optimized with respect to the power delay product (PDP).

1.INTRODUCTION

Flip flops consumes more power due to the presence of clock system, so measures were taken to reduce the load on clock system. Reduced clock swing flip flop was one method implemented earlier to decrease the clock power with respect to other flip flops. By using this method clock systems voltage swing was reduced [7]. Reduced swing technique was used in differential conditional capture flip flop to reduce the clock load, but in this flip flop both low swing and full swing clock signals are given as enable signal [6]. Since power was not reduced as expected, therefore many flip flops such as differential discharge flip flop, differential pre-charge flip flop, pulse triggered flip flops and so on were introduced by reducing the circuit complexity. To decrease the switching activity of the flip flops conditional capture and pre charge techniques were used. In paper [8] it discusses about many parameters such as setup time, hold time, D-Q delay and C-Q delay.

2.Related Work

A transmission-gate-based FF (TGFF) is arguably the most widely used FF currently. One possible drawback of this design is the excessive work load on the clock signal where complementary signals are required. The consequence is the presence of a considerable dynamic power even when the data switching activity is low. Recently, true single-phase clocking (TSPC) FF designs have been developed with the objective of lowering the clock signal loading. This is

usually achieved through circuit simplification. Cross-coupled set–reset (SR) latches are used in lieu of the TG-based latch to support single-clock-phase operations. Degenerate or topologically compressed SR latches [12], [13] are adopted to lower the circuit complexity. In this paper, we present a novel SR-latchbased FF (SRFF) design comprising both static-CMOS logic and complementary pass-transistor logic (CPL). This design follows the principle of TSPC operations to alleviate the clock signal loading. Both logic structure reduction and transistor optimization schemes are applied to optimize the design.

H. Kawaguchi and T. Sakurai, A reduced clock-swing flip-flop (RCSF) for 63% power reduction**.**A reduced clock-swing flip-flop (RCSFF) is proposed, which is composed of a reduced swing clock driver and a special flip-flop which embodies the leak current cutoff mechanism. The RCSFF can reduce the clock system power of a VLSI down to one-third compared to the conventional flip-flop. This power improvement is achieved through the reduced clock swing down to 1 V. The area and the delay of the RCSFF can also be reduced by a factor of about 20% compared to the conventional flipflop. The RCSFF can also reduce the RC delay of a long RC interconnect to one-half.Reduced clock-swing flip-flop (RCSFF) is proposed to lower the voltage swing of the clock system. The schematic diagrams of the conventional flip-flop and the proposed RCSFF. With the conventional flip-flop, the clock swing cannot be reduced because and are required, and overhead becomes

imminent if two clock lines and are to be distributed. On the other hand, if only is distributed, most of the clock-related MOSFET's operate at full swing, and only minor power improvement is expected. The RCSFF is composed of a true single-phase master-latch and a cross-coupled NAND slave-latch. The master-latch is a current-latch-type sense-amplifier. The salient feature of the RCSFF is that it can accept a reduced voltage swing due to the single-phase nature of the flip-flop. The voltage swing,Vclock , can be as low as 1 V.

V. Oklobdzija, V. Stojanovic, D.Markovic, and N.Nedovic,DigitalSystem ClockingHigh-Performanceand Low-Power Aspects .In CMOS multistage clock buffer design, the duty-cycle of clock is liable to be changed when the clock passes through several buffer stages. The pulse-width may be changed due to unbalance of the p- and nMOS transistors in the long buffer. This paper describes a delay locked loop with double edge synchronization for use in a clock alignment process. Results of its SPICE simulation, that relate to 1.2 lm CMOS technology, shown that the duty-cycle of the multistage output pulses can be precisely adjusted to $(50 \pm 1)\%$ within the operating frequency range, from 55 MHz up to 166 MHz.Almost all contemporary digital VLSI systems and other digital systems rely on clock pulses to control the movement of data. To reach the highest circuit speed in CMOS applications, the clock distribution system must be carefully designed. A great deal of attention has been paid to clock recovery, clock regeneration, timing, and distribution during the last several years.

B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J.K.S. Chiu,and M. M.-T. Leung, Improved sense-amplifier-based flip-flop designand measurements.Design and experimental evaluation of a new senseamplifier-based flip-flop (SAFF) is presented. It was found that the main speed bottleneck of existing SAFF's is the cross-coupled set-reset (SR) latch in the output stage. The new flip-flop uses a new output stage latch topology that significantly reduces delay and improves driving capability. The performance of this flip-flop is verified by measurements on a test chip implemented in 0.18 m effective channel length CMOS. Demonstrated speed places it among the fastest flip-flops used in the state-of-the-art processors. Measurement techniques employed in this work as well as the measurement set-up are discussed.

V. Stojanovic and V. G. Oklobdzija Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems .We propose a set of rules for consistent estimation of the real performance and power features of the flip-flop and master–slave latch structures. A new simulation and optimization approach is presented, targeting both highperformance and power budget issues. The analysis approach reveals the sources of performance and power-consumption bottlenecks in different design styles. Certain misleading parameters have been properly modified and weighted to reflect the real properties of the compared structures. Furthermore, the results of the comparison of representative master–slave latches and flipflops illustrate the advantages of our approach and the

suitability of different design styles for high-performance and low-power applications.

3.LOW-POWE21-TRANSISTORS USING TOPOLOGICALLY COMPRESSED SCHEMES

3.2.1 Introduction

➢ **Transmission Gate Logic**

As transmission gates, is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. n principle, a transmission gate made up of two field effect transistors, in which in contrast to traditional discrete field effect transistors - the substrate terminal (Bulk) is connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal
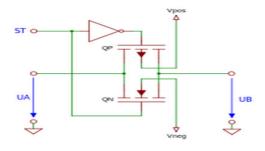
One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the n-channel MOSFET, and this begins to turn off. At the same time, the p-channel MOSFET has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct
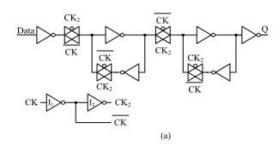
and the transmission gate switches.Thereby it is achieved that the transmission gate passes over the entire voltage range. The transition resistance of the transmission gate varies depending upon the voltage to be switched,and corresponds to a superposition of the resistance curves ofthe two transistors.
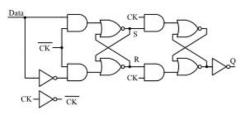

Fig1 Principle diagram of a transmission gate

The control input ST must be able to take to control depending on the supply voltage and switching voltage different logic levels.To provide a basis for comparison, some existing FF designs are reviewed first. A classic master–slave-type TGFF design is shown in Fig. 2
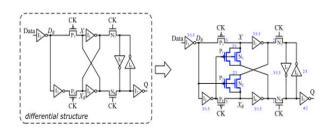

Fig2 Master Slave type TGFF

Indicating that it comprises two TG-based latch designs. Inverters I1 and I2 are used to generate complementary clock signals. This

design suffers from a high capacitive clock loading problem (a total of 12 transistors driven by the clock), which indicates a sustained power consumption even when the input remains static . This problem also occurs in conventional SRFF designs, as shown in Fig.3

Fig3 Conventional SRFF designs

To overcome the power consumption problem, two FF designs employing an adaptive coupling (ac) technique and a topologically compressed scheme have been proposed. Fig. 4 shows the ac FF design .

Fig4 AC Flipflop design

Unlike conventional TGFF designs, this design uses a differential latch structure with pass-transistor logic to achieve TSPC operation. The TGs are replaced with either n- or p-type pass transistors. To overcome the impact of process variations on the master latch, a pair of level restoring circuits is inserted into the crosscoupled paths of the

master latch. In this design, only four MOS transistors (two pMOS and two nMOS) are driven by the clocksignal, andthe transistorcountis loweredto 22.A lighter clock loading in addition to the circuit simplification of the FF design can lower the power consumption significantly. In this design, the data contention problem in the slave latch deteriorates as the data switching activity increases, and the advantages of power saving are thus diminished. The level restoring circuit pair of the master latch results in a longer setup time. Moreover,this design suffers from a power leaking problem when certain input and internal node combinations occur.

3.2.2 Procedure

Fig.3.6 shows another SR-latch-based TSPC FF design named topologically compressed FF (TCFF), obtained through a topologically compressed scheme. The logic schematic of this design is shown in Fig. 3.5, and theoriginal MOS circuit is shown in Fig. 3.6. The master latch adopts the configuration of a MUX with feedback and can be implemented with two AND-OR-Invert (AOI) gates and an inverter. The latch is transparent when the clock signal CK is 0.The inputs pass through the AOI gates and the output of the inverter; that is, node x3 is always complementary to the input data. When CK turns 1, the contribution from the input data is blocked and x3 remains unchanged because of a closed path formed by the upper AOI and the inverter.

The slave latch also comprises two AOI gates and an inverter. The complementary inputs from the master latch are fed to AND terms, which are also controlled by the clock

signal, of the two AOI gates. Only one phase of the clock signal is used in this design.The MOS circuit in Fig. 3.6 can be further optimized by factoring out the shared terms. For N (pull-down) logic,one CK-controlled nMOS transistor can be shared by the two discharging paths. For P (pull-up) logic, four pairs of pMOS transistors are connected to VDD, and two of these pairs share identical inputs. Therefore, two pMOS pairs of the master latch can be eliminated. Notably, nodes $x2$ and $x3$ are always complementary to each other, implying that either the $x2$- or $x3$-controlled pMOS transistors will turn ON. The drain node of the turned ON pMOS transistor corresponds to a virtual VDD. Through the addition of an extra clockcontrolledpMOS transistor across the two AOI gates, the two clock-driven pMOS transistors can be removed without affecting the function.

3.3 DESIGN OF TSPC 19-TRANSISTOR FLIP-FLOP BASED ON REDUCTIONSCHEMES

3.3.1 Introduction

The proposed design, named logic structure reduction FF (LRFF), can be considered as an enhancement of the TCFF design in different performance aspects. This design is achieved by various optimization measures. The first measure is the logic reduction for a shorter setup time, the second one is circuit simplification for lowering the power consumption, and the third one is the elimination of the node floating case to avoid the static power leaking problem.

i) Flip-flop

A flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bi stable multi vibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

ii) Logic Structure

- A clear definition of objectives & indicators is the starting point
- They are used to define problems, now and in the future
- Scenarios can be used to identify alternative futures
- An alternative is to start with identifying problems, while checking that all objectives have been covered
- Possible instruments are suggested as ways of overcoming the problems which have been identified
- Barriers to implementation will arise for certain policy instruments
- Strategies are developed as combinations of instruments, packaged to reduce the impact of the barriers
- The impacts of the individual instruments or the overall strategies are then predicted using a model

- The results for these options are then compared using an appraisal method based on the objectives
- This process may well identify ways in which the instruments or strategies can be improved
- It is possible at this stage to use optimisation techniques to help identify better strategies
- The preferred instrument or strategy is then implemented, and its performance assessed against the objectives; these results may help improve future prediction.

On a regular basis, a monitoring programme assesses changes in problems, based on the objectives.
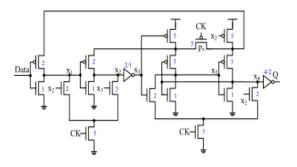

Fig.5 Circuit optimization

The transistor count is reduced from 28 to 21 andonly three transistors are driven directly by the clock signal. All these factors contribute to a significant power saving of the design. This design is fully static, even though both pull-up and pull-down logic networks are largely simplified. In conclusion, the TCFF design is based on three optimization principles:

1) use only a single phased clock

2) reduce the number of transistors driven by the clock

3) reduce the total transistor count.

Despite the significant improvement in the power consumption, the timing performance of the TCFF design is compromised. In particular, the design suffers from a longer setup time because of a weakened pull-up network in which only two pMOS transistors are connected to VDD directly. The critical path consists of three pMOS transistors connected in series. Although this problem can be alleviated by enlarging the pMOS transistors, the power consumption is negatively impactedFor P (pull-up) logic, four pairs of pMOS transistors are connected to VDD, and two of these pairs share identical inputs.

➤ Complementary Pass Transistor Logic

As indicated in the small figure in Fig.6, this term can be implemented using one pass transistor with CK as the control signaland x3 (or x2) as the sink of the dischargingcurrent.The converged discharging path in the TCFF design can be split into two separate paths, each comprising one pass transistor.
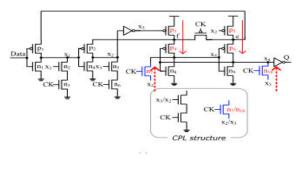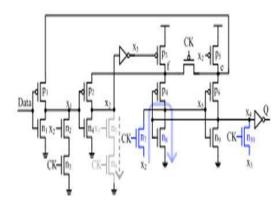

Fig.6 CPL Structure

Because these two pass transistors operate in a complementary manner, they are considered as CPL, and the transistor count can thus be reduced by one. The benefit of this logic structurereductionis twofold. First, it simplifies the circuit for power saving. Although the pulldowndelay mightbe slightly prolonged,it does not correspond to the worst case timing (in contrast to the pull-up delay). Second, when node x2 (or x3) is equal to 1, the pass transistor works in conjunction with the pull-up path formed by pMOS transistors p3/p4 (or p5/p6) to boost the output node of AOI to 1. This path is considered auxiliary because a "weak 1" can be delivered by an nMOS pass transistor. This additional current boost, however, improves the worst case delay when the slave latch is in the transparent mode (CK=1). A shorter clock-to-Q (CQ) delay can be obtained. The dotted and solid arrowed lines in Fig. 3.15indicate the working of these two charging paths to drive node x5 (or x4). The second logic structure reduction scheme is applied to the second AOI gate of the master latch. The discharging path of node x2 controlledby CK and x3 dischargesonly when both signals equal 1. CMOS(Complementary pass transistor logic):This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high.
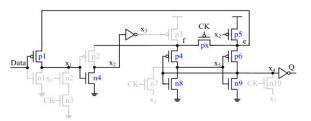
The symbol is an OR gate with a small circle on the output. The small circle represents inversion.As illustrated in Fig. 7 pass transistor n7 in addition to pull-down transistor n8controlled.by x4 forms an alternative discharging path for node x2
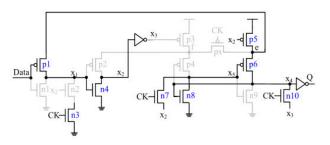

Fig.7 New discharging from n7 and n8 to ground

On the other hand, in an Active-low latch both inputs are normally HIGH, and the latch is triggered by a momentary LOW signal on either input. When the SET input momentarily goes LOW, the output goes HIGH. The output then stays HIGH until the RESET input momentarily goes LOW.

The master latch is in a transparent state, and nodes x2 and x3 are driven to 0 and 1, respectively. All transistors shown in gray are turned OFF. Signals from the master latch are blocked from entering the slave latch because both clockcontrolled feed-in transistors n7 and n10 are turned OFF. The slave latch is now in a hold state and the output remains unchanged. Note that x2 and x3 fed to p3 and p5 of the slave latch are not for the purpose of signal input. Instead, they serve to control the pseudo VDD nodes e and f.

Fig 8 Data latching process when ck=0,data=0

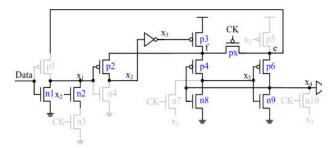Fig.9Data latching process when ck=1,data=0

The clockcontrolled px bridges these two nodes to ensure that they both become VDD. When CK turns 1, as illustrated in Fig. 3.21, the data from the master latch (i.e., x2 and x3) are fed to the slave latch through n7 and n10, respectively. Nodes x2 and x3 must maintain their values for a sufficient amount of time (i.e., the hold time requirement) to change the state of the slave latch. Because the clock-controlled transistor px is now turned OFF, node f is disconnected from VDD to facilitate a fast state transition. If the input data change after the hold time, both p2 and n4 are turned OFF. This implies that the data from the master latch are blocked from entering the slave latch. Node x2 remains at 0 because of the reverse signal flowthrough pass transistor n7. Therefore, no internal node floating problems occur. All transistors shown in gray are turned OFF. Signals from the master latch are blocked from entering the slave latch
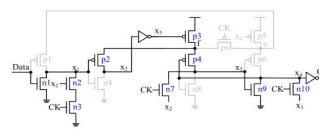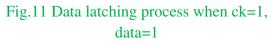
because both clockcontrolled feed-in transistors n7 and n10 are turned OFF. The slave latch is now in a hold state and the output remains unchanged.

Fig.3.10Data latching process when ck=0,data=1

Fig.11 Data latching process when ck=1, data=1

Note that x2 and x3 fed to p3 and p5 of the slave latch are not for the purpose of signal input. Instead, they serve to control the pseudo VDD nodes e and f. The clockcontrolled px bridges these two nodes to ensure that they both become VDD. When CK turns 1. Nodes x2 and x3 must maintain their values for a sufficient amount of time (i.e., the hold time requirement) to change the state of the slave latch. Because the clock-controlled transistor px is now turned OFF, node f is disconnected from VDD to facilitate a fast state transition.For the case of latching data=1, as indicated in Fig. 10, the master latch is transparent to admit the new data and the slave latch holds

its current value. For the slave latch, p3 is turned ON and the bridge transistor px passes VDD from node f to node e. This is in contrast to the case of data=0. In this evaluation, we also noticed a potential internal node floating problem associated with the ACFF design if clock gating was applied. As indicated in the circuit shown in Fig. 11, when the clock signal was frozen at 1 and the input data changed from 1 to 0, both nodes X and XB were determined to be in a floating state. This phenomenon can be illustrated by the simulation waveforms revealing that for each 1 to 0 transition of the input, the levels of nodes X and XB started to degrade in an exponential form. For a time span longer than 200 ns, the levels could be drifted to 0.89 and 0.21 V, respectively, at a VDD value of 1 V, resulting in additional power consumption.

➤ Power-Delay-Product Evaluation

Both PDPCQ and PDPDQ were employed as a composite performance index in our evaluation. When the switching activity was 12.5%, both PDP indices of the proposed design were the lowest, followed by those of the TCFF and ACFF. However, the indices of the remaining four non-TSPC designs trailed by a large margin. The proposed LRFF design, in particular, can simultaneously balance the power and speed performance for the best results. Illustrates a bar chart summarizing the PDP comparison results under different switching activities. shows the PDP performance under process variations with a 25% data switching probability. For each process corner (SS 0.8 V/ 125 °C, TT 1 V/25 °C, FF 1.2 V/−40 °C,

SF 1 V/25 °C, and FS 1 V/25 °C), the setup time and hold time were scanned to obtain the best PDP number. All FF designs were determined to function properly under process variations. Our design maintained its lead in all cases. Therefore, this evaluation also verifies the performance consistency of the LRFF design.

3.3.3 Procedure

As indicated in the MOS schematic shown in Fig. 3.8 theconverged discharging path controlled by $x2/x3$ and CK in the slave latch is first split into two separate discharging paths, each comprising two nMOS transistors in series and implementingthe logic $x2 \cdot CK \cdot 0$ and $x3 \cdot CK \cdot 0$. If $x2 = 1$ (or $x3 = 1$),it is logically equivalent to $\bar{x2} \cdot CK$ (or $\bar{x3} \cdot CK$). Because $x2$ and $x3$ are complementary, $\bar{x2} \cdot CK = x3 \cdot CK$ (or $\bar{x3} \cdot CK = x2 \cdot CK$). As indicated in the small figure in Fig. 3.14 this term can be implemented using one pass transistor with CK as the control signal and $x3$ (or $x2$) as the sink of the discharging current. The converged discharging path in the TCFF design can be split into two separate paths, each comprising one pass transistor. Because these two pass transistors operate in a complementary manner, they are considered as CPL, and the transistor count can thus be reduced by one. The benefit of this logic structure reduction is twofold. First, it simplifies the circuit for power saving. Although the pulldown delay might be slightly prolonged, it does not correspond to the worstcasetiming (in contrast to the pull-up delay). Second, when

node $x2$ (or $x3$) is equal to 1, the pass transistorworks in conjunction with the pull-up path formed by pMOS transistors $p3/p4$ (or $p5/p6$) to boost the output node of AOI to 1. This path is considered auxiliary because a "weak 1" can be delivered by an nMOS pass transistor. This additionalcurrent boost, however, improves the worst case delay when the slave latch is in the transparent mode (CK = 1). A shorter clock-to-Q (CQ) delay can be obtained. The dotted and solid arrowed lines in Fig. 3.14 indicate the working of these two charging paths to drive node $x5$ (or $x4$). The second logic structure reduction scheme is applied to the second AOI gate of the master latch. The discharging path of node $x2$ controlled by CK and $x3$ discharges only when both signals equal 1. As illustrated in Fig. 3.18 pass transistor $n7$in addition to pull-down transistor $n8$ controlled by $x4$ forms an alternative discharging path for node $x2$. We can thus remove the original (and redundant) path to simplify the circuit. This measure not only improves the power performance but also reduces the capacitive load of node $x2$. A shorter propagation delay can be achieved for the master latch when operating in the transparent mode, resulting in a shorter setup time of the FF design. The circuit schematic after the application of the two logicstructure reduction schemes is presented in Fig. 3.19. The total number of transistors is only 19. Only one single phase of the clock is required, and the fan-out for the clock signal is four (one pMOS and three nMOS transistors). The proposed LRFF is fully static and can avoid the case of temporary output node floating. When CPL
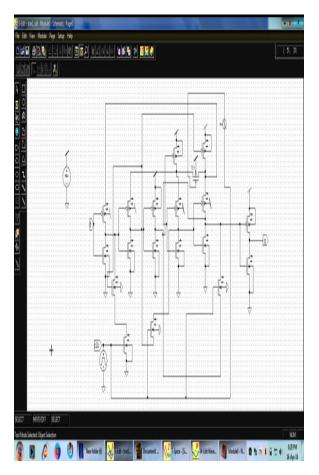
is introduced, the circuit complexity of its p-logic network is largely reduced, even though the design is not a dynamic logic. In conclusion, the proposed design can successfully achieve circuit complexity reduction and timing parameter enhancement simultaneously.
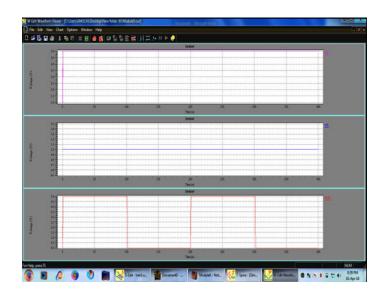
RESULT AND ADVANTAGES

5.1 RESULT

Fig12 Circuit connection of Master- slave D-flip-flop using TCFF technique

The above figure represents the circuit of master- slave D-flip-flop using modified gate input technique. The circuit is designed in the tanner tool. The input to the circuits is D and the clock

Fig13 Simulation wave forms low power 19-transistor true single phase clocking using reduction schemes

The above circuit represents the outputs wave forms of the low power 19- transistor true single phase clocking using reduction schemes,v(clk) is the clock input of the citcuit, v(d) is the data input of the circuit, v(q), is the output of circuit.

Fig14 Power Consumption

NETLIST DETAILS OF THE CIRCUIT

Transistor count

- Transistor – 19

Power Results

- VVoltagesSource_1 from time 1e-008 to 4e-007
- Average power consumed-> 1.028366e-009 watts
- Max power 1.057001e-009 at time 1.02e-007
- Min power 9.382613e at time 1e-008

Propagation Time

- Paring   0.00 seconds
- Setup   0.00 seconds
- DC operating point   0.01 seconds
- Transient analysis   0.06 seconds
- ---
- Total   0.07 seconds

5.2 ADVANTAGES

- High speed
- Low power consumption and low voltage
- Low power dissipation
- Reduce circuit Area
- Reduce long discharging path problem

5.3 APPLICATIONS
- Used in low power applications
- Used in Memories
- Used in Sequential circuit
- Used in Chip designs

CONCLUSIN AND FUTURE SCOPE
5.4 CONCLUSION:

We present a novel FF design achieved by employing a modified SR latch structure incorporating a hybrid logic consisting of static-CMOS logic and CPL. The key idea is providing an additional discharge path between the master and slave latches, which not only shortens the transition time to enhance the power and speed performance, but also reduces circuit complexity for better timing parameters. Extensive simulations were conducted and various performance indices such as power consumption, PDP, setup time delay, and CQ delays were evaluated. The proposed design was determined to excel in almost every performance index, except for hold time performance. In particular, the proposed design consistently outperformed other designs under different voltage and switching activity settings. This thus proves the efficiency of the proposed FF design.

5.5 FUTURE SCOPE

We hope that presented results will encourage further research activities in TCFF technique. The issue of sequential logic design with TCFF is currently being explored, as well as technology compatibility. More work was recently done in automation of logic design methodology based on TCFF technology.

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