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A Novel Harmonica Elimination Method for Single-Phase Industrial Applications

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ABSTRACT:

There are many ongoing researches in the field of harmonic compensation using active and passive power filters or the combination of the two, which are known as hybrid power filters. These filters can be implemented as series or shunt units. For shunt compensation, the voltage rating of the components is usually higher, and the impedance of the filtering unit should be very high to block the flow of the fundamental harmonic. For the series compensation, the impedance for the fundamental components should be minimal. In order to improve the power quality, many control algorithms have been proposed for automatic and selective harmonic compensation. In this project to ensuring power quality both in the grid current and PCC by harmonic elimination is presented. The proposed method is developed to take care of harmonics in grid-connected (GC) mode, as well as in the islanded or standalone (SA) mode of operation, where the main objective is to remove the harmonics from the grid current and the point of common coupling (PCC) voltage. The suggested placement of the harmonic reduction unit dictates the use of a special controller structure that uses the harmonics magnitude in the dq reference frame. In the proposed control algorithm, the required amount of attenuation for harmonics is determined to meet the total harmonic distortion. Fast and efficient algorithm for phase detection irrespective of the presence of harmonics has been utilized for the system. The effectiveness of proposed method is verified by using Matlab/simulink software.

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INTRODUCTION

In the modern world of advanced technology there is an increasing demand for high quality, reliable power. While the utility industry is dedicated to providing undistorted and uninterrupted power to its customers, there will inevitably be lapses in the utilities' ability to maintain these commitments. This may be undesirable or unacceptable for certain commercial and industrial users. Thus, there has been a steady increase in the demand for reliable electronic power processing equipment at increasingly high power levels. The following sections describe some of the applications for high power Voltage. Source Inverters (VSIs) in today's world and beyond. For the purposes of this thesis, it will be assumed that all high power inverters referred to herein will be three-phase inverters, composed of either three or four phase legs. Uninterruptible power supplies (UPSs) are not a new technology. Static (solid state) UPSs were first developed in the 1960s [1-5] and have become a significant market to date. Most UPSs produced today are low-power backup supplies for computers in the event of utility outages. However, there are several applications for high power UPS systems. For example, large computer network servers and telecommunications equipment may require uninterrupted power in the tens to hundreds of kilowatts range [6-7].

In addition, semiconductor fabrication and other industrial processes require an extremely high level of power quality, because even short transients can disrupt the processes, resulting in loss of product. In the past, high power UPSs were generally fed by diesel engine-driven rotary systems as a backup [8-9]. However, these systems have a finite response time that results from switching the utility power line to the backup source.

This may be an unacceptable transient for a critical load. In order to achieve a truly uninterrupted power source for critical loads, an inverter preferred system, must be employed [10]. In such a system, a rectifier is used to charge a battery, which is in turn the source for an inverter that is constantly supplying AC power to the critical load. In the case of an inverter preferred UPS system for semiconductor.

In [11], the compensation of harmonic currents in three phase four-wire system has been achieved using hysteresis hand controller for both split-capacitor and Four-leg inverter topologies. But hysteresis hand

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controller results in continuously varying switching frequency and make high frequency filtering difficult. Whereas in constant switching frequency approach, the filter current tends to ride either the upper or lower hand depending on the switch duty cycle. Hence small amount of low order harmonics are present in the filter current and neutral wire current. Using the instantaneous reactive power theory [Z], it has been shown that the reactive power requirement of a three phase circuit can be compensated instantaneously without the requirement of energy storage device. In modified form, instantaneous reactive power theory [12-13] is also seen to compensate for reactive and harmonic components of load currents in balanced and unbalanced system. But the drawbacks of these schemes are expanded architecture, complex circuitry and need for real time calculations. Smedley and Qiao have proposed an approach based on Unified Constant-frequency Integration (UCI) control 141. This scheme gives satisfactory results to compensate reactive and harmonic currents in a three-phase system [14]. This scheme is not computation intensive and hence, there is no need for high performance processors. Also there is no need to sense utility voltages. Hence the information about zero crossing of supply voltage is not needed. This control method is based on one-cycle control and uses an integrator with reset to control the pulse width of an ac-dc converter so that current drawn by it, compensates the reactive and harmonic currents drawn by the non-linear loads.

II. PLACEMENT OF HARMONIC COMPENSATION UNIT IN MICROGRID SYSTEM

In conventional methods [13], [14], the series harmonics reduction units are placed at the grid side, as shown in Fig.1 where the objective is to make the line impedance at the harmonic frequency as high as possible. From Fig.1,

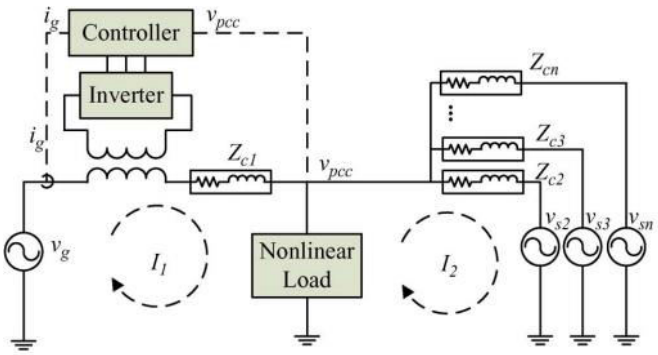

Fig.1.Conventional harmonic compensation method.

The mesh equations for the overall system for harmonic components can be written as follows:

$$I_{n_1} Z_{n_{c1}} + V_{n_{\text{inj}}} = V_{n_{\text{pcc}}} \quad (1)$$

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$$I_{n_2} Z_{n_{c2}} = V_{n_{\text{pcc}}} \tag{2}$$

Where $V_{n_{pcc}}, V_{n_{inj}}, I_{n_1} Z_{n_{c1}}$ represents the *n*th harmonic PCC voltage, injected voltage, grid current, and coupling

impedance, respectively. The grid current can be expressed as

$$i_g = I_1 = \sum_{n=1}^{N} A_{n_1} \sin(n\omega t + \theta n) \tag{3}$$

The injected harmonic voltage in series with the grid is proportional to the grid current such as

$$V_{n_{\text{inj}}} = k_n I_{n_1} \tag{4}$$

Where gain of $k_n$is related to the coupling impedance and the transformer turns ratio. Based on (1) and (4), I_{n_1}can be determined as

$$I_{n_1} = \frac{V_{n_{\text{pcc}}}}{Z_{n_{c1}} + k_n} \tag{5}$$

The compensation unit pushes voltage harmonics to make the grid current harmonics free; however, this voltage harmonics distort the PCC voltage. Moreover, during the SA mode of operation, the grid branch is disconnected making the compensation unit idle.

The proposed placement for the harmonics injection unit in this research is the distributed generation side, as shown in Fig.2. In this case, the objective of the harmonic compensation unit is to make the impedance in the sources of the micro grid side as small as possible to divert all the current harmonics far from the grid side.

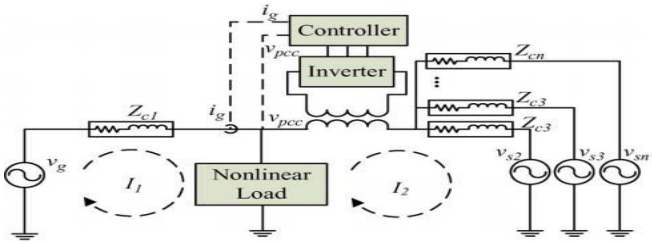

Fig.2. Proposed harmonic compensation method.

This way, if the grid voltage is harmonics free, the PCC voltage will become harmonics free. Moreover, when the grid is disconnected the harmonics reduction unit can continue to operate. The unit makes the PCC voltage harmonic free by providing harmonic voltage at its output that counteracts the harmonics results from the voltage drop at the coupling impedances away SA operation. For the harmonic components, the equation for mesh current I_1 and I_2 can be written as follows:

$$I_{n_1} Z_{n_{c1}} = v_{n_{\text{pcc}}} \tag{6}$$

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$$V_{n_{\text{inj}}} + I_{n_2} Z_{n_{c2}} = V_{n_L} \quad (7)$$

From (6) it is clear that if I_{n_1} is close zero then $V_{n_{pcc}}$ will be close to zero also. In literature, the inverters in the microgrid are controlled to share the current harmonics such that theharmonics in the PCC can be reduced. This approach can help in distributing the harmonics production across the sources, but it cannot insure that the total harmonic distortion (THD) at the grid current or at the PCC voltage is below the required limit. Having the compensation unit close to the PCC allows an easy access to the PCC voltage and the grid current, whereas the accessibility could be impractical for other sources due to the geographical spread of the micro grid. Then, the compensation unit can secure the harmonics free grid current and PCC voltage by diverting the harmonics to the side of the other sources, which can share the harmonics effectively through the techniques provided in.

III. CONTROLLER STRUCTURE

The overall block diagram of the controller structure is shown in Fig.3. The block diagram for the harmonics elimination unit is shown in Fig.4. The harmonics elimination unit mainly consists of two major blocks—harmonics estimation block and harmonics injection block. Efficient and effective harmonics estimation and the harmonics elimination methods, suggested and illustrated in Fig. 4, are used for phase detection and harmonics component estimation. As the existence of the harmonics affect the PLL accuracy, the first stage is used to eliminate the harmonics from the sampled grid signal ensuring accuracy of the PLL. The second stage provides fast and accurate harmonics estimation as the PLL produces an accurate phase. The harmonics injection block, which dictates the amount of harmonics injection by the harmonics compensator.

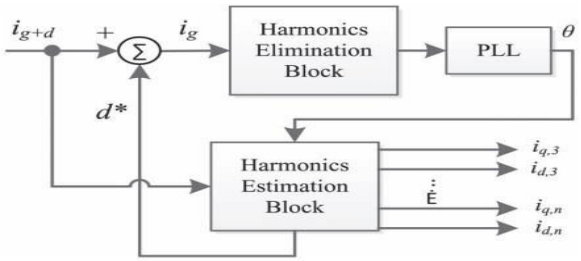

Fig.3. Overall, harmonic compensation block.

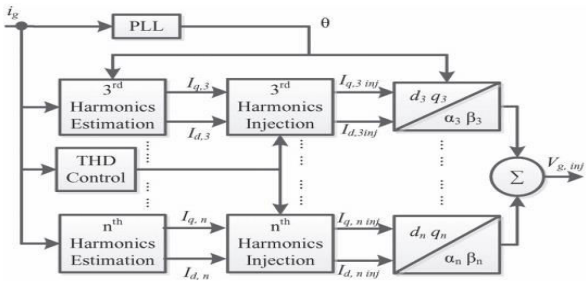

Fig.4. Harmonics elimination block diagram

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The grid current and/or the PCC voltage are fed to the phase locked look (PLL) block. The PLL lock extracts the phase of the fundamental component. Then, using the PLL output, the 3rd, 5th. . . n^{th} harmonics of these signals are estimated. The d_q components of the estimated harmonics are sent to the harmonics injection block to determine how much voltage at the specified harmonic frequency should be injected into the line based on the error between the actual and reference.

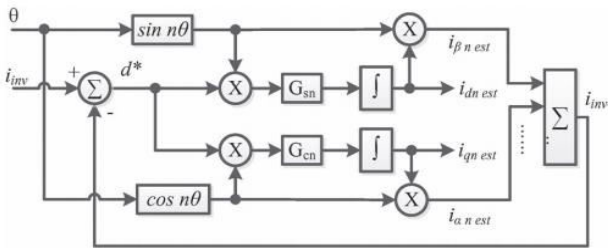

Fig.5. Harmonics estimation block.

The harmonics estimation block is used to estimate the amount of harmonics needed to be injected from the compensator. The block diagram for harmonics estimator is shown in Fig.5. The harmonics estimation is performed based on the phase provided by the PLL block. The closed-loop system provides the estimated voltage in both $\alpha\beta$ and d_q rotating reference frame for fundamental, as well as harmonics components. The transfer function for the harmonics estimation block can be written as

$$\frac{\hat{V}_{d,n}(s)}{V_{d,n}(s)} = \frac{0.5G_{\mathrm{sn}}}{s + 0.5G_{\mathrm{sn}}}. \tag{8}$$

According to IEEE 519, the individual harmonic components should be less than 3% and the THD should be less than 5% to ensure power quality. The reference value of THD in the THD control block, as shown in Fig.4, should be set according to this requirements. When the overall harmonics is reduced below the recommended THD, the amount of the injection for individual harmonics component is kept constant. This also ensures the system to operate in stable condition.

In the presence of non-integer harmonics or any other disturbances the measured current signal shown in Fig.3, can be expressed as

$$i_{g+d} = i_g + d \tag{9}$$

Where i_g is the grid current and d is the disturbance. The estimated disturbance can be expressed as

$$\hat{d} = i_{g+d} - \hat{i}_g = i_g + d - \hat{i}_g = err + d \tag{10}$$

Where, $\hat{i}_g$ is the estimated value of the current and *err* is the estimation error. The estimation error is expected to be much

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smaller than the disturbance ($err \prec\prec d$). The error *err* reflects the effect of *d* on the estimation of $\hat{\imath}_g$ which is attenuated significantly by the filters of the estimators (see Fig.5). Thus, $\hat{\imath}_g$ can be described as

$$\hat{i} = i_{g+d} - \hat{d} = i_g + d - err - d = i_g - err. \quad (11)$$

Since *err* will go to zero after a couple iterations, $\hat{\imath}_g$ will become error free. Thus, PLL will not be affected by the presence of non-integer harmonics.

IV.CONTROLLER OPERATION

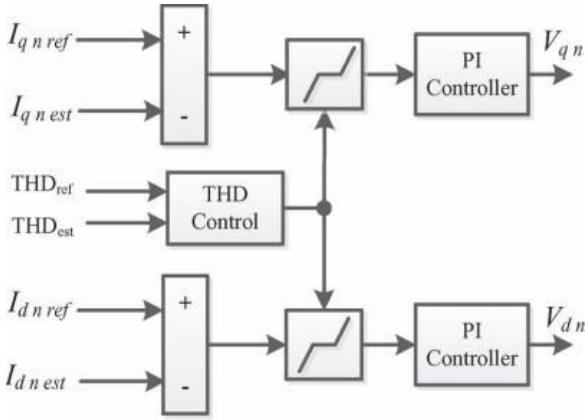

Fig.6. Harmonics injection unit.

Fig.5 illustrates the block diagram of the harmonics injection unit, where the desired amounts of harmonics are commanded in d_q reference frame. Desired THD level is also provided as a reference into the controller block. The THD control block receives the commanded THD and actual THD of the grid current or voltage at PCC. The THD reference is usually set according to the required power quality. The *d* and *q* component of the harmonic current or voltage should be reduced to eliminate harmonics from the system.

This scheme ensures that in the absence of any particular harmonics, the compensation unit will not inject any extra harmonics to the system (see Fig.6). The PI controller is responsible for reducing the harmonics components below the specified limit. After the THD level reaches below the allowable limit, the PI controller output stabilizes and continues to inject the particular amount of harmonics. The flow diagram of the overall harmonics elimination process of grid current and PCC voltage is provided in Fig.7.

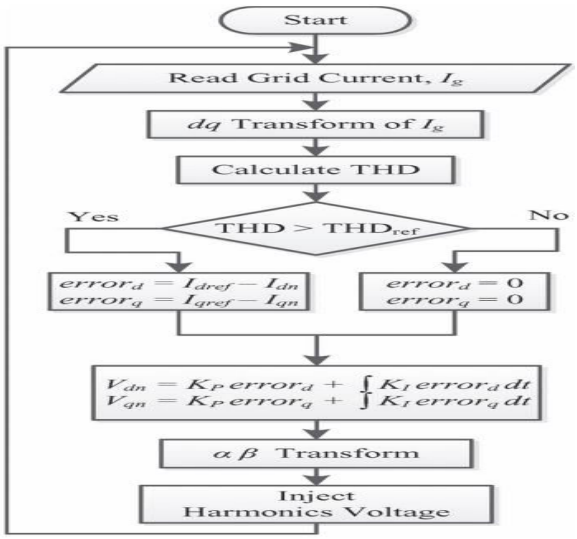

Fig.7. System Flow Diagram.

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The harmonic resonance condition may occur due to the capacitors connected to a micro grid. The control of harmonic resonance can be achieved through tuning the virtual impedance in the micro grid controller. Increasing the virtual impedance will result in limiting the harmonic current flow.

To design a PI controller for harmonic compensation, an approximate model for the equivalent system is derived in d_q rotating reference frame, as shown graphically in Fig.8. The differential equations for the systems can be written as

$$L\frac{di_d}{dt} = -Ri_d + v'_{dh} + \omega Li_q - v_{dh} \quad (12)$$

$$L\frac{di_q}{dt} = -Ri_q + v'_{qh} + \omega Li_d - v_{qh} \quad (13)$$

In the Laplace domain (12) and (13) can be written as

$$sLI_d = -RI_d + V'_{dh} + \omega LI_q - V_{dh} \quad (14)$$

$$sLI_q = -RI_q + V'_{qh} + \omega LI_d - V_{qh} \quad (15)$$

The transfer function can be expressed in terms of the PI controller (*kp,ki*) and harmonics estimation gain, *G*, as shown in Fig.5, as

$$V'_{xh} = \frac{k_p s + k_i}{s}\frac{G}{s+G} i_x \quad (16)$$

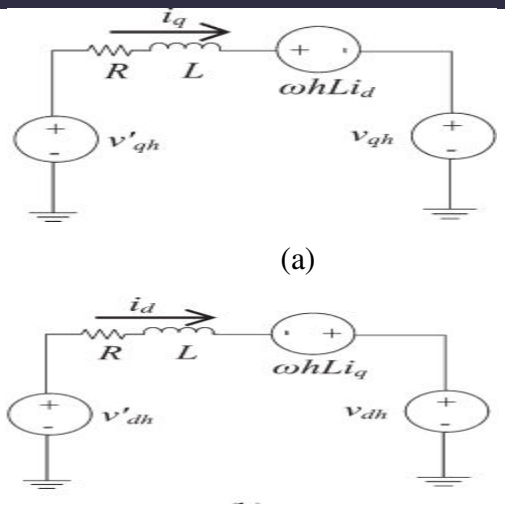

Fig.8. Equivalent (a) *q* component (b) *d* component circuit for PI controller design.

V. VOLTAGE SOURCE INVERTER

In order to demonstrate the control techniques described in this thesis, it is useful to show simulation results based on a specific example. For this purpose, a single inverter model is developed and used throughout this document. The switching and average models described below are based on a three-phase, four-leg inverter rated at 90 kVA with a 115 Vrms, 400 Hz output.

A. Inverter Switching Model

The switching model of the inverter is developed in order to be as close to a truth model as possible. This model should give accurate time domain waveforms for the inverter under various loading conditions

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and transients. Figure 9 shows a schematic of the inverter switching model. The fourth leg enables control of the neutral current. In three-phase, three-leg inverters, if the load requires a neutral connection, this point is usually connected to the neutral point of the filter capacitors or to the midpoint of the DC link. When this is the case, unbalanced loads or single phase non-linear loads will cause neutral currents to flow and zero sequence distortion. When a fourth leg is employed, the neutral point is controlled, and zero sequence distortion can be reduced through control strategies.

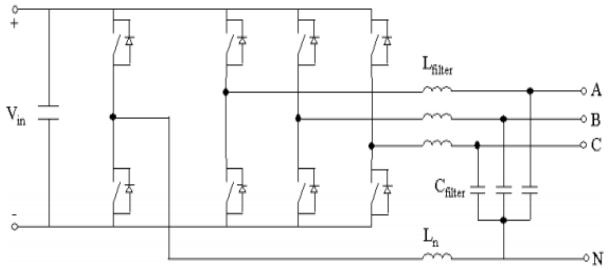

Figure .9.Schematic of the switching model of a four-leg inverter.

VI.MATLAB/SIMULATION RESULTS

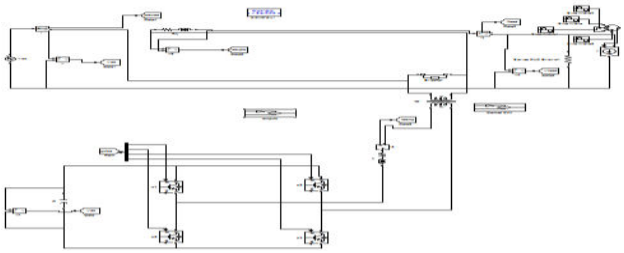

Fig 10 Matlab/simulation circuit of Conventional harmonic compensation method.

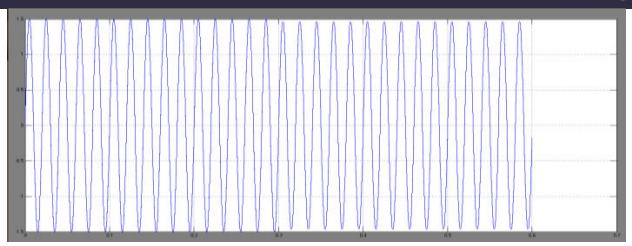

Fig 11 simulation wave form of current source

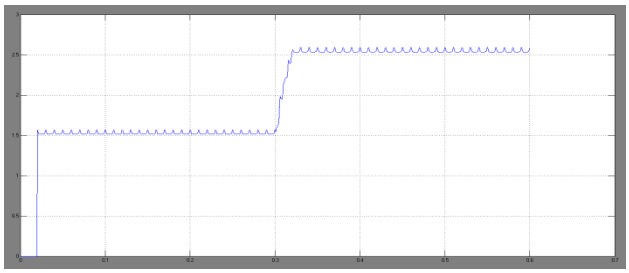

Fig 12 simulation wave form of Total Harmonic Distortion source current

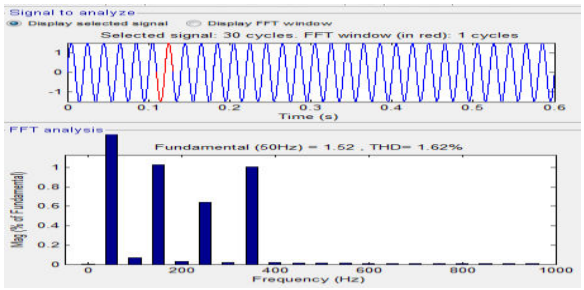

Fig 13 FFT analysis of the critical load current before the compensation is applied

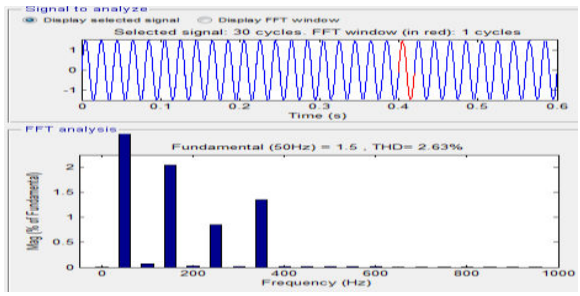

Fig 14 FFT analysis of the critical load current after the conventional compensation method is applied.

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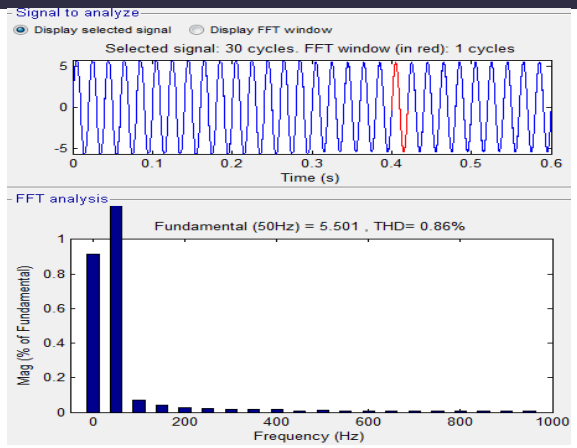

Fig 15 Grid current in conventional method before and after applying harmonic compensation.

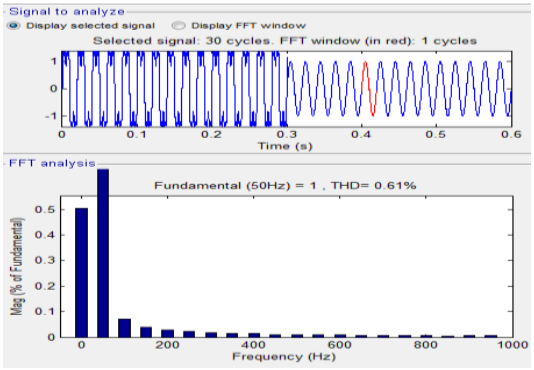

Fig.16.FFT analysis of the critical load current after the proposed compensation method is applied.

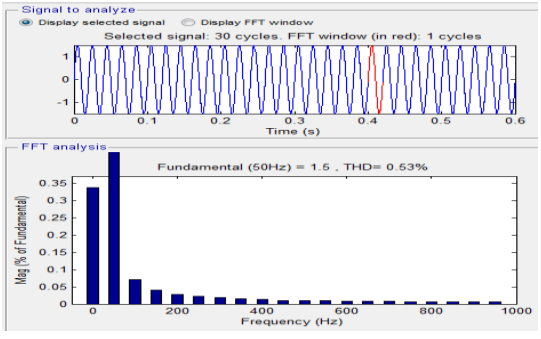

Fig 17 FFT analysis of the critical load current before the compensation is applied.

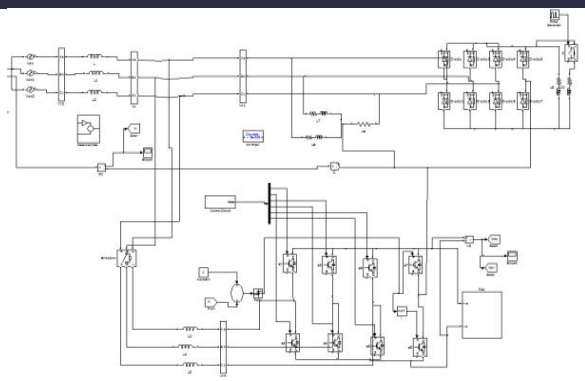

Fig 18 Matlab/simulation circuit of harmonic compensation method with three phase source industrial application

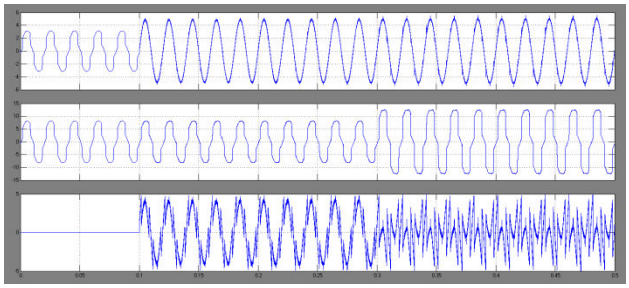

Fig 19 simulation wave form of single phase voltage and current source.

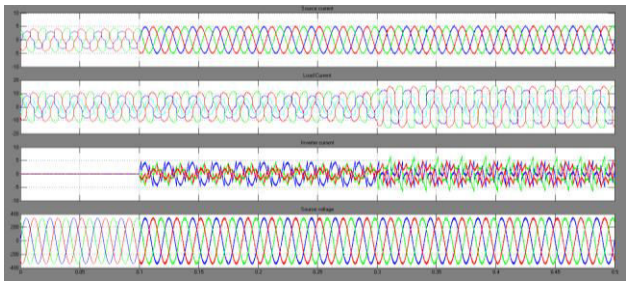

Fig.20. simulation wave form of three phase source and load current, inverter current and source voltage.

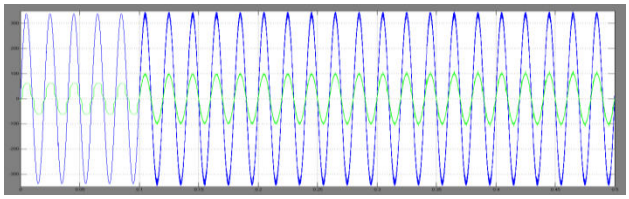

Fig 21 Simulation Wave Form Of Power Factor Correction.

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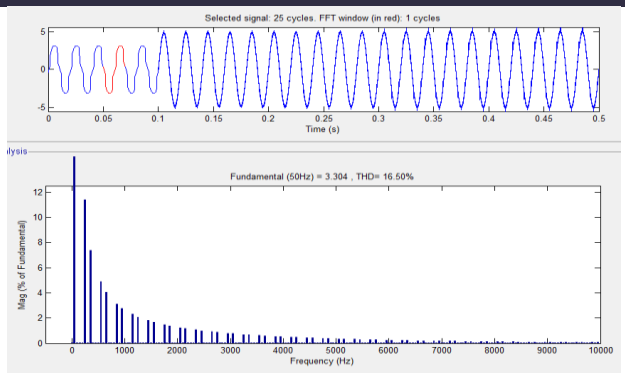

Fig.22.source current THD For before compensations.

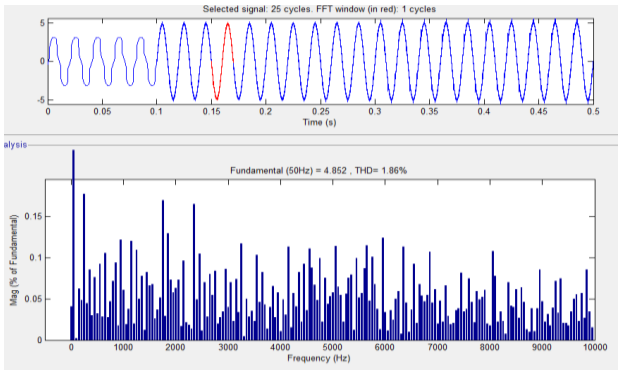

Fig.23.Source Current THD For After Compensations.

VII.CONCLUSION

The research reported in this thesis has focused on the interesting challenges presented to inverter-fed, high power systems by specific loading conditions. No-load,unbalanced loading, and non-linear loading each have unique characteristics that negatively influence the performance of the VSI. Ideal, infinitely stiff systems are uninfluenced by loading conditions; however, realistic systems, with finite output impedances, encounter stability issues, unbalanced phase voltage, and harmonic distortion. The research reported in this thesis has taken a control approach to solve these problems. The traditional solution to lightly loaded or unloaded conditions is simply to design low controller bandwidths, such that stable operation of the VSI is ensured. While this approach effectively addresses the problem, the result will be very poor transient performance of the system. The use of an inner current control loop has been shown, through theory and simulation, to provide increased damping of the filter poles at light load, enabling the voltage control bandwidth to be increased. For the system example in this paper, the control bandwidth was improved by and order of magnitude, significantly enhancing transient performance. The proposed injects a voltage to counteract the harmonics in the system and reduce the THD to desired levels.An improved based harmonic elimination technique has been applied in this paper for control of inducti on motors and the various simulations has been performed on Simulink.

REFERENCES

[1].Saeed Anwar, Ali Elrayyah, and Yilmaz Sozer, Senior Member, IEEE"Efficient Single-Phase Harmonics EliminationMethod

for Microgrid Operations"IEEE Transactions On Industry Applications, Vol. 51, No. 4, July/August 2015

[2] R. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," 2nd Ed., Springer Science+Business, 2001, Ch.18.

[3] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "Frequency Response Analysis of Current Controllers for Selective Harmonic Compensation in Active Power Filters," IEEE Trans. Power Electron., vol. 56, no. 2, pp. 1826–1835, Feb. 2009.

[4] F. Blaabjerg, R. Teodorescu, M. Liserre, A. Timbus,"Overview of Control and Grid Synchronization for Distributed Power Generation Systems," IEEE Trans. Ind. Electron., vol. 53, pp. 1398-1409, Oct. 2006.

[5] M. Brenna, G.C. Lazaroiu, G. Superti-Furga, and E. Tironi, "Bidirectional Front End Converter for DG With Disturbance Insensitivity and Islanding-Detection Capability," IEEE Trans. Power Delivery, vol. 23, no. 2, pp. 907-914, April 2008.

[6] T. Kerekes, R. Teodorescu and U. Borup, "Transformer less Photovoltaic Inverters Connected to the Grid," in Applied Power Electronics Conf., APEC 2007 - Twenty Second Annual IEEE, pp. 1733 – 1737, Feb. 2007-March 2007.

[7] M. Dai, M. Marwali, J. Jung, and A. Keyhani, "Power flow control of a single distributed generation unit," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 343–352, Jan. 2008.

[8] D. Ben Attous and Y. Bekakra, "Speed Control of a Doubly Fed Induction Motor using Fuzzy Logic Techniques", International Journal of Electrical Engineering and Informatics, Vol. 2, No. 3, December 2010.

[9] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," IEEE Transactions on Industry Applications, vol. 36, pp. 834–841, May/June 2000

[10] Kennedy, James. "Particle swarm optimization." Encyclopedia of Machine Learning. Springer US, 2010. 760-766.

[11] Moradi, M. H., and M. Abedini. "A combination of genetic algorithm and particle swarm optimization for optimal DG location and sizing in distribution systems." International Journal of Electrical Power &Energy Systems 34.1 (2012): 66-74.

[12] Gandomi, Amir Hossein, et al. "Chaos-enhanced accelerated particle swarm optimization." Communications in

Nonlinear Science and Numerical Simulation 18.2 (2013): 327-340.

[13] X. Yu and A. M. Khambadkone, "Combined active and reactive power control of power converter building block to facilitate the connection of micro-grid to Electric Power system," in Proc. IEEE ECCE, 2009, pp. 1444–1450.

[14] M. Rahmatian, M. J. Sanjari, M. Gholami, and G. B. Gharehpetian, "Optimal control of distribution line series compensator in micro grid considering fault current limitation function," in Proc. 17th Conf. EPDC, May 2012, pp. 1–5.