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SINGLE AND DOUBLE-ADJACENT ERROR CORRECTING PARALLEL DECODER USING GOLAY CODES

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ABSTRACT: In this paper we are going to implement the encoding algorithm in field programmable gate array prototype for the purpose of Golay codes. Generally, golay code is an error correction code which performs very close to Shannon's limit. Reliable communication is needed to obtain good performance in the system. In this paper two golay codes are used one is binary golay code and extended golay code. Binary golay code is represented as 8 and coming to extended binary golay code is represented as 16. Here for golay encoder a high speed low latency architecture is designed in virtex-4 FPGA. At last depending upon the likelihood decoding technique an optimized and low complexity decoding architecture is presented.

KEY WORDS: Golay code, encoder, decoder and field programmable gate array.

I.INTRODUCTION

As we know that communication system transmits data from source to destination by using a channel or medium. Depending upon the channel medium and external noise the received data becomes reliable. This received data consists of external noise, because of this interference occurs in the signals. Now Shannon introduces coding theorem where reliable transmission is achieved if data is less than the channel capacity. In this the error correction and detection codes are obtained by adding the redundant symbols in original data which are known as Error Correction Codes (ECC). The main advantage of this error correction code is that it is helpful for long distance one way communication like satellite communication and deep space communication. The error correction codes are used in wireless communication and storage devices. The both error correction and detection code transmits the error less

data in noisy channel. Here the error detection is used to detect the errors obtained in the receiver and error correction is used to correct the errors which are received by the receivers. There are different types of error correction codes, depending upon the property we will use the error correction code. Error correction codes are classified as block codes, convolution codes, low density parity check code and Golay code. To address the error correction codes golay code is used and it plays vital role in many applications like code excitation for LASER and ultrasound imaging. To generate a golay code an automatic pattern generator is used which is high cost. To overcome this hardware module is programmed by yielding a golay encoded code word. For the purpose of forward error correction golay decoder is used in communication links. At last we can conclude that high speed and high

throughput hardware decoder is used in forward error correction.

II. EXISTED SYSTEM

In existed system an extendable golay code is used. The extendable golay code is obtained by adding parity check bit to the golay code. This extended golay code will has minimum distance of eight and it correct 3 bit errors and detect 4 bit errors. The decoding of the Golay code is done in a series of steps and requires several clock cycles. The existing SEC-DAEC decoders are similar to SEC decoders but they need to check also the syndrome values that correspond double adjacent errors. This requires roughly doubling the number of comparisons. Then, the correction of each bit is triggered by three syndrome values. This results in a decoder that is significantly more complex than a simple SEC decoder. The proposed parallel decoder as discussed before has the objective of correcting single and double-adjacent bit errors. The first step is to place the bits in the memory such that data and parity bits are interleaved. This interleaving has no impact on memory performance, as it is a simple remapping of the bits when they are read from or written to the memory. Let us now consider the syndrome values for an error on the second bit (first data bit), a double adjacent on bits one and two, a double adjacent on bits two and three, and a triple adjacent on bits one, two, and three. From below figure (1) we can observe the parity check of golay code.

Fig. 1. Parity check matrix of golay code

III. PROPOSED SYSTEM

From below figure (2) shows the block diagram of proposed system. The VLSI-architecture for soft-decision decoding of the 16 Golay code with parity-check operation is shown in Fig. 2. This high-speed soft-decision decoder processes simultaneously four parallel hard-decision operations in parallel structure. Thus, a high data rate can be achieved in the range of hundreds of M bits/s.
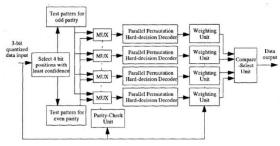

FIG.2. PROPOSED SYSTEM

Craig K. Rush forth described an efficient bit-serial Very Large Scale Integrated (VLSI) implementation of the exact maximum-likelihood decoding of the Golay (16, 8) Code in the additive white Gaussian noise channel. The design consists of two chips developed using Path Programmable Logic (PPL) and an associated system of automated design tools for 3μm NMOS technology. They have estimated that their decoder will produce an information bit every 1.6-2.4μs. Higher speeds can be achieved by using a faster technology or by replicating the chips to perform more operations in parallel.There are two closely related binary Golay Codes. The extended binary Golay Code encodes 12 bits of data in a 6-bit word in such a way that any 3-bit errors can be corrected or any 3-bit errors
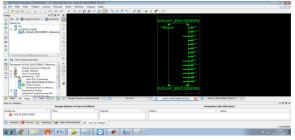
can be detected. The other, the perfect binary Golay Code has code words of length 16 and is obtained from the extended binary Golay Code by deleting one co-ordinate position. In standard code notation the codes have parameters [16,8] corresponding to the length of the Code words. the extended binary Golay Code consists of a dimensional subspace W of the space words such that any two distinct elements of W differ in at least eight coordinates. In the extended binary Golay Code, all code words have the Hamming weights of 0, 8, 12, 16. The binary Golay Code leads us to the extended Golay Code. Codes can be easily extended by adding an overall parity check to the end of each Code word.
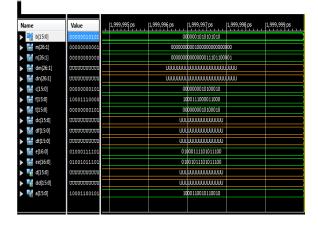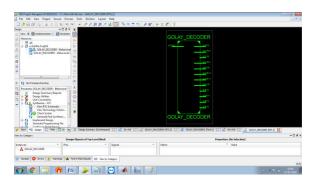
IV. RESULTS

FIG.3. RTL SHEMATIC OF GOLAY ENCODER

FIG. 4. GOLAY ENCODER OUTPUT
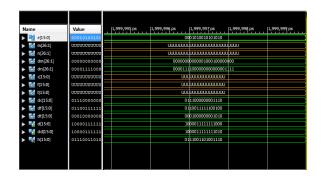

FIG. 5. RTL SCHEMATIC OF GOLAY DECODER

FIG. 6. GOLAY DECODER OUTPUT

V. CONCLUSION

In this paper, the Golay Code and operation for various encoder and decoder is discussed. This encoding and decoding algorithm have been successfully applied to short block codes such as Golay Code. Decoding algorithm consists of syndrome measurement unit, weight measurement unit and weight constraint. From approximated count of reduction the number of gates resulting in minimizing the area and improved latency of 16 clock cycles in the Decoder Architecture. Improved Latency of the Encoder Architecture. The purpose of this thesis is to review the published encoding and decoding models in the literature and to critique their reliability effects. We will try to reduce the area, Maximum Combinational Path Delay

(MCPD) of decoding algorithm of Golay Code.In future we can compress these golay codes up to (8,4) and provide the high security. We can apply these codes in G.F operation for high security applications.

VI. REFERENCES

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