COPY RIGHT

Title: **LOW POWER CONSUMPTION FOR ECG ACQUISITION SYSTEM WITH 0.3V SUPPLY**

Paper Authors

VASANTH KAMATH V,DR. M. MAHESH

Universal College of Engineering & Technology, Guntur

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

LOW POWER CONSUMPTION FOR ECG ACQUISITION SYSTEM WITH 0.3V SUPPLY

VASANTH KAMATH V[1], DR. M. MAHESH[2]

[1]PG Student (M Tech) Dept. of ECE at Universal College of Engineering & Technology, Guntur

[2]Associate Professor, Dept Of ECE at Universal College of Engineering & Technology, Guntur

Abstract: New power-efficient electrocardiogram acquisition system that uses a fully digital architecture to reduce the power consumption and chip area. The proposed architecture is compatible with digital CMOS technology and is capable of operating with a low supply voltage of 0.3 V. In this architecture, no analog block, e.g., low-noise amplifier (LNA), and filters, and no passive elements, such as ac coupling capacitors, are used. A moving average voltage-to- time converter is used, which behaves instead of the LNA and anti aliasing filter. A digital feedback loop is employed to cancel the impact of the dc offset on the circuit, which eliminates the need for coupling capacitors. The circuit is implemented in 0.13-um CMOS process. The simulation results show that the front-end circuit consumes 18.4pW of power.

Key words: Anti aliasing, area efficient, digital integrated circuit (IC), electrocardiogram (ECG), low power, moving average filtering, offset cancellation, sensor interface.

I. INTRODUCTION

BIOMEDICAL devices are becoming more popular. This is due to the rapid advancement of integrated circuit(IC)fabrication. Such devices are being used as wear able or implantable gadgets as well as monitoring equipment. In all these applications, the bio signal is first preconditioned and converted to digital. A digital signal processor then processes the digital data form unitoring or diagnosis applications. Biomedical signal acquisition systems[1]–[5]typically consist of alow noise amplifier(LNA),a band pass filter, an analog sample-and-hold, and an analog-to digital converter(ADC),as shown in Fig. 1(a). While the architecture shown inFig.1(a)is typically used, in some cases chopping technique issued to reduce the impact of the flicker noise, as showing Fig. 1(b)[6]–[8]. With the advancement of

CMOS technology, the supply voltage is being reduced, which decreases the voltage head- room for analog block of an IC. Although the technology scaling leads to lower power consumption and higher performance in digital circuits; many parameters [such as signal-to noise ratio(SNR),dynamic range, gain, and soon] of
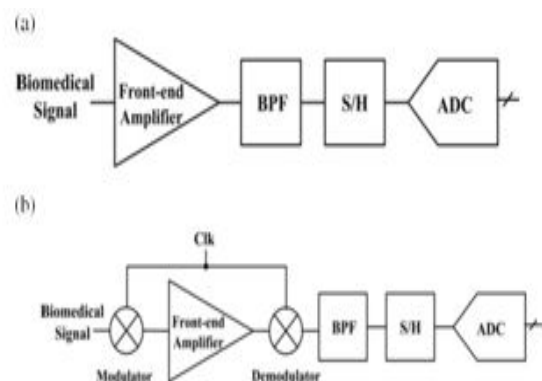

Fig. 1. Biomedical signal acquisition system. (a)Conventional based. (b) Chopperbased.
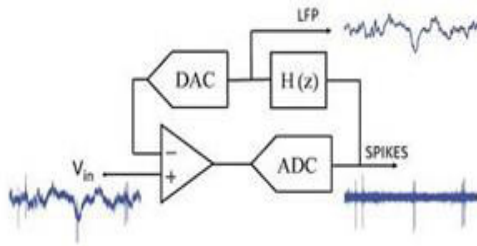
Fig. 2. Mixed signal feedback architecture [10].

The analog parts of an IC are negatively impacted. Therefore, it is desirable to find new architectures, in which more digital blocks are used. Recently, a few methods, which are based on digital techniques, are introduced [9], [10]. The block diagram of the system designed in [10] is shown in Fig. 2. In this circuit, many of the functions that are typically implemented by analog blocks are performed by digital circuits. Using this digitally enhanced approach can help increase the flexibility of the system in removing unwanted interferences. Moreover, digital calibration techniques can be used more easily. Eliminating the interferences at the input of the system, before substantial gain is applied, can relax the dynamic range requirements and minimize the supply voltage. This can lead to reduce the overall power consumption and area; both of which are critical for implantable and multi electrode systems [9]. This is achieved using mixed signal feedback and digital blocks [9], [10]. Hence, it appears that the use of digital techniques in the implementation of these systems can lead to a better performance and better compatibility with digital CMOS technology.

TABLE I
POWER BREAKDOWN BY BLOCK [10]

	Power
Merged Amplifier-DAC	$4.13\,\mu W$
Summing Amplifier & DAC	$0.66\,\mu W$
ADC	$0.24\,\mu W$
Digital Filters	$0.1\,\mu W^{\circ}$

°Estimated

Table I shows the power breakdown by block of the circuit in [10]. As can be seen, the amplifier; the only analog block that is used, consumes most of the power. Hence, if we can replace the amplifier with an appropriate digital block, the circuit will be more efficient in terms of power. However, there are other issues that should be addressed before moving toward fully digital implementation. Two of these issues are as follows.

1)   Removing the DC Offset Voltage of Electrodes without Passive Elements: In these systems, a dc offset voltage as large as 50 mV is associated with the electrodes. Typically this offset is removed by ac coupling the instrumentation amplifier with the electrode [1]–[3]. This is not very desirable, since it requires large capacitors.

2)Providing a Solution for Anti aliasing Filter: Anti aliasing is typically done by low-pass analog filters [9]. Box car sampling technique can be a solution for the fully digital implementation[10]. Motivated by the above-mentioned issues, we have designed a new fully digital electrocardiogram (ECG) signal acquisition system. The circuit is designed in 0.13-um CMOS technology and operates by a supply voltage of 0.3V. Using the proposed architecture, the area and power

International Journal for Innovative
Engineering and Management Research
A Peer Reviewed Open Access International Journal

www.ijiemr.org

consumption are reduced. In Section II, the architecture of the proposed fully digital front end is introduced. In Section III, the proposed offset cancellation algorithm is discussed, and the MATLAB simulation results are presented. Section IV details the design of the individual circuit blocks. Simulation results are provided in SectionV. Finally, the conclusion is drawn in Section VII.

II.   PROPOSED FULLYDIGITAL FRONT-END ARCHITECTURE

Fig. 3(a) shows the block diagram of the proposed fully digital architecture. In this structure, the processing of the biosignal is performed in the time and digital domain. Hence, the advantages of digital CMOS technology are utilized. The analog biosignal coming from the electrode is directly connected to the front-end circuit and is converted to time with a voltage-to-time converter (VTC). From this point on in the circuit, the signal information is in the phase of the VTC output signal. The output of the VTC is applied to the time-mode processing block, in which the antialiasing and offset cancellation are done in time domain. Then, a time-to-digital converter (TDC) transfers the time-mode signal into digital domain where other processes (digital filtering, data compression/reduction, and soon)are performed.
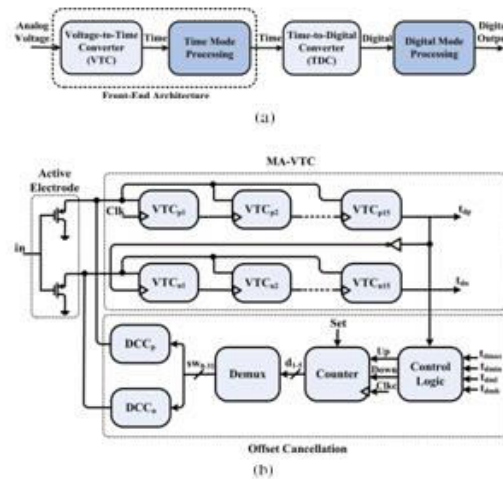

Fig.3.   (a) Overall block diagram of the proposed system. (b) Proposed digital front-endarchitecture.

The proposed digital architecture is shown in Fig. 3(b). It consists of an active electrode, two digital-to-current converters (DCCs), a moving average VTC (MA-VTC), a control logic block, a counter, and a demultiplexer. In this architecture, ac coupling capacitors are removed, and the impact of the electrode offset on the circuit is cancelled via a feedback loop. The technique used for the offset cancellation will be described in Section III. As explained earlier (Fig. 1), in conventional bio signal acquisition systems, an LNA is used after the electrode. In the proposed architecture, this block is removed. In the following text, each of the blocks of the proposed architecture is explained.

A.Active Electrode

An active electrode is an electrode, in which some active elements are used to reduce the power line interference [11]. Fig. 4 shows two different two-wired active electrodes for comparison [11]. The circuit in Fig. 4(a) uses an op-amp, while the one in Fig. 4(b) is implemented using a single transistor. In [11], important parameters of such

electrodes, such as offset, noise, gain, and output resistance, are compared. It is shown in [11] that the circuit in Fig. 4(b) has a superior performance in terms of noise, common mode rejection ratio (CMRR), and power consumption compared with the circuit of Fig. 4(a). However, the offset and the output resistance are worse. Since, in ECG applications, the most important limiting factor is the input noise of the system, we have used the active electrode with a single MOS transistor.

B.Voltage to Time Converter(VTC)

In the proposed digital implementation, the analog input voltage is converted to a measurable time via a VTC at the first stage. The signal information is now in the delay of the clock signal (CLK). The VTC should be designed in such a way that the small amplitude of the input voltage generates.

Fig. 4. Active electrode with either (a) an op-amp or (b) a MOS transistor, both operating as a voltage follower[11].

Fig. 5. VTC_n and VTC_p characteristics.

a large enough delay, linearly. In order to have time-domain amplification and acceptable SNR, we have used 15 stages of positive VTC (VTCp) and 15 stages of negative VTC (VTCn). The delays versus input voltage of VTCp and VTCn are shown in Fig. 5. As the input voltage becomes larger, the delay of VTCp increases, while the delay of VTCn decreases. We have used both the positive and the negative VTCs in our design to implement a moving average filter (as will be explained later). The cascaded stages of VTCs form delay-line structures. A major advantage of the delay-line-based structure lies in its all-digital implementation. In addition, the delay- line structure introduces time-domain amplification into the design. In particular, the input signal can be amplified in the time domain by simply extending the time window (using more VTC stages). This is in contrast to voltage amplification involving complicated analog amplifiers in the conventional systems[12].

C. Moving Average Filtering

Since, VTCs work with a clock and are broadband compared with the signal bandwidth, not using an anti aliasing filter before VTCs would lead to out-of-band noise aliasing. To pre-vent aliasing and to avoid having an analog filter in the design, wehavedevelopedthestructureshowninFig.6f orconverting the voltage-to-time as well as anti aliasing filtering. In this structure, a chain of 15 positive VTCs are followed by another chain of 15 negative VCTs. This configuration generates a since function and is behaving similar to an anti aliasing filter.
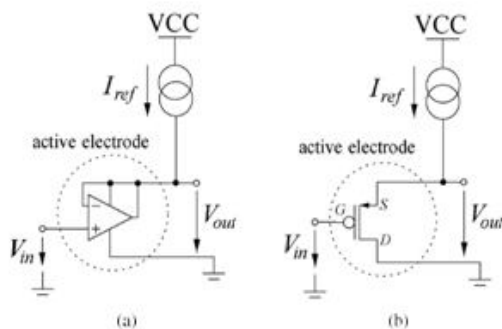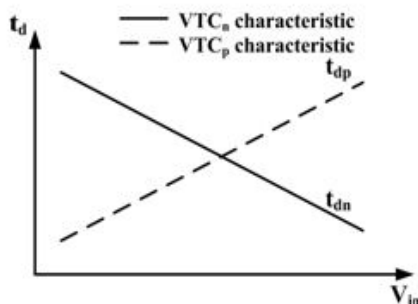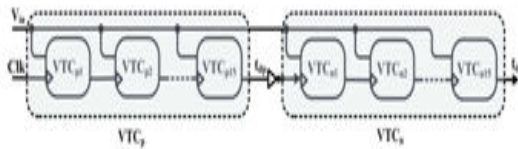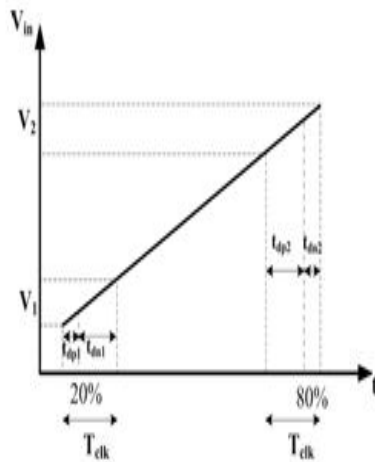
Fig. 6. Schematic of the MA-VTC circuit.

Fig. 7. Delays of VTC$_p$ and VTC$_n$ blocks for two different inputs.

In another word, the moving average filter is merged with VTCs, and hence we call this block MA-VTC. Therefore, the anti aliasing filtering is being done without using any passive component or analog amplifier. In [9], anti aliasing filtering is done by large-area and power hungry analog implementation. The moving average feature of the MA-VTC can be explained intuitively as the following. The CLK signal travels through the chain of VTCs. When CLK is passing through the first stage, the delay proportional to Vin should be generated. However, this delay maybe shortened/lengthened by the noise. This small variation of the delay happens in all the stages. At the output of the last stage, the overall delay is the sum of the delays of

the individual VCTs. As a result, the high-frequency noise, that has caused the delay variations, is cancelled out by the sum operation. This noise cancellation is more effective when the averaging happens during the whole clock period. To achieve this, a negative VTC block succeeds the positive VTC block. This can be explained by Fig. 7. If the input is small, V1, VTCp block will generate a small delay, tdp1in Fig. 7 (e.g., 20% of Tclk), and VTCn block will produce a large delay, tdn1in Fig. 7 (e.g., 80% of Tclk). The sum of these delays is constant and equal to Tclk. As Vin increases (e.g., V2) tdp rises and tdn decreases (e.g., tdp2is 80% of Tclk and tdn2is 20% of Tclk). In this case, the sum of the tdp and tdn is still Tclk. This is valid for any other input amplitude. Having tdp and tdn, Vin can be recovered based one quations presented in Section II- Dof this paper.

According to the above explanation, the output of MA-VTC is the average of Vin over a period of CLK signal. Actually, the proposed circuit integrates signal in a time window Tclk. Each VTC in the chain integrates the signal over a limited time period which depends on the delay of that VTC. For example, the first VTC integrates the signal from the rising edge of the clock to the time equal to the delay of this VTC. The second VTC integrates the signal from the rising edge of the output of the first VTC over a time period determined by its delay. This happens for all the VTCs in the chain. The sum of these integration periods is equal to the clock period. Hence, the integration over this time window can be represented by

$$Y(T_s,t)=\frac{1}{T_s}\int_{t-T_s}^{t} V_{in}(\tau)d\tau,\qquad(1)$$

Therefore, its impulse response is a rectangular pulse in the range of $[0,T_s]$

$$h(t)=\frac{1}{T_s}\int_{t-T_s}^{t}\delta(\tau)d\tau=u(t)-u(t-T_s).\qquad(2)$$

Hence, its frequency response is a sinc function

$$H(j\omega)=\frac{2\sin((T_s/2)\omega)}{\omega T_s}.\qquad(3)$$

In this way, the moving average filtering is embedded in the MA-VTC, preventing aliasing of the wideband noise.

D. Clock Frequency and Signal Recovery

VTC_p and VTC_n blocks are designed in such a way that the absolute slopes of their characteristic curves (Fig. 5) are equal. Hence, for any input voltage, wecan write

$$t_{dp}+t_{dn}=t_{tot}=\text{Constant}.\qquad(4)$$

The delay time tdp (or tdn) of a VTC gate is supposed to be a linear function of its input voltage and is given by

$$t_{dp}=aV_{inp}+\beta_1\qquad(5)$$
$$t_{dn}=-aV_{inn}+\beta_2\qquad(6)$$

Where V_{inp} and V_{inn} are the input voltage during the time interval that the clock pulse passes through VTC_p and VTC_n, respectively. In addition, a and $\beta_{1,2}$ are constants. The clock period, T_{clk}, must be chosen such that for the maximum variation of the input $t_{dn}$is not zero and is always measurable. Therefore, the clock period should be slightly more than t_{tot}. Hence

$$T_{CLK}\geq t_{dp}+t_{dn}=a(V_{inp}-V_{inn})+\beta_1+\beta_2.\qquad(7)$$

The outputs of the digital front end are t_{dP} and t_{dn}. These delays are converted to two digital numbers (D_P and D_N) by two

TDCs. The digital number corresponding to the input voltage, D_{in}, can be obtained from

$$D_{in}=\frac{D_{\beta}-D_{\alpha}}{2D_{\alpha}}+\frac{D_{\beta 2}-D_{\beta 1}}{2D_{\alpha}}\qquad(8)$$

where Dα, Dβ1, and Dβ2 are digital numbers of α, β1,and β2, respectively.

III. PROPOSED OFFSET CANCELLATION TECHNIQUE

The ECG signal acquisition system shouldbe capable of rejecting the dc polarization voltage of the bio potential electrodes, appearing as a dc offset at the input. This requires a high-pass filter (HPF) with a cutoff frequency <1 Hz. This filter requires large capacitors and on-chip implementation of such a filter is not efficient in terms of area. In the proposed architecture, a new offset cancellation technique issued ,in which offset cancellation is done in two stages.
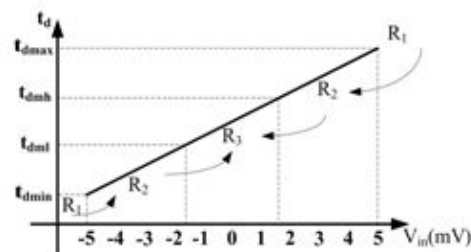

Fig. 8. Characteristic of the VTCp in the ±5-mV range.

First, the impact of the offset on the VTCs are eliminated, such that none of the VTCs are saturated. This is achieved by a digital feedback loop and allows the circuit to take the value of the offset to the digital output. In the second stage, the offset can be removed in the digital domain. In our design, we have assumed an offset voltage

of 50 mV. As will become clear later, the proposed system can be easily redesigned to accept even larger offsets.

A. Algorithm

Large amounts of electrode offset make the MA-VTC circuit nonlinear and saturated, to avoid this; we designed MA-VTC circuit, such that it is linear for twice the maximum ECG signal amplitude. The impact of the offset is cancelled by the following algorithm. Fig. 8 shows the characteristic of VTCp. The VTC is linear in the range of 5 to 5 mV. This linear region is divided into two regions of R2 and R3. R2 is related to the region for which tdmh<td<tdmax or tdmin<td<tdml. Similarly, R3 shows the region for which tdml<td<tdmh. Besides R2 and R3 regions, R1 represents regions, in which the input is out of predefined linear range, 5 mV, of the VTC (i.e., the delay is more than tdmax or less than tdmin). Assuming that the maximum amplitude of the input signal is 2.5 mV, the delay goes in the R1 region if the value of the offset exceeds 2.5 mV. In this case, due to the offset, the circuit behaves nonlinear and may be saturated. When the input falls in the R1 region, offset cancellation block distinguishes this by comparing tdwith tdmax/tdmin, and reduces the offset, such that the circuit goes back inR3.TheDCCblock[Fig.3(b)]is in the charge of this shift of the operation region. With reducing the Offset and putting the circuit in the R3 region, the operation remains linear. The R2 region is considered in order to add a hysteresis to the system so that the offset cancellation block does not activate very frequently.This algorithm is

first simulated with MATLAB to verify its functionality (circuit-level simulation results are reported in Section IV). In MATLAB the delay is compared with td max and td min. If the offset is detected, a voltage is added to or subtracted from the input. At the end, a residual offset of <5 mV may remain, which is tolerable for the circuit. Fig. 9(a) shows the simulation result for a sinusoidal input voltage with 2-mV amplitude and 100-Hz frequency superimposed on a 0.3 Hz, 50-mV sine wave (as an offset voltage).A scan be seen, the output is remained in the ±5-mV range.
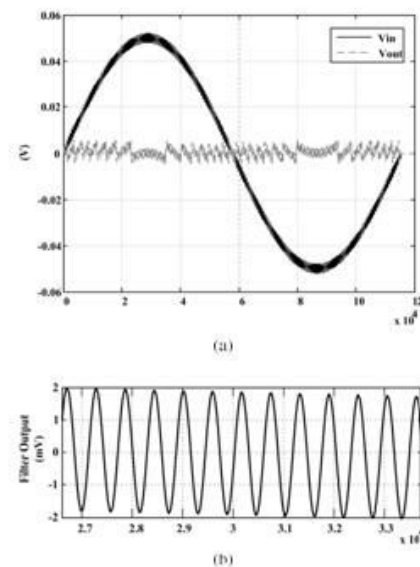

Fig. 9. (a) Input and output of the digital front end with offset cancellation. (b) Filter output.

B.Architecture

The block diagram of the proposed offset cancellation technique is shown in Fig. 10. It contains two 5-bit DCCs, control logic circuit, 5-bit counter, and 5–32 demultiplexer (Demux). Since the offset voltage changes very slowly, the frequency of the clock signal used for the counter (Clkc) is 10 times less than the clock of

the rest of the circuit. In this structure, the output delay of the VTCp block, tdp, is compared with tdmax and tdmin in the control logic block by a time comparator (TC) to determine the operation region of the VTCp(i.e., R1, R2, or R3). If the delay is more (less) than tdmax(tdmin), the DOWN (UP) signal will be set by the control logic block. The output of the counter changes accordingly and is applied to the Demux, which controls the DCC. The DCC generates a current proportional to its digital input and decreases/increases the input voltage of the VTCp and VTCn, (each LSB of the DCC corresponds to 3.125 mV and this is the voltage that is added to/subtracted from the input in each step). This process will continue until the circuit goes into the R3 region. In this case, the offset value is on the tolerable range of the circuit, (5 mV). Then, offset can be eliminated in digital domain with a simple and low-cost digital HPF with a frequency response of
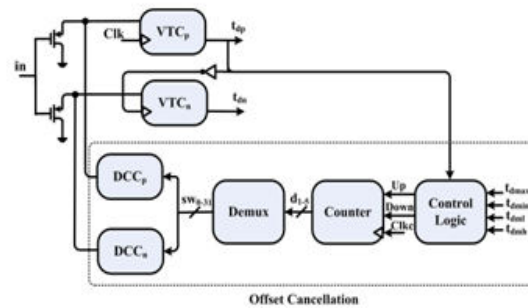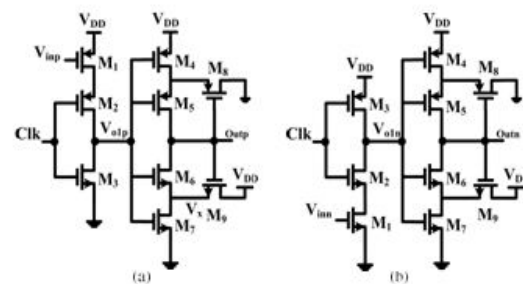

Fig. 10. Proposed offset cancellation block diagram.

Fig. 11. VTC circuit. (a) Controlled by a pMOS transistor used in VTCp blocks. (b) Controlled by a nMOS transistor used in VTCn blocks.

$$H(Z)= \frac{1}{1+ \frac{\mu_0}{1-z^{-1}}},\qquad (9)$$

The pole of this filter is $Z = 1/(1 - \mu_0)$. The distance of the pole from zero $(Z = 1)$ determines the sharpness of the filter near zero frequency. The smaller the coefficient, μ_0, the higher the quality factor of the filter and the lower the filter attenuation at nonzero frequencies. To implement this filter, only a simple accumulator and a coefficient $\mu_0 < 0$ is

Necessary, which can simply be considered as a negative power of two. Thus, this factor can be implemented only by a shift to the right. We applied the recovered output of the front end to the filter and Fig.9(b) shows the output of this filter. The above-mentioned algorithm has the advantage of can- ceiling the impact of process variations. Process variations can shift the delay to region R1. The digital feedback loop brings back the delay to region R3 and the impact of the process variations is cancelled.

IV.CIRCUITDESIGN

The proposed fully digital front end is implemented in the 0.13-um CMOS technology to evaluate its performance. The supply voltage is 0.3V, and the circuits are designed to operate in the sub threshold region to reduce the power consumption. Each block of the system and its design

challenges is discussed in the following sections.

A. V_{TC} Circuit

Fig. 11 shows the circuits of the VTCs used in VTCp And VTCn blocks (each block contains 15 stages of these Cells). It consists of a current-starved (CS) inverter and an inverting Schmitt trigger. As can be seen in this figure, the input voltages, Vinp and Vinn, control the current passing through transistor M1 and change the rise/fall delay of the CS inverter. The Schmitt trigger circuit at the output of the CS inverter issued to sharpen the rising/falling edge of the clock at

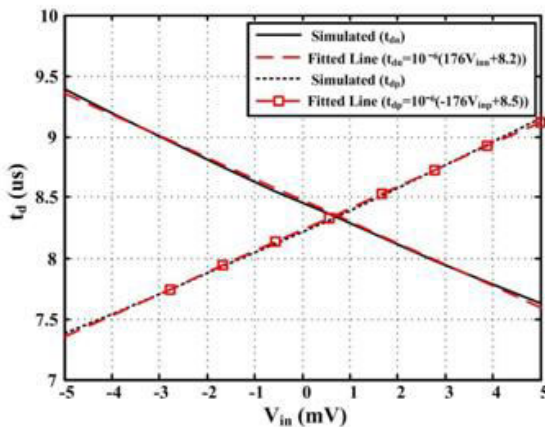

Fig. 12. Delay of the voltage to time converter from simulation and the line fitted to the simulation data, for VTCp and VTCn circuits.
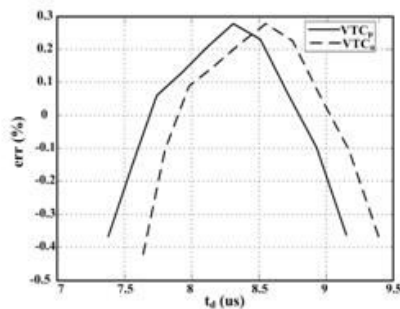

Fig. 13. Error curve for VTCp and VTCn.

the output. This helps reduce the jitter and power consumption in the succeeding stages.Fig. 12 shows the characteristic curve of the VTCn and VTCp at the typical

process corner (TT). The clock frequency in this simulation is 57.8 kHz. As can be seen, the delay Changes almost linearly with the input voltage of the VTC. The dashed line in this figure shows the line fitted to the simulation data. The two equations representing the dashed lines are as follows:

$$t_{dn} = 10^{-6}(+176 V_{inn} + 8.2) \tag{10}$$
$$t_{dp} = 10^{-6}(-176 V_{inp} + 8.5). \tag{11}$$

The error between(10) and(11) and the curves obtained from simulations are shown in Fig. 13. For the VTCp, the error is between −0.36% and +0.27% and for the VTCn the error is between −0.44% and +0.27% at TT. Table II Shows this error at different process corners. When the input voltage varies from 5 to 5 mV, the delay changes by

1.76 us, hence, VTCp and VTCn have again of 176and176us/V, respectively. The maximum power consumption at the frequency of 57.8 kHz is 78.26 nW for VTCp and 56.92 nW for VTCn.

TABLE II

ERROR BETWEEN SIMULATION AND FITTED LINE FOR VTCs AT DIFFERENT PROCESS CORNERS

Corner	Errors for VTC_p	Errors for VTC_n
FF	-0.44%-0.28%	-0.48%-0.32%
SF	-0.39%-0.3%	-0.41%-0.24%
SS	-0.38%-0.26%	-0.29%-0.19%
FS	-0.46%-0.28%	-0.37%-0.29%

B. Mathematical Modeling of the VTC

In this section, we provide an analytical delay model for the VTC circuit in sub threshold region. Referring to Fig. 11, the delay of the VTC (td) can be composed of two components, one for the CS inverter

(td1) and one for the Schmitt trigger circuit (tsch)

$$t_d = f(V_{ctrl}) + t_{sch} = t_{d1} + t_{sch}. \qquad (12)$$

For the sake of simplicity, we assume tsch is constant. The Schmitt trigger is designed to have the minimum possible delay. Hence, the assumption does not cause a noticeable error, as will become clear shortly. In order to have a better controllability, the size of transistor M2 should be much bigger than that of M1. In such an arrangement, the current is controlled by M1. In order to find a relationship between Vinp (or Vinn) and the delay of the circuit (td1), we should calculate the current passing through transistor M1. Once this current is known, one can find the output voltage. Here, the calculations will be done for the circuit of Fig. 11(a) when the clock signal changes from high to low. The drain current of M1 in the subthreshold region can be calculated from[13]

$$I_1 = I_{01} \exp \frac{V_{DD} - V_{inp} - |V_{thp}|}{nV_T} \left[1 - \exp - \frac{V_{SD1}}{V_T} \right] (13)$$

In (13), V_T is the thermal voltage and n is the subthreshold slope factor. Moreover, we ignore the term $(1 - \exp(V_{SD1}/V_T))$ (since this term is close to 1). The output voltage (V_{o1p}) can be found from

$$C_n \frac{dV_{o1p}}{dt} = I_{01} \exp \frac{V_{DD} - V_{inp} - |V_{thp}|}{nV_T} \cdot \left[1 - \exp - \frac{V_{DD} - V_{o1p}}{V_T} \right] \qquad (14)$$

where C_n represents the overall capacitance at node V_{o1p}. Solving the above differential equation with the initial condition $V_{o1p} = V_{m+}$ (V_{m+} is upper switching voltage of the Schmitt trigger) at $t = t_{d1p}$ results to

$$t_{d1p} = \frac{C V_{m+}}{I_{01} \left[\exp \frac{V_{DD} V_{inp} V_{thp}}{-nV_T} \right]} \qquad (15)$$

To compute the delay of the CS inverter, we should find Vm+. We assume node Out pis high, which turns OFF transistor M8 and series connection of M4 and M5 can be considered as a single transistor with a length of L4+ L5. The Vm+ is the input to the Schmitt trigger at which the current of M6(I6) starts to become larger than the current passing through the equivalent transistor of M4 and M5 (I j). The gate–source voltage of M6 depends on Vx, which can be calculated by setting the current of M9 equal to the current of M7. Doing so would lead to Vx= VDD/2. Now, Vm+ can be found from

$$I_{05} \exp \frac{- V_{DD} - V_{m+} - V_{thp}}{nV_T} \left[1 - \exp \frac{- V_{DD} - V_{oulp}}{V_T} \right]$$
$$= I_{06} \exp \frac{- V_{m+} - V_{DD}/2 - V_{thp}}{nV_T} \left[1 - \exp \frac{V_{oup} - V_{DD}/2}{V_T} \right] \qquad (16)$$

In (16), the last term is ignored. This leads to

$$V_{m+} = \frac{3}{4} V_{DD} + \frac{1}{2} V_{thn} - \frac{1}{2} V_{thp} + \frac{nV_T}{2} \ln \frac{I_{05}}{I_{06}}. \qquad (17)$$

Now, by substituting (17) in (15), the delay time of the CS inverter can be computed

$$t_{d1p} = \frac{C_p}{I_{01}} \frac{\frac{3}{4} V_{DD}}{- V_{DD} + V_{thp}} \cdot \frac{1}{2} V_{thn} \cdot \frac{1}{2} V_{thp} \cdot nV_T \cdot \frac{I_{05}}{I_{06}}$$
$$\cdot \exp \frac{V_{inp}}{nV_T} \qquad (18)$$

Therefore

$$t_{d1p} = k_p \exp \frac{- V_{inp}}{nV_T} \qquad (19)$$

where

$$k_p = \frac{C_p}{I_{01}} \frac{\frac{3}{4} V_{DD}}{- V_{DD} + V_{thp}} \cdot \frac{1}{2} V_{thn} \cdot \frac{1}{2} V_{thp} \cdot nV_T \cdot \frac{I_{05}}{I_{06}}$$
$$\exp \frac{- V_{DD} + V_{thp}}{nV_T}$$

Using the Maclaur inexpansion for exponential term sin(19) and ignoring the second and higher order terms (since the amplitude of the ECG signal, and

consequently the input voltage of the CS inverter, is very low), one can find the following equation forth delay of the VTC:

$$t_{dp} = k_p \left[1 + \frac{V_{imp}}{nV_T} \right]^2 + t_{sch} \qquad (20)$$

Similarly, for the circuit of Fig. 11(b)

$$t_{d1n} = k_n \exp\left(- \frac{V_{inn}}{nV_T} \right) \qquad (21)$$

where

$$k_p = \frac{C_n}{I_{01}} \left[\frac{3}{4} V_{DD} + \frac{1}{2} V_{thn} - \frac{1}{2} V_{thn} - \frac{nV_T}{2} \ln \frac{I_{05}}{I_{06}} \right]^2$$

$$\cdot \exp\left(- \frac{V_{thn}}{nV_T} \right)$$

$$t_{dn} = k_n \left[1 - \frac{V_{inn}}{nV_T} \right]^2 + t_{sch} \qquad (22)$$

These equations can be used for recovery of the signal, as explainedinSectionII-D.Fig.14plotsthecharacteristiccurve of the VTCp and VTCn. In this figure, the simulated data is compared with the analytical model as well as the fitted line. The error between the analytical model and the simulations at TT corner are shown in Fig. 15. Table III represents this error at different process corners. As can be seen, the maximum error is0.48%.
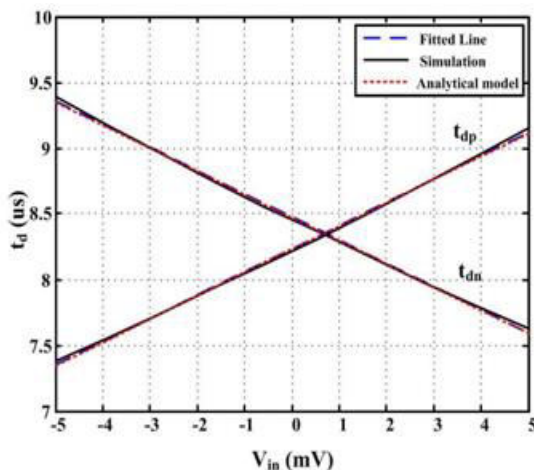

Fig. 14. Delay of the delay element from simulation and analytical model, and empirical model, for VTC$_p$ and VTC$_n$circuits.
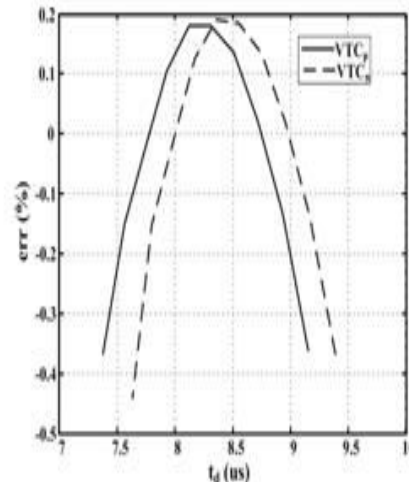

Fig. 15. Error between the simulations and the analytical model for VTC$_p$ and VTC$_n$.

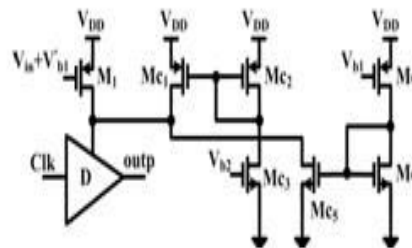
Fig. 16. Schematic of the PSRR enhancement circuit.

C.PSRR Enhancement Circuit

In order to improve the power supply rejection ratio (PSRR) of the VTCpcircuit, we have used the circuit shown in Fig. 16. Block In the VTCpcircuit, power supply noise leads to change in Vsg1. Hence, the current of M1 would vary, which leads to change the delay of the system and reduces the PSRR of the front end. To overcome this problem, we have used the PSRR enhancement circuit. In this circuit, current variations of transistor M1 due to supply noise is compensated with transistor.
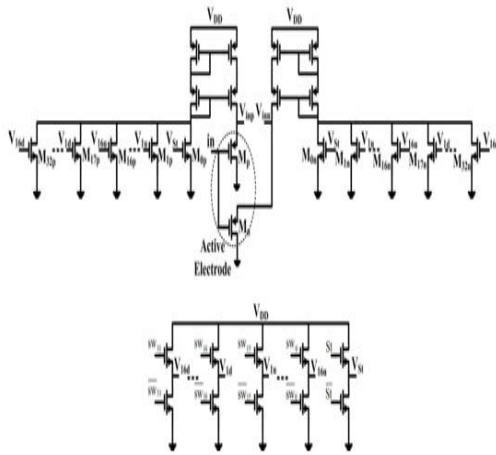
Fig. 17. Structure of the current DCCs.

D.DCCs Circuit

In the fully digital ECG front-end architecture of Fig. 3(b) two DCC blocks are used. These blocks are in charge of generating a current that depends on the 32-bit digital number (SW0 to SW31) at the output of the Demux. The DCC circuit is shown in Fig. 17, in which the lower circuit generates the gate voltages required for the reference current generator in the upper circuit. The currents produced by transistors M0pto M32pand M0n to M32npass through transistors Mpand Mnto generate the two voltages Vinp and Vinn. These voltages are then applied to the VTCp and VTCn blocks. The transistors of the DCC are sized so that Vinp and Vinn are changed in a way that the impact of the offset at the input of the active electrode as well as that of the VTC and DCC blocks are cancelled. To better understand the behavior of the DCC, assume that the offset at the input increases (decreases) leading to a rise (fall) in Vinp and Vinn. As a result, the delay of the VTCpblock increases (decreases) and that the VTCn decreases (increases). This delay variation is sensed by the TCs in the control

block and a new control bit is generated by the counter and Demux. Consequently, one of the current controlling transistors(M1pto M32pfor the DCCp and M1nto M32nfor the DCCn) are turned ON and Vinp and Vinn are reduced by 3.125 mV. This procedure is repeated until the operation of the VTC blocks goes back to region R3 in Fig.8.

E. Control Logic

The control logic diagram is shown in Fig. 18. It is composed of TCs, AND and OR gates, and set-reset (SR) latches. As explained in Section III-A, for detecting the offset, the control logic should compare tdp with four predefined delays (tdmax, tdmin, tdml, and tdmh). Note that in an analog front end, for detecting the offset voltage, an analog voltage comparator should be used. In our design, the offset is detected by TCs, which are implemented by D flip-flops and are more power and area efficient compared with the analog voltage comparators. The outputs of the control logic circuit are the UP and DOWN signals, which control the up/down counter in the offset cancellation block. The counter in our design is implemented by NAND gates and jkflip-flops.

V.SIMULATIONRESULT

The proposed architecture is implemented in 0.13-um CMOS technology. Fig. 19 shows the frequency response of the front end. The dots in this figure represent the simulation results, and the solid line shows an ideal sinc function. As can be seen, the frequency response of the front end closely resembles the sinc function with fs57.8 kHz.To show the behavior of the offset cancellation block a 1 kHz 2-mV sinusoid voltage

superimposed on a 5 Hz 50-mV sin wave is applied to the input. The input and the recovered output voltages are shown in Fig. 20. As can be seen, at point A (Vin 5.5 mV), the delay of the VTCpis 8.8641 us, which indicates the operation region of the VTC is in R1 region (refer to Fig. 8). The offset cancellation mechanism has brought back the operation region to R3. The circuit operates in region R3and moves to region R2as the offset of the input increases. When the input offset voltage reaches 11 mV, the offset cancellation circuit detects this shift and cancels the impact of the input offset(pointB).After recovery, the whole signal is present in the output digital signal and digital filtering should be done finally. In order to check the performance of the front end an ECG signal from the MIT-BIH arrhythmia database (record 101) [14] is applied to the system. Fig. 21shows the original (Vin) and the recovered signals (Vout). As can be seen, at the beginning, the offset cancellation circuit is acting and setting the output of the DCCs and after this transition.
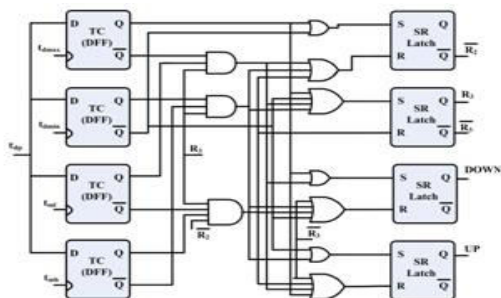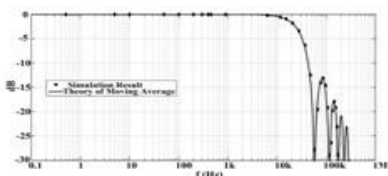

Fig. 18. Schematic of the control logic.
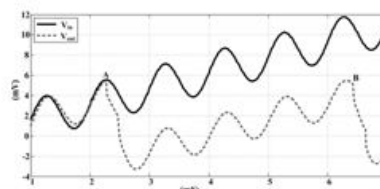

Fig. 19. MA-VTC filter result.

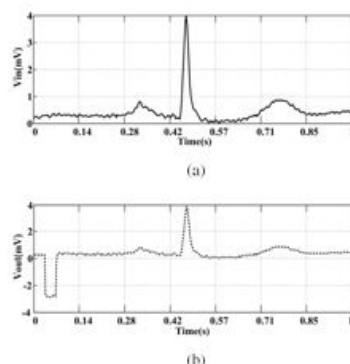Fig. 20. Input and recovered output of the front end with offsetcancellation.

(a)

(b)

Fig. 21. Record number 101 of the MIT-BIH database. (a) Original signal. (b) Recovered signal.

TABLE IV

SUMMARY OF SIMULATED SYSTEM CHARACTERISTICS

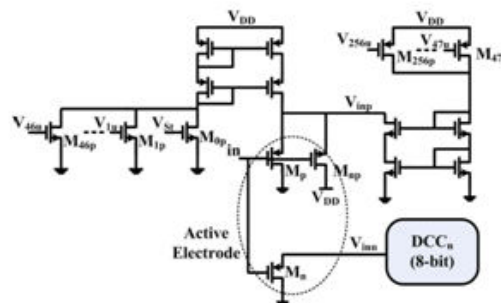| Parameter	Values
Technology	0.13µm
Supply voltage	0.3V
Power consumption	0.18pW

Fig. 22. Jitter noise power spectral density.

Fig. 23. Modified structure of DCC p.

Time the output signal is reliable. The overall performance parameters of the front end are shown in Table IV. The VTC gain is defined as the ratio delay variation at the output of the VTC blocks and the input voltage range. In order to explore the noise performance of the front end, the jitter is

obtained at the output of the front end. The noise power spectral density is shown in Fig. 22 and a jitter noise of 5 ns and SNR of 42 dB are obtained. Depending upon the required resolution this amount of noise may be large. Since there is a tradeoff between power and noise, in order to reduce the noise more power should be burnt. Using the proposed PSRR enhancement circuit in this paper leads to the PSRR of 67.7 dB. The power consumption of the overall front end is 18.4pW and is noticeably less than other mixed-signal ECG front-end circuits. This can be considered as one of the main advantages of the proposed fully digital architecture.

VI.CONCLUSION

In the expectation of the future dominance of digital CMOS technology, we have implemented a fully digital front-end architecture for an ECG acquisition system. In this system, passive elements, LNA, and analog filters are not used. The proposed digital architecture is compact and power efficient compared with the other analog implementations of these systems. A new offset cancellation technique is used, which reduces the 50-mV offset voltage to <5 mV and makes it tolerable for the system. A moving average mechanism embedded into the VTC of the front end eliminates the need for anti aliasing filter. The proposed architecture is simulated in0.13-um CMOS technology at 0.3 V supply voltage. The simulated power consumption is 18.4pW.

REFERENCES

[1]X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," IEEE J. Solid-State Circuits, vol. 44, no. 4, pp. 1067–1077, Apr.2009.

[2] R.R.HarrisonandC.Charles,"A low-powerlow-noiseCMOSamplifier for neural recording applications," IEEE J. Solid-State Circuits, vol. 38, no.6,pp.958–965,Jun.2003.

[3] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad,and

A. M. Sodagar, "Analysis and design of tunable amplifiers for implantable neural recording applications," IEEE J. Emerg. Sel. Topics Circuits Syst, vol. 1, no. 4, pp. 546–556, Dec.2011.

[4] M. S. J. Steyaert and W. M. C. Sansen, "A micro power low-noise monolithic instrumentation amplifier for medical purposes,"IEEE

J. Solid-State Circuits, vol. 22, no. 6, pp. 1163–1168, Dec. 1987.

[5] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micro power neural recording amplifier," IEEE Trans. Biomed. Circuits Syst.,vol.1,no.2,pp.136–147,Jun.2007.

[6]T.Denison,K.Con√soer,A.Kelly,A.Hache nburg,andW.Santa,

[7]Q.Fan,√F.Sebastiano,J.H.Huijsing,andK. A.A.Makinwa,"A1.8µW 65 nm CMOS for wireless sensor nodes," IEEE J. Solid-State Circuits, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.

[8] P. K. Chan and J. Cui, "Design of chopper-stabilized amplifiers with reduced offset for sensor applications," IEEE Sensors J., vol. 8, no. 12, pp. 1968–1980, Dec.2008.

[9] J. L. Bohorquez, M. Yip, A. P. Chandrakasan, and J. L. Dawson, "A bio medical sensor interface with a sinc filter

and interference cancellation," IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 746–756, Apr.2011.

[10]   R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm2, 5 µW, DC-coupled neural signal acquisition IC with 0.5 V supply," IEEE J. Solid-State Circuits, vol. 47, no. 1, pp. 232–243, Jan.2012.

[11]   M. Fernandez and R. Pallas-Areny, "A simple active electrode for power line interference reduction in high resolution bio potential mea- surements," in Proc. 18th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc., Bridging Disciplines Biomed., vol. 1. Oct./Nov. 1996, pp.97–98.

[12]G.Li,Y.M.Tousi,A.Hassibi,andE.Afshari ,"Delay-line-basedanalog-   to-digital converters," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no.6,pp.464–468,Jun.2009.

[13]   Y. Tsividis, K. Suyama, and K. Vavelidis, "Simple 'reconciliation' MOSFET model valid in all regions," Electron. Lett., vol. 31, no. 6, pp. 506–508, Mar.1995.

[14]   MIT-BIH Arrhythmia Database. [Online].   Available: http://www.physionet.org/physiobank/datab ase/mitdb/,   accessed Jun.2011.