INTERNATIONAL JOURNAL · ENGINEERING RESEARCH ·

International Journal for Innovative Engineering and Management Research

A Peer Revieved Open Access International Journal

www.ijiemr.org

COPY RIGHT

IJIEMR Transactions, online available on 23rd February 2018. Link :

http://www.ijiemr.org/downloads.php?vol=Volume-7&issue=ISSUE-2

Title: Cost Effective Approach For Multi Level Filter Design For Reconstruction Of Stable And Dynamic Applications.

Volume 07, Issue 02, Page No: 611 - 617

Paper Authors

***BOLISETTI VEERABABU, R.VINAY KUMAR.**

* Dept of ECE, Kakinada Institute of Engineering & Technology.

International Journal for Innovative Engineering and Management Research ★

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

International Journal for Innovative Engineering and Management Research

A Peer Revieved Open Access International Journal

www.ijiemr.org

COST EFFECTIVE APPROACH FOR MULTI LEVEL FILTER DESIGN FOR RECONSTRUCTION OF STABLE AND DYNAMIC APPLICATIONS

***BOLISETTI VEERABABU, **R.VINAY KUMAR**

*PG Scholar, Vlsd, Dept of ECE, Kakinada Institute of Engineering & Technology, Korangi, A.P.

**Associate Professor, Dept of ECE, Kakinada Institute of Engineering & Technology, Korangi, A.P.

ABSTRACT

Transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct-form configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. We have derived a general multiplier-based architecture for the proposed transpose form block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less area-delay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involves 42% less ADP and 40% less EPS than the best available FIR filter structure proposed for reconfigurable applications. For the same filter length and the same block size, the proposed structure involves 13% less ADP and 12.8% less EPS than that of the existing direct-form block FIR structure.

1. INTRODUCTION

A filter is a device or process that removes some unwanted component or feature from a signal. Filtering is a class of signal processing, the defining feature of filter being the complete or partial suppression of some aspect of the signal. There are two main kinds of filter, analog and digital. Filters can be classified in several different groups, depending on what criteria are used for classification. The two major types of digital filters are finite impulse response digital filters (FIR filters) and infinite impulse response digital filters (IIR).

FIR filters are one of the primary types of filters used in Digital Signal Processing. FIR filters are said to be finite because they do not have any feedback. Therefore, if we send an impulse through the system (a single spike) then the output will invariably become zero as soon as the impulse runs through the filter. A non-recursive filter has no feedback. The Finite Impulse Response Filter Realization is as shown in figure 1.

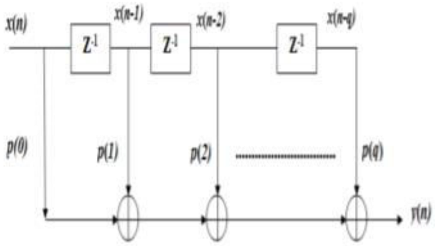

FIGURE: FIR FILTER REALIZATION

2. RELATED WORKS

Pramod Kumar Meher (2006) proposed the structure that involves significantly less memory and less areadelay complexity compared with the existing DA-based structures for circular convolution. Besides, it is shown that the proposed systolic designs for circular convolution can be used for computation of linear convolution as well. Basant Kumar Mohanty and Pramod Kumar Meher (2015) explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications.

Yu Pan and Pramod Kumar Meher(2014)proposed the resource minimization problem in the scheduling of adder-tree operations for the MCM block, and presented a mixed integer programming (MIP) based algorithm for more efficient MCM-based implementation of FIR filters. Experimental result shows that up to 15% reduction of area and 11.6% reduction of power (with an average of 8.46% and 5.96% respectively) can be achieved on the top of already optimized adder/subtractor network of the MCM block.

Abbes Amira, Pramod Kumar MeherandShrutisagarChandrasekaran (2008) presented the design optimization of one and two dimensional fully pipelined computing structures for efficient implementation of finiteimpulse-response (FIR) filter to obtain effective area, delay and power by using systolic decomposition of innerproduct computation based on distributed arithmetic(DA). The systolic decomposition scheme is found to offer a flexible choice of the address length of the lookup tables (LUT) for DA-based computation to decide on suitable area time trade off. It is observed that by using smaller address lengths for DA-based computing units, it is possible to reduce the memory size, but on the other hand that leads to increase of adder complexity and the latency.

3. EXISTING METHODS

In the existing method, Basant Kumar Mohanty and Pramod Kumar Meher explore the possibility of realization of FIR filter in transpose form configuration for efficient area and delay realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, they have derived a flow graph for transpose form block FIR filter with optimized register complexity.

A generalized block formulation is presented for transpose form FIR filter. They have derived a general multiplier based architecture for the proposed transpose form block filter for reconfigurable applications. In the existing method, the implementation of direct-form structure has less area delay product (ADP) and less energy per sample (EPS) for the short-length filters. But for medium or large length filters, it has high ADP and high EPS. In the FIR filter structure, the ripple carry adders are used to add the partial inner products.

The well known adder architecture, Ripple Carry Adder is composed of cascaded full adders for n-bit adder. It is constructed by cascading full adder blocks in series. The carry out of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder it requires n full adders.

a) Not very efficient when large number bit numbers are used.

b) Delay increases linearly with bit length. The ripple carry adder provides efficient area utilization but its operating speed is slow. This is the main drawback of the existing method.

4. PROPOSED WORK

In the proposed method, the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications is explored. The proposed structure will have significantly less area delay product (ADP) and less energy per sample (EPS) for medium or large filter lengths than the existing block implementation of direct-form structure. In the proposed method, the realization of block FIR filter in transpose form configuration in order to take advantage of the MCM scheme is explored and the inherent pipelining for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications.

The main contributions of this paper are as follows.

1) Computational analysis of transpose form configuration of FIR filter and derivation of flow graph for transpose form block FIR filter with reduced register complexity.

2) Block formulation for transpose form FIR filter.

3) Design of transpose form block filter for reconfigurable applications.

4) A low-complexity design method using MCM scheme for the block implementation of fixed FIR filters.

4.1 MULTIPLE CONSTANT MULTIPLICATION (MCM)

In any FIR filter, the multiplier is the major constraint which defines the performance of the desired filter. Therefore, over the past three decades, design of an efficient hardware architecture for fixed point FIR filter has been considered as the major research focus as reported in published literatures.

In FIR filter, the multiplication operation is performed between one particular variable (the input) and many constants (the coefficients) and known as the multiple constant multiplication (MCM). The algorithms proposed to implement the MCM for an efficient FIR filter design can be categorized in two main groups: 1) graph based algorithms and 2) common sub-expression elimination

(CSE) algorithms. Most of these graph based or CSE algorithms presented earlier are used to obtain efficient FIR filter hardware architecture by running the algorithms on a particular (fixed) set of coefficients for some time (a couple of hours to days) on a highly efficient computing platform (like using 1–20 number of 3.2 GHz computers in parallel mode. However, FIR filter implementation employing effective MCM design by running these algorithms on a fixed set of coefficients is not suitable for the application like SDR system because of the following two reasons: 1) coefficient of the filters in SDR system are dynamically programmable based on requirement of different standards and 2) highly computationally efficient platform needed for those algorithms is unaffordable in SDR system. Multiple constant multiplication (MCM) scheme is widely used for implementing transposed direct-form FIR filters. While the research focus of MCM has been on more effective common sub expression elimination, the optimization of adder-trees, which sum up the computed sub-expressions for each coefficient, is largely omitted.

4.2 PROPOSED STRUCTURES

There are several applications where the coefficients of FIR filters remain fixed, while in some other applications, like SDR channelizer that requires separate FIR filters of different specifications to extract one of the desired narrowband channels from the wideband RF front end. These FIR filters need to be implemented in a RFIR structure to support multi standard wireless communication.

4.3 IMPLEMENTATION OF FIXED-COEFFICIENT FIR FILTER USING MCM BLOCKS

The proposed structure for FIR filters using MCM-based is shown in fig.2. The MCM-based structure involves six MCM blocks corresponding to six input samples.

The Register Unit involves (L − 1) registers of B-bit width. The Pipelined Adder Unit involves L(M−1) adders and the same number of registers, where each register has a width of (B+ B'), B, and B' respectively, being the bit width of input sample and filter coefficients. Therefore, the proposed structure involves LN multipliers, L(N − 1) adders, and [B(N − 1) + B'(N − L)] flip flops and L samples are processed in every cycle where the duration of cycle period T = [TM + TA + TFA(log2 L)]

4.4 IMPLEMENTATION IN VERILOG:

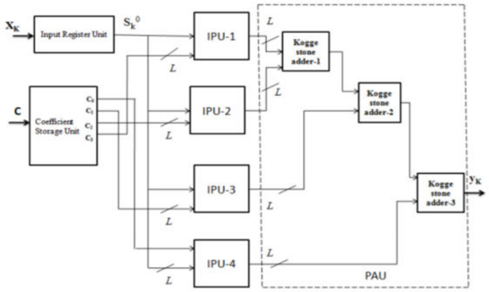

Fig.3. Block FIR filter for reconfigurable applications.

The Coefficient Storage Unit (CSU) is used to store the coefficients of all the filters. These coefficients are used in the reconfigurable applications. It has N Read Only Memory (ROM) Lookup Tables (LUTs) where N is the length of the filter (N=ML). The Register Unit

(RU) is used for storing the input samples is shown in Fig.2. It contains (L-1) registers. During the K th cycle, the register unit accepts input sample XK and computes L rows of SK 0 in parallel. The outputs from the RU are given as inputs to M Inner Product Units.

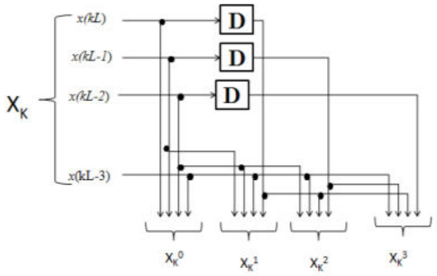

Fig.4. Internal structure of Register Unit (RU) for block size L=4

The Inner Product Unit (IPU) is used to perform a multiplication operation of SK 0 with the small weight vector cm is shown in Fig.3. The M Inner Products Units accepts L rows of SK 0 from the RU and M small weight vectors from the CSU. Each Inner Product Unit contains L number of Inner Product Cells (IPCs) which performs L inner product computations of L rows of SK 0 with coefficient vector cm and produces a block of L number of partial inner products. All the four IPUs work simultaneously and M blocks of a result are obtained.

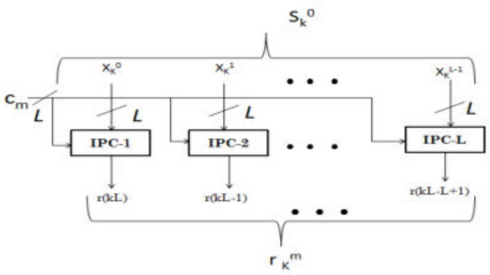

Fig.5. Internal structure of (m+1)th IPU.

The internal structure of (l +1) th IPC is shown in Fig.4. The Inner Product Cell (IPC) accepts (l+1)th row of Sk 0 and small weight vector cm and produce a partial result of inner product r(kL −l), for $0 \le l \le L - 1$. Each IPC consists of L multipliers and (L-1) number of adders.

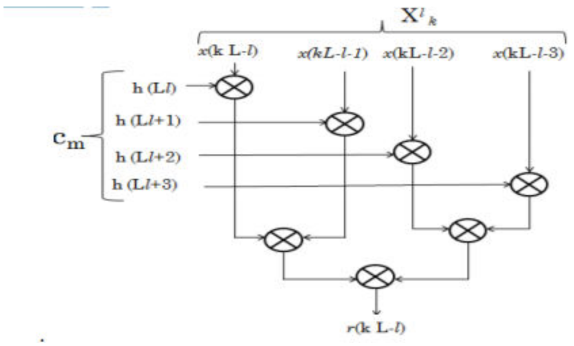

Fig.6. Internal structure of (l + 1)th IPC.

The Pipelined Adder Unit (PAU) receives partial products from all the M IPUs. Array of Kogge Stone Adder is used in PAU to add all the partial products is shown in Fig.5. KSA is one of the Carry Tree Adders or Parallel Prefix Adders. Kogge Stone Adders gains more importance among all the adders because of its high performance.

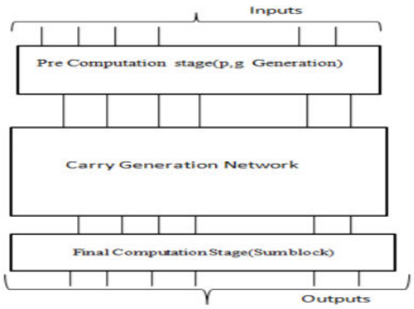
Inputs
Pre Computation stage(p,g Generation)
Carry Generation Network
Final Computation Stage(Sum block)
Outputs

Fig.7. Different Stages in Kogge Stone Adder

KSA can be implemented in 3 stages, namely Pre-Computation Stage, Carry generation network and final computation stage. Generate and Propagate signals are computed in Pre-Computation Stage, corresponding to each pair of input bits A and B. The second stage compute carries corresponding to each bit. Execution of these operations is performed in parallel form, and they are partitioned into smaller pieces. Group generate and propagate bits which are computed in the first stage are used as intermediate signals in carry generation network. The final computation stage is common for all the adders of this family which gives the summation of input bits.

5. SIMULATION RESULTS

The comparision table for existing method and proposed method with respect to the delay, number of slices, number of LUTs, number of IOs, number of bonded IOs and power consumption is shown below. Table 1: Comparison of delay, number of slices, number of LUTs, number of IOs, number of bonded IOs and power consumption of existing method and proposed method.

Conclusion In this paper, the possibility of realization of block FIR filters in transpose form configuration for area and delay efficient realization of fixed FIR applications were explored and also the impact of power consumption, delay, area has been analyzed. Simulation results have been calculated. The use of ripple carry adders in existing method increases area and power consumption. To overcome this drawback, carry look ahead adder is used in the proposed method. The proposed structure has the best results in the reduction of number of slices, LUTs, power consumption, area delay product, energy per sample than the existing method for higher order FIR filter.

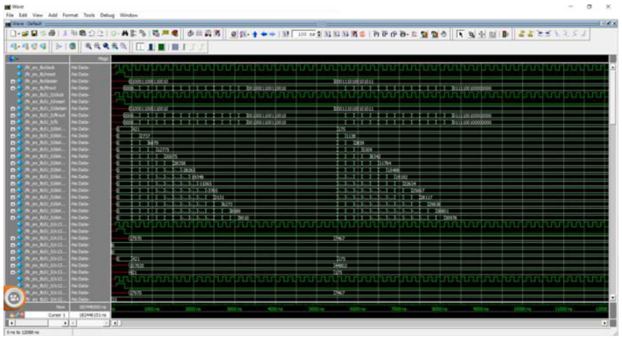

FIGURE: Representing The FIR FILTER RECONFIGURABLE DESIGN

REFERENCES

[1] Basant Kumar Mohanty, and Pramod Kumar Meher (2015,) 'A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications', IEEE Transactions on VLSI System.

[2] Mahesh R. and Vinod A. P. (2010), 'New reconfigurable architectures for implementing FIR filters with low complexity', IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 29, no. 2, pp. 275–288.

[3] Meher P.K. (2010), 'New approach to look-up-table design and memory based realization of FIR digital filter', IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 3, pp. 592–603.

[4] Mohanty B. K. and Meher P. K. (2013), 'A high-performance energy-efficient architecture for FIR adaptive filter based on new distributed arithmetic formulation of block LMS algorithm,' IEEE Trans. Signal Process., vol. 61, no. 4, pp. 921–932.

[5] Park S.Y. and Meher P.K. (2014) , ‘Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter’, IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 7, pp. 511–515.

[6] Pramod Kumar Meher, ShrutisagarChandrasekaran and Abbes Amira (2008), ‘FPGA Realization of FIR Filters by Efficient and Flexible Systolization Using Distributed Arithmetic’,IEEE Transactions On Signal Processing, Vol. 56, No. 7.

[7] Pramod Kumar Meher (2006), ‘Hardware-Efficient Systolization of DA-Based Calculation of Finite Digital Convolution’, IEEE Transactions On Circuits And Systems-II: Express Briefs, Vol. 53, No. 8.

[8] Vinod A. P. and Lai E. M. (2006), ‘Low power and high-speed implementation of FIR filters for software defined radio receivers’, IEEE Trans. Wireless Commun., vol. 7, no. 5, pp. 1669–1675.