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# LOW POWER AND REUSABLE FM0/MANCHESTER ENCODER FOR DSRCS APPLICATIONS.

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## ABSTRACT:

The main objective of this project is to design a low power and reusable FM0, Manchester encoder for DSRCS applications. Fully reused VLSI architecture using (similarity-oriented logic simplification) SOLS technique for both FM0 and Manchester encodings is proposed. Dedicated short-range communications are one-way or two-way short-range to medium-range wireless communication channels specifically designed for automotive use and a corresponding set of protocols and standards. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. Further, this project is enhanced by using clock gating technique; we are going to reduce the power in memory organization. Power supply will be provided to corresponding accessed rows only.

**KEYWORDS**: SOLS (similarity-oriented logic simplification), FM0, Manchester, DSRCS (Dedicated Short range Communications).

## I. INTRODUCTION

FM0 and Manchester coding techniques are used to encode the data while transmit the signal through medium. Using similarities in the FM0 and Manchester coding, we developed the reused VLSI hardware architecture. Since, encoding plays the vital role in secured communication. Developing architecture for such encoding techniques is need of the hour. One sort of renowned and commonly used communication technique is DSRC (Dedicated Short Range Communication) which is designed support the variety of applications (Figure 1). Based on vehicular environments communication. DSRC, the subset of RFID (Radio Frequency Identification) for tracking and identification. DSRC standards adopts both FM0 and Manchester encoding for signal reliability and dc balance.

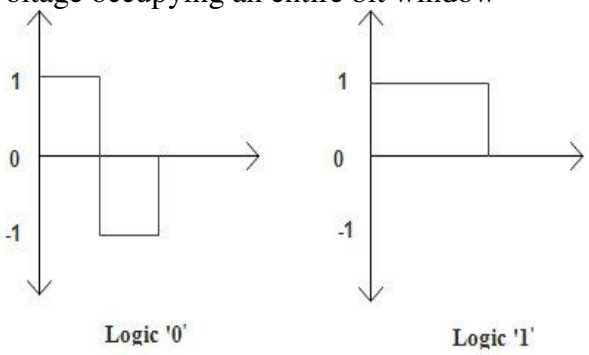
## Coding Principles Of Fm0, Manchester:

The coding principles of FM0 and Manchester encoder are discussed as follows,

*A. FM0 encoding*

FM0 encoding is also called as bi-phase space encoding scheme. In FM0 encoding, the signal to be transmitted and done according , to the following rules, It inverts the phase of the base band signal at the boundary of each symbol.

- For representing logic ‘0’ level, it inverts the signal at the mid of the symbol.
- For representing logic ‘1’ level, it constant voltage occupying an entire bit window




## THE STATE CODE PRINCIPLE FOR FM0/MANCHESTER

The Manchester encoding is an XOR operation only. The FM0 code starts with the FSM principle. The FSM of FM0 code classified into

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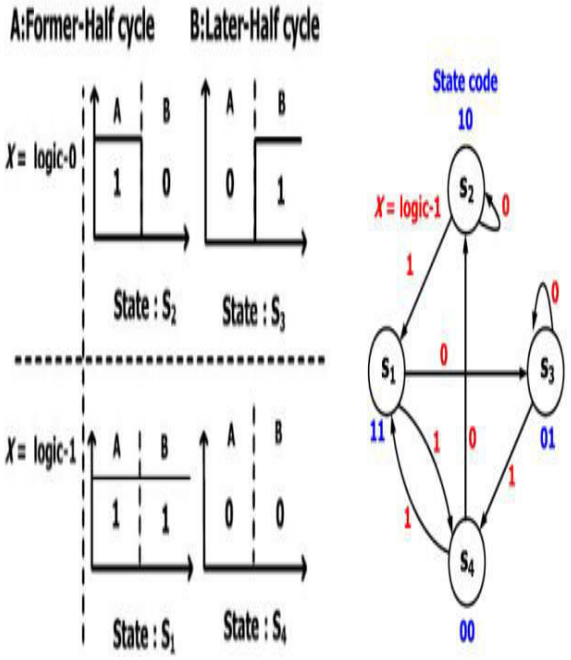
four states. The four states as shown in the below figure.




FSM of FM0 uppose the initial state is S1, and its state code is 11 for A and B, respectively.

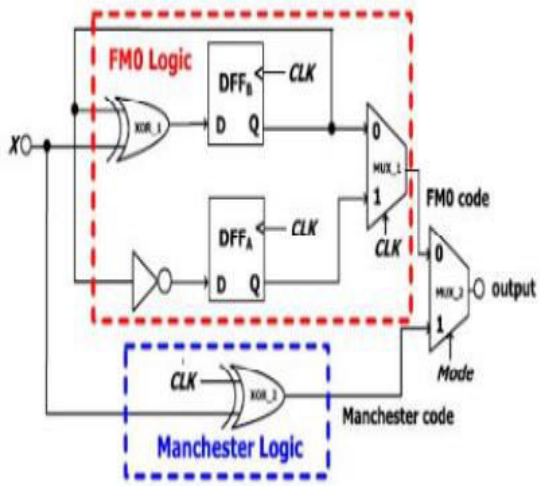
1) If the X is logic-0, the state-transition must follow both rules for FM01 and 3. The only one next-state that can satisfy both rules for the X of logic-0 is S3. If the X is logic-1, the state-transition must follow both rules for FM0 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also conduct the transition table of each state A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1)and the B(t − 1), respectively. With this transition table, the Boolean functions of A(t) and B(t) are given as

2) $A(t) = B(t-1)\ B(t) = X \oplus B(t-1)$

With both A(t) and B(t), the Boolean function of FM0 code is denoted as CLK A(t) +~ CLK B(t)

| Previous state | | Current state | | | |
|---|---|---|---|---|---|
| A(t-1) | B(t-1) | A(t) | | B(t) | |
| | | X=0 | X=1 | X=0 | X=1 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 |

## HARDWARE ARCHITECTURE OF FM0/MANCHESTER CODE:




This is the hardware architecture of the fm0/Manchester code. the top part is denoted the fm0 code and then the bottom part is denoted as the Manchester code. in fm0 code the DFFA and DFFB are used to store the state code of the fm0 code and also mux_1 and not gate is used in the fm0 code. When the mode=0 is for the fm0 code. the Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code.

## II. EXISTING SYSTEM

**FMO AND MANCHESTER ENCODER USING SOLS TECHNIQUE:** The SOLS technique is classified into two parts area

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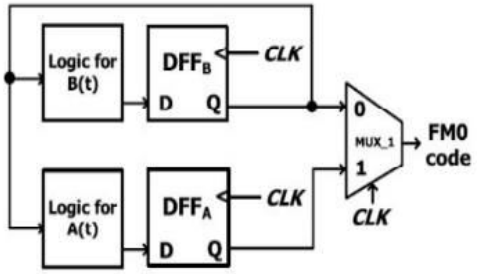
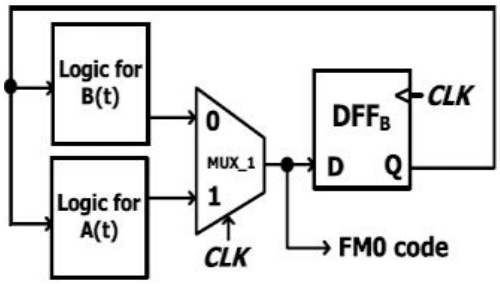
compact retiming and balance logic operation sharing

### A. area compact retiming

For fm0 the state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1).

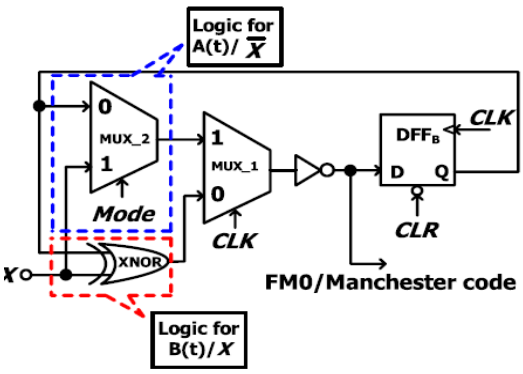



Area compact retiming




FM0 encoding without area compact retiming

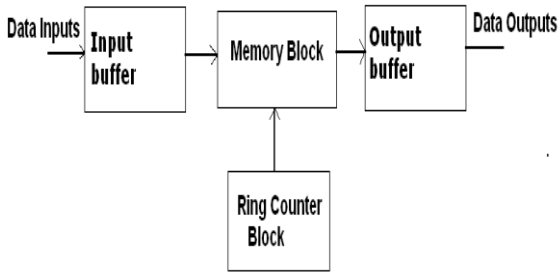
The previous state is denoted as the A(t-1) and then the B(t-1).and then the current state is denoted as the A(t) and then the B(t)




Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The transistor count of the FM0 encoding architecture without area-compact retiming is 72,and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

## III.PROPOSED SYSTEM

### Memory Organization:




### input buffer:

The Input buffer is also commonly known as the input area or input block. When referring to computer memory, the input buffer is a location that holds all incoming information before it continues to the CPU for processing. Input buffer can be also used to describe various other hardware or software buffers used to store information before it is processed.

### memory block:

(RAM) Random-access memory (RAM) is a form of computer data storage. Today, it takes the form of integrated circuits that allow stored data to be accessed in any order (that is, at random). "Random" refers to the idea that any piece of data can be returned in a constant time, regardless of its physical location and whether it is related to the previous piece of data

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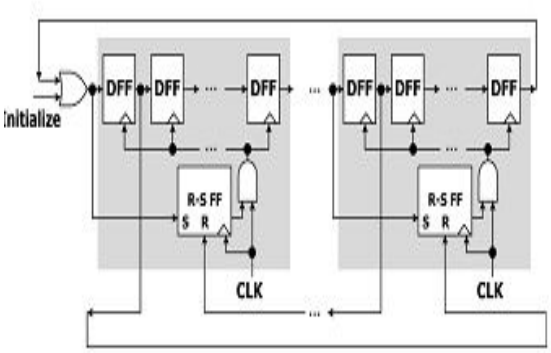
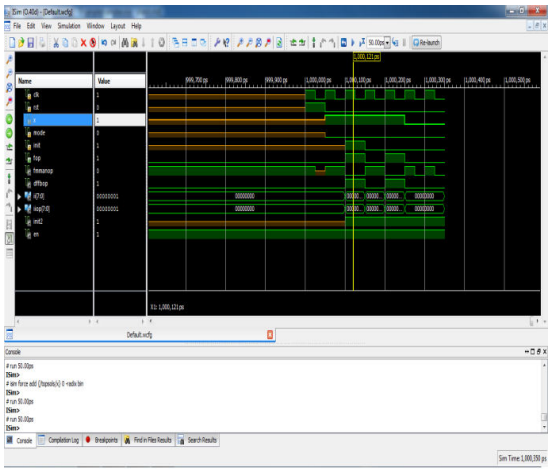
**ring counter:** A **ring counter** is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register.

There are two types of ring counters: *traight ring counter* or *Overbeck counter* connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. For example, in a 4-register one-hot counter, with initial register values of 1000, the repeating pattern is: 1000, 0100, 0010, 0001, 1000... . Note that one of the registers must be pre-loaded with a 1 (or 0) in order to operate properly.




The above block diagram shows the power controlled Ring counter.First, total block is devided into two blocks. Each block is having one SR FLIPFLOP controller

## IV. RESULTS



| | POWER (mw) |
|---|---|
| EXISTING | 445 |
| ENHANCED | 375 |

## V. CONCLUSION

Using similarities in the FM0 encoding and Manchester encoding techniques, hardware architecture is to be developed. Manchester and FM0 coding are very popular codes, as these codes are level insensitive, self-clocking and they provide signal absence detection and having the encoding clock rate embedded within the transmitted data. They encode the data as 1's and 0's. FM0 and Manchester encoding architectures combined together to form efficient compact architecture through SOLS (Similarity Orientation Logic Simplification) Technique. The SOLS technique is done on hardware utilization by means of two core techniques. They are namely area compact retiming and balance logic operation sharing (BLOS). FM0 codes and Manchester coding equations are combined in balance logic operation sharing along with clock gating technique. This deduced architecture of FM0 and Manchester coding would well support the DSRC standards.

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## Biographiies:

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