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Paper Authors

***P DIVYA SREE, P SIVA KRISHNA.**

* Dept of E.C.E, Pace Institute of Technology and Sciences

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DESIGN OF MODIFIED 16-BIT PARALLEL PREFIX KOGGE STONE ADDER

***P DIVYA SREE, **P SIVA KRISHNA**
*PG Scholar, Dept of E.C.E, Pace Institute of Technology and Sciences, Ongole
**Assistant Professor, Dept of E.C.E, Pace Institute of Technology and Sciences, Ongole

ABSTRACT: A carry skip adder (CSKA) structure is presented which has lower power consumption with a higher speed. The performance of the conventional CSKA is improved by achieving the speed enhancement by applying concatenation and incrementation schemes. The existed structure utilizes AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) compound gates for the skip logic. Low power very large scale integration (VLSI) circuits are most significant for designing of high performance and portable devices. The high speed, small area and low cost are the main considerations of VLSI circuits. This paper presents the design and hardware implementation of 32-bit Kogge-Stone parallel prefix adder. The proposed design is simulated using ISE simulator. The design shows 38% improvement in speed and 11.53% improvement in area compared to carry look ahead adder. The maximum power consumption for Kogge-Stone adder is 0.014W.

Keywords— Serial Adder, Parallel Prefix Adder, Kogge Stone Adder, High speed VLSI.

I.INTRODUCTION

VLSI Integer adders are applicable in Arithmetic and Logic units (ALU‟s), microprocessors and memory addressing units. Speed of the adder often decides the minimum clock cycle time. Parallel Prefix adder is utilized for its speed when compared with ripple carry adder. Parallel Prefix adders have been established as the most efficient circuits for binary addition. The regular structure and fast performance of parallel prefix adder makes particularly attractive for VLSI implementation. The classical parallel prefix adder structures presented in the literature over the years optimize for logic depth, area, and fan-out and interconnect count of logic circuits. Parallel Prefix adders (PPA) are family of adders derived from the commonly known carry look ahead adders. The parallel prefix adders are KS adder (kogge-stone), SKS adder (sparse kogge-stone), Spanning tree and Brent Kung adder. These adders are flexible and used to speed up the binary additions. RCA is a serial adder. RCA is used to perform any number of additions.

RCA is serial adder and it has propagation delay problem. When bits are increasing then delay also increases simultaneously. Hence parallel adders (parallel prefix adders) are preferred in proposed system. RCA is replaced by Kogge Stone Adder (KSA) for increasing the speed with reduced area. The advantage of utilizing the flexibility in implementing the three structures based upon throughput requirements. Due to continuing integrating intensity and the growing needs of portable devices, low-power and high-performance designs are of prime importance.

II. PARALLEL PREFIX ADDER

The Parallel Prefix adders involve the execution of an operation in parallel. This is

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done by segmentation the operation in smaller pieces which are computed in parallel. The output is depends on the initial inputs. Parallel Prefix Adder (PPA) is equivalent to carry look ahead adder (CLA). A Carry look ahead adder is a type of adder used in digital logic. CLA is designed to overcome the latency introduced by repelling effect of carry bits in RCA. A CLA improves speed by reducing carry bits. It calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of larger bit value.

CLA uses the concept of generating (G) and propagating (P) carries. The two differ in the way their carry generation block is implemented. The main advantage of PPA is the carry reduces the number of logic levels by essentially generating the carries in parallel. PPA fastest adder with focus on design time and is the choice for high performance adder in industry. In this paper, design and implementation of optimized 32 bit KSA is proposed.

III.EXISTED SYSTEM

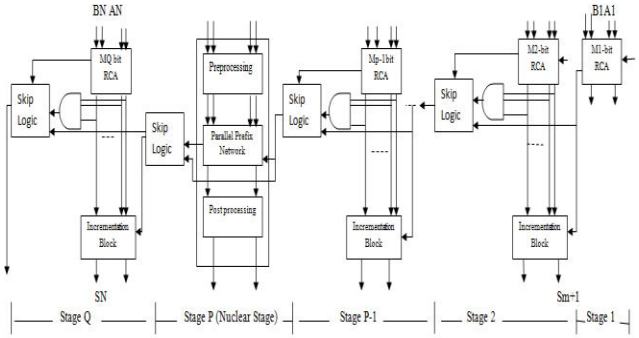

Fig. 1 Structure Of The Existed Hybrid Variable Latency Cska

The existed structure is based on combination of the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, it is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the existed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

IV.PROPOSED SYSTEM

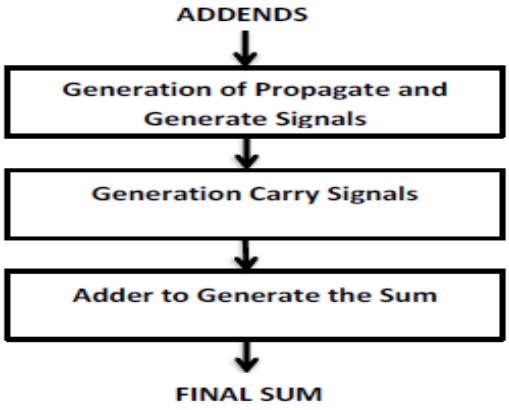

Fig. 2. Architecture Of Kogge Stone Adder (Ksa)

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Fig.2. shows the architecture of Parallel prefix adder. Kogge Stone Adder (KSA) is a parallel Prefix Adder. It is considered as fastest and is widely used in industry for high performance arithmetic circuits. KSA employs the 3-stage structure of the CLA adder. In KSA carries are computed fast by computing the carries in parallel. The carry computation method leads to speed up the overall operation significantly. This reduces the area and increase the speed. As shown in Fig. 2, the construction of KSA involves three processing stage.

A. Pre-processing stage:

This step involves computation of generate and propagate signals corresponding to each pair of bits in A and B. These signals are given by the logic equations below:

$$pi = Ai\ XOR\ Bi \qquad (1)$$

$$gi = Ai\ AND\ Bi \qquad (2)$$

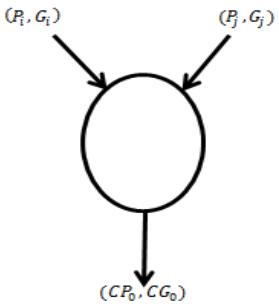

Fig. 3. Carry Generation Stage

B. Carry generating network:

Fig.3. Show the block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equations below:

$$CP0 = Pi\ AND\ Pj \qquad (3)$$

$$CG0 = Gi\ OR\ Pi\ AND\ Gj \qquad (4)$$

C. Post Processing Stage:

This step is final step and is common to all adders of this family. It involves computations of sum bits. Sum bits are computed by the logic given below:

$$Si = Pi\ XOR\ Ci{-}1 \qquad (5)$$

V. IMPLEMENTATION OF KSA

The Kogge Stone tree structure for 32 bit is shown in Fig. 4. The height of an adder is given by $log2$(n) logic stages. Hence for 16 bit adder, the height is 4 logic stages. Similarly for 32 bit, the height is 5 logic stages. The radix of the adder refers to how many results of previous logic stages are considered to generate next stage. In this design, Radix 2 is considered. Higher the radix the number of logical stages reduces. The sparsity of this design is "1". This refers to the number of carry bits generated by the carry-tree. KSA has regular layout, minimum fan-out or minimum logic depth. The delay of KSA is equal to $log2$(n). Each block performs carry generate and propagate logic as shown in Fig. 3. KSA has an area of (n*$log2$(n))-n+1 where n is the number of input bits.

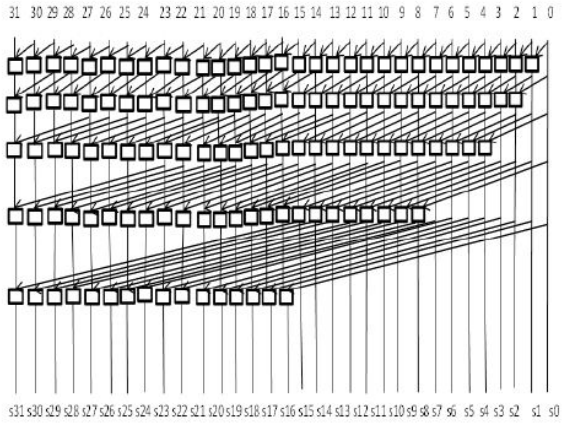

Fig. 4. Architecture Of 32 Bit Kogge Stone Adder

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VI.RESULTS

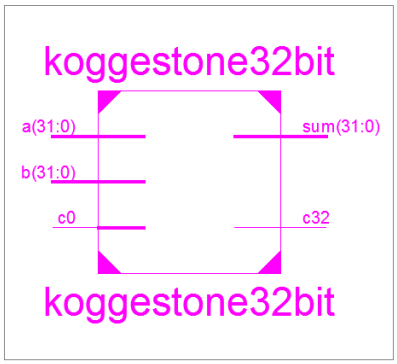

FIG. 5. RTL SCHEMATIC

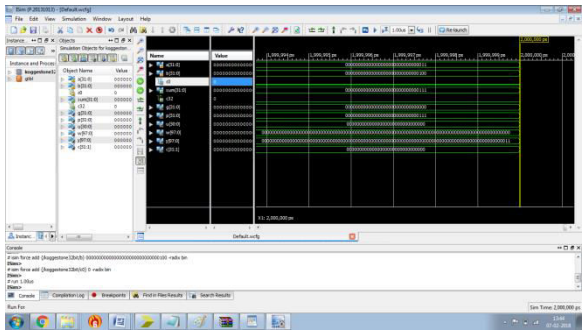

FIG. 6. OUTPUT WAVEFORM

VII.CONCLUSION

Prefix adders have been one of the most notable among several designs proposed in the past. The advantage of utilizing the flexibility in implementing the three structures based upon throughput requirements. PPA fastest adder with focus on design time and is the choice for high performance adder in industry. In this paper design and implementation of 32 KS adder is presented. For a 32 bit KSA, the design shows 11.53 percentage improvement in area and 38 percentage improvement in speed when compared to CLA adder. The power consumption for Kogge stone adder is 0.014W. The result shown that the proposed adder, parallel prefix adder is faster and requires less area then carry look ahead adder.

VIII.REFERENCES

1. V.Krishna Kumari, Y. Sri Chakrapani,"Designing and Characterization of Kogge stone, Spanning tree and Brent kung Adders".
2. Ms.Madhu Thakur, Prof. Javed Ashraf, "Design of Braun multiplier with Kogge Stone Adder & its Implementation on FPGA.
3. Adilakshmi Siliveru, M Bharathi,"Design of kogge Stone and Brent kung adders using Degenerate Pass Transistor Logic".
4. O. J. Bedrij, "Carry-Select Adder", IRE transactions on Electronics Computers, vol.EC-11, pp. 340-346, June1962.
5. Young joon Kim and Lee-Sup Kim, "64-bit carry-select adder with reduced area", Electronics Letters, vol.37, issue 10, pp.614-615, May 2001.
6. Y. Choi, "Parallel Prefix Adder Design", Proc. 17th IEEE Symposium on Computer Arithmetic, p 90-98, 27th June 2005.
7. Pakkiraiah Chakali, Madhu Kumar Patnala, "Design of High speed Kogge-stone based Carry Select Adder".