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A NOVEL METHOD OF POWER QUALITY IMPROVEMENT OF UNIFIED POWER QUALITY CONDITIONER BY USING FUZZY LOGIC CONTROLLER

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ABSTRACT-
In this paper Fuzzy based unified power quality conditioner for power quality improvement is presented. Unified power quality conditioner is a compensating device which is made for mitigation of all power quality problems together. This device will reduce harmonics which affects the quality of power. Unified power quality conditioner is the combinations of series active power filter and shunt active power filter which are joined back to back by a common DC link through capacitor. The performance of the filters mainly depends on its control strategy. A Fuzzy Logic Controller (FLC) is based on fuzzy sets and fuzzy rules with their membership functions of inputs and outputs. In this paper control technique is used for series active power filter and shunt active power filter is synchronous Reference frame (SRF) and instantaneous PQ (IPQ) used to compensate power quality problems by a three phase unified power quality conditioner under imbalanced and distorted load conditions. This paper accentuates improvement of power quality by using Unified power quality conditioner with proportional integral controller and fuzzy logic controller and comparing it with without compensating devices. The performance and behavior of the proposed controllers has been evaluated through MATLAB/SIMULINK.

Keywords-*Active filter, dual control strategy, power conditioning, three-phase distribution systems, unified power qualityconditioner (UPQC), Fuzzy Logic Controller.*

I. INTRODUCTION

The demand for power quality (PQ) improvement has been growing in recent years, mainly due to the increase of nonlinear loads connected to the electrical power system causing distortions in the utility voltages at the point of common coupling. Other PQ problems, such as voltage sags/swells and voltage unbalances can also affect the proper operation of sensitive equipment causing malfunction. Furthermore, additional procedures should be taken into account in order to overcome PQ problems associated with harmonic currents generated by nonlinear loads, load unbalances, and reactive power demanded by the load. Several procedures have been adopted to mitigate PQ problems, which can be carried out by means of active power-line conditioners, such as unified PQ conditioners (UPQCs), shunt, series and hybrid active power filters (APFs), and dynamic voltage restorers. By means of single-phase or three-phase topologies, shunt APFs are placed in parallel with non-linear loads, and controlled to operate as a non sinusoidal cur-rent source. In three phase systems, they can only be employed for compensating harmonic currents or load unbalances and load reactive power compensation. Operating as non sinusoidal voltage sources or sinusoidal current sources, series APF filters, which are placed between the utility grid and the load, can compensate harmonic currents, load un-balances, and reactive power of the load, while the load volt-ages are regulated. On the other hand, UPQC

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systems can perform, simultaneously, the series–parallel active power-line compensation by using both series and parallel APFs. Thus, for overcoming utility PQ problems, UPQCs have been employed based on different concepts and solutions, comprising single-phase systems or in three-phase applications, considering three phase three-wire (3P3W) systems or three-phase four-wire (3P4W) systems.

Accordingly, in most UPQC-based applications, the series and parallel APFs are controlled as non sinusoidal sources by using non sinusoidal references to control voltage and current quantities. It is well known that non sinusoidal references are difficult to be synthesized by Pulse width-modulated (PWM) converters and require an additional effort in order to achieve good performance in APF or UPQC applications. On the other hand, sinusoidal control references have been used in applications involving uninterruptible power supply (UPS) systems, such that in the standby operation mode the UPS system acts similarly to a UPQC performing the series–parallel power compensation. In this application, the series converter is controlled to operate as a sinusoidal current source rather than a non-sinusoidal voltage source, while in the parallel conditioning the parallel converter is controlled to operate as a sinusoidal voltage source rather than a non-sinusoidal current source.

In addition, this dual compensation strategy has also been tested in UPQC applications. Thus, different from the conventional conditioning strategy, which uses non sinusoidal control references, the dual compensating strategy uses only sinusoidal references to control the PWM converters. As a result, the generation of the control references is easier to obtain, allowing the use of simpler algorithms to accomplish this aim. It can be noted that, since the parallel converter is controlled to handle only sinusoidal voltages, the utility voltage components that are different from the positive-sequence components will appear across the series coupling transformers so that they are indirectly compensated without the need to calculate any non-sinusoidal compensation reference voltages. Moreover, since the output voltages are controlled to be in phase with the utility voltages, the use of a phase-locked loop (PLL) system operating with constant amplitude is necessary in order to generate the sinusoidal output voltage references.

II. UPQC TOPOLOGY DESCRIPTION

The UPQC topology employed to implement the dual compensation strategy presented in this paper is shown in Fig.1.It comprises both three-leg (3-Leg) and four-leg (4-Leg) PWMconverters sharing the same dc-link.

The UPQC is connected between a 3P3W power supply distribution system and a 3P4W plant site composed of several types of three-phase and single-phase loads. It is assumed that the single-phase loads use the neutral conductor to operate. In this case, a 3P4W distribution system is necessary, which is composed of three power conductors and a neutral conductor tofeed the loads. Thus, as can be noted in the UPQC-based 3P4 Distribution system shown in Fig.1, the neutral current flows through the wire conductor connected to the fourth leg of the shunt 4-Leg PWM converter.

The 4-Leg PWM converter was chosen to actas the shunt APF, because it is able to operate with lowerDC-link voltage amplitude when compared to the 3-Leg PWM split-capacitor topology. In addition, the 3-Leg splitcapacitor topology requires an additional control loop to compensate its inherent dc-link capacitor voltage unbalances. Although the 4-Leg converter has a greater number of switches,the power rating of the devices that compose its fourth leg isreduced, because the

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current that flows through the neutral conductor in most cases is low.

a) Dual Compensation Principle

In order to make the input currents sinusoidal, balanced and in phase with the utility voltages, in the dual compensating strategy, the series PWM converter is controlled to operate as a sinusoidal current source. In this case, its impedance must be high enough to isolate the harmonic currents generated by the nonlinear loads. On the other hand, the parallel PWM converter also makes the output voltages sinusoidal, balanced, regulated and in phase with the utility voltages. In other words, it is controlled to operate as a sinusoidal voltage source, such that its impedance must be sufficiently low to absorb the load harmonic currents.

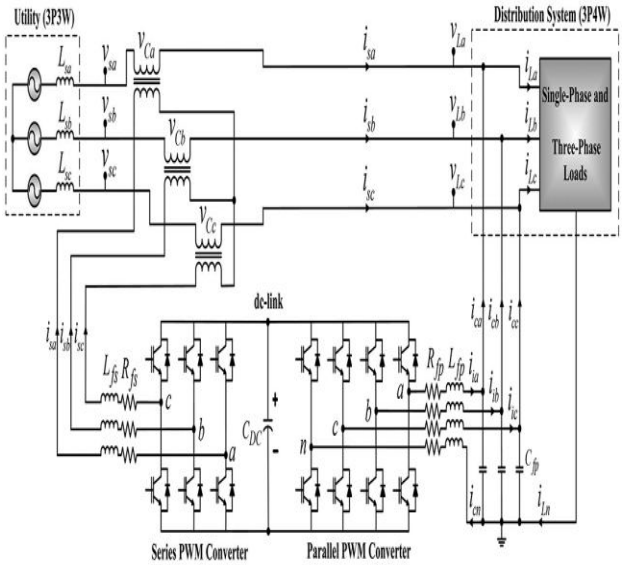

Fig.1. 3P4W distribution system based on UPQC topology connected to 3P3W power system

Since the series and parallel converters have high and low impedances, respectively, the load harmonic currents flow naturally through the parallel converter. Furthermore, compensation for load unbalances is ensured by controlling the series converter to follow sinusoidal and balanced references so that the negative and zero sequence components are compensated. Finally, the fundamental reactive power compensation is ensured by controlling the series converter current references to be in phase with the utility voltages.

On the other hand, the utility harmonic voltages and unbalances are compensated ensuring that the controlled output voltages follow sinusoidal and balanced references such that the amplitude differences between the input and output voltages will appear across the series coupling transformers, meaning that any utility voltage disturbances are naturally compensated. This makes the dual compensating strategy more attractive than the conventional strategy, considering that the load is less affected by the occurrence of grid voltage disturbances, such as voltage sags. This is possible because, different from the conventional strategy in which the series converter controls the output voltages, in the dual compensating strategy this task is entirely assumed by the parallel converter.

III. MODELING OF SERIES AND PARALLEL CONVERTERS

The modeling of the series and parallel PWM converters are presented in this section. In addition, the voltage and current controllers implemented in the SRF (dq0 axes) are discussed.

a) Series Converter Modeling

The state-space system and the transfer functions of the series converter in the dq axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances and resistances are identical, as follows: Lfsa = Lfsa = Lfsa = Lfsb = Lfsc = Lf s and Rfsa =Rfsb = Rfsc = Rfs. By means of Fig.1, the equations that represent the system are given by (1) and (2)

$$u_{sab\_PWM} = v_{L_{fsa}} + v_{R_{fsa}} + v_{C_{ab}} - v_{R_{fsb}} - v_{L_{fsb}} \quad (1)$$

$$u_{sbc\_PWM} = v_{L_{fsb}} + v_{R_{fsb}} + v_{C_{bc}} - v_{R_{fsc}} - v_{L_{fsc}} \quad (2)$$

Whereusab PWM and usbc PWM are the respective PWM voltages at the 3-Leg series converter terminals considering the voltages of

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the PWM series converter in thedq axes (usd_PWM and usq_PWM), the state-space equation is given by

$$\dot{x}_{\mathrm{sdq}}(t) = A_{\mathrm{sdq}} x_{\mathrm{sdq}}(t) + B_{\mathrm{sdq}} u_{\mathrm{sdq}}(t) + F_{\mathrm{sdq}} w_{\mathrm{sdq}}(t) \quad (3)$$

Where

$$\dot{x}_{\mathrm{sdq}}(t) = \begin{bmatrix} \frac{di_{\mathrm{sd}}}{dt} \\ \frac{di_{\mathrm{sq}}}{dt} \end{bmatrix}, \; x_{\mathrm{sdq}}(t) = \begin{bmatrix} i_{\mathrm{sd}} \\ i_{\mathrm{sq}} \end{bmatrix}, \; u_{\mathrm{sdq}} = \begin{bmatrix} u_{sd\_\mathrm{PWM}} \\ u_{sq\_\mathrm{PWM}} \end{bmatrix}$$

$$w_{\mathrm{sdq}}(t) = \begin{bmatrix} v_{\mathrm{cd}} \\ v_{\mathrm{cq}} \end{bmatrix}, \; A_{\mathrm{sdq}} = \begin{bmatrix} -\frac{R_{fs}}{L_{fs}} & \omega \\ -\omega & -\frac{R_{fs}}{L_{fs}} \end{bmatrix},$$

$$B_{\mathrm{sdq}} = \frac{1}{3L_{fs}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$F_{\mathrm{sdq}} = \frac{1}{3L_{fs}} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}.$$

Thereby, based on (3), the series converter average model represented as a signal flow graph is shown in the dotted area of Fig.2 (a). In addition, the current controller into the *dq*axes is also shown, where *Gs*(PI)*d* and *Gs*(PI)*q* represent the transfer functions of the PI current controllers; *D*sd and *D*sq arethe duty cycles; *V*dc is the dc-bus voltage; and *K*PWM is thegain of the PWM modulator given by *K*PWM = 1/*P*PWM [31],where *P*PWM is the peak value of the PWM triangular carrier implemented in the digital signal processor (DSP). The current coupling between the *dq*axes, shown in the average model ofFig.2 (a), is eliminated by using the scheme presented inFig. 2(b), where the dotted blocks represent the decoupling effects implemented in the block diagram shown in Fig. 2(a).

Thus, based on Fig.2 (a), the transfer functions of the closed loop system can be represented by (4), where $Kp_{s(d,q)}$ and $Ki_{s(d,q)}$ are the proportional and integral controller gains, and $i^*_{s(d,q)}$ represents the continuous current references in the *dq*coordinates

$$\frac{i_{S(d,q)}(s)}{i^*_{S(d,q)}(s)} = \frac{X_1\left(Kp_{s(d,q)}s + Ki_{s(d,q)}\right)}{L_{fs}s^2 + \left(R_{fs} + X_1 Kp_{s(d,q)}\right)s + X_1 Ki_{s(d,q)}} \quad (4)$$

Where X1 = K_{PWM}Vdc

b) Parallel Converter Modeling

The state-space system and the transfer functions of the parallel converter in the dq0 axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances, resistances and capacitances are identical, as follows: Lfpa = Lfpb = Lfpc = Lfpn = Lfp, Rfpa =Rfpb = Rfpc = Rfpn = Rfp, and Cfpa = Cfpb = Cfpc = Cfp.

By means of Fig.1, the equations that represent the system are given by (5), (6), and (7) as follows:

$$u_{\mathrm{pan\_PWM}} = R_{\mathrm{fpa}} \cdot i_{\mathrm{ia}} + L_{\mathrm{fpa}} \frac{di_{\mathrm{ia}}}{dt} + v_{\mathrm{La}} + L_{\mathrm{fpn}} \frac{di_{\mathrm{cn}}}{dt} + R_{\mathrm{fpn}} \cdot i_{\mathrm{cn}} \quad (5)$$

$$u_{\mathrm{pbn\_PWM}} = R_{\mathrm{fpb}} \cdot i_{\mathrm{ib}} + L_{\mathrm{fpb}} \frac{di_{\mathrm{ib}}}{dt} + v_{\mathrm{Lb}} + L_{\mathrm{fpn}} \frac{di_{\mathrm{cn}}}{dt} + R_{\mathrm{fpn}} \cdot i_{\mathrm{cn}} \quad (6)$$

$$u_{\mathrm{pcn\_PWM}} = R_{\mathrm{fpc}} i_{\mathrm{ic}} + L_{fcc} \frac{di_{\mathrm{ic}}}{dt} + v_{\mathrm{Lc}} + L_{\mathrm{fpn}} \frac{di_{\mathrm{cn}}}{dt} + R_{\mathrm{fpn}} \cdot i_{\mathrm{cn}} \quad (7)$$

Whereu_{pan}_PWM,u_{pbn}_PWM, and u_{pcn}_PWM are the respectivePWM voltages at the terminals *a*, *b*, and *c* of the 4-Leg parallel converter.

The capacitor currents of the output filters (i_{Cfpa}, $i_{\mathrm{Cfp\,b}}$ handi_{icapc}) are given by

$$i_{C_{\mathrm{fpa}}} = C_{\mathrm{fpa}} \frac{dv_{\mathrm{La}}}{dt} = i_{\mathrm{ia}} - i_{\mathrm{ca}} \quad (8)$$

$$i_{C_{\mathrm{fpb}}} = C_{\mathrm{fpb}} \frac{dv_{\mathrm{Lb}}}{dt} = i_{\mathrm{ib}} - i_{\mathrm{cb}} \quad (9)$$

$$i_{C_{\mathrm{fpc}}} = C_{\mathrm{fpc}} \frac{dv_{\mathrm{Lc}}}{dt} = i_{\mathrm{ic}} - i_{\mathrm{cc}} \quad (10)$$

Wherei_{ia}, i_{ib}, and i_{ic} are the currents of the inductors, and ica,icb, and icc are the output currents of the parallel converter.

Considering the PWM converter voltages of the parallel synchronous rotating frame the state-space equation is found as

$$(u_{\mathrm{pd\_PWM}}, u_{pq\_\mathrm{PWM}}, \text{and } u_{p0\_\mathrm{PWM}}),$$

$$\dot{x}_{\mathrm{pdq0}}(t) = A_{\mathrm{pdq0}} x_{\mathrm{pdq0}}(t) + B_{\mathrm{pdq0}} u_{\mathrm{pdq0}}(t) + F_{\mathrm{pdq0}} w_{\mathrm{pdq0}}(t) \quad (11)$$

Where

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$$\dot{x}_{\mathrm{pdq0}}(t) = \left[\frac{di_{\mathrm{id}}}{dt}\ \frac{di_{\mathrm{iq}}}{dt}\ \frac{di_{\mathrm{i0}}}{dt}\ \frac{dv_{\mathrm{Ld}}}{dt}\ \frac{dv_{\mathrm{Lq}}}{dt}\ \frac{dv_{\mathrm{L0}}}{dt}\right]^T$$

$$x_{\mathrm{pdq0}}(t) = \left[i_{\mathrm{id}}\ i_{\mathrm{iq}}\ i_{\mathrm{i0}}\ v_{\mathrm{Ld}}\ v_{\mathrm{Lq}}\ v_{\mathrm{L0}}\right]^T$$

$$u_{\mathrm{pdq0}}\begin{bmatrix} u_{\mathrm{pd\_PWM}} \\ u_{\mathrm{pq\_PWM}} \\ u_{\mathrm{p0\_PWM}} \end{bmatrix},\ w_{\mathrm{pdq0}}\begin{bmatrix} i_{C_{\mathrm{fpd}}} \\ i_{C_{\mathrm{fpq}}} \\ i_{C_{\mathrm{fp0}}} \end{bmatrix}$$

$$A_{\mathrm{pdq0}} = \begin{bmatrix} -\frac{R_{\mathrm{fp}}}{L_{\mathrm{fp}}} & \omega & 0 & -\frac{1}{L_{\mathrm{fp}}} & 0 & 0 \\ -\omega & -\frac{R_{\mathrm{fp}}}{L_{\mathrm{fp}}} & 0 & 0 & -\frac{1}{L_{\mathrm{fp}}} & 0 \\ 0 & 0 & -\frac{R_{\mathrm{fp}}}{L_{\mathrm{fp}}} & 0 & 0 & -\frac{1}{4L_{\mathrm{fp}}} \\ \frac{1}{C_{\mathrm{fp}}} & 0 & 0 & 0 & \omega & 0 \\ 0 & \frac{1}{C_{\mathrm{fp}}} & 0 & -\omega & 0 & 0 \\ 0 & 0 & \frac{1}{C_{\mathrm{fp}}} & 0 & 0 & 0 \end{bmatrix}$$

$$B_{\mathrm{pdq0}} = \begin{bmatrix} \frac{1}{L_{\mathrm{fp}}} & 0 & 0 \\ 0 & \frac{1}{L_{\mathrm{fp}}} & 0 \\ 0 & 0 & \frac{1}{4L_{\mathrm{fp}}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

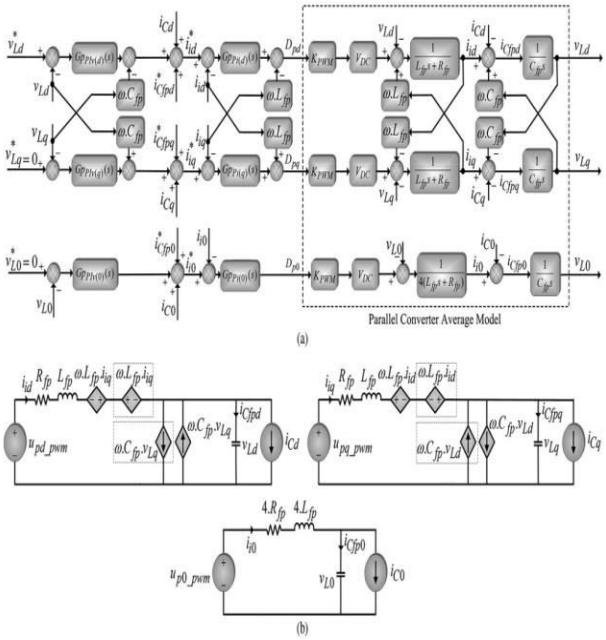

Fig.2. Parallel converter: (a) signal flow graph of the voltage controllers and average model; (b) model of the uncoupled system in SRF dq0 axes.

$$F_{\mathrm{pdq0}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -\frac{1}{C_{\mathrm{fp}}} & 0 & 0 \\ 0 & -\frac{1}{C_{\mathrm{fp}}} & 0 \\ 0 & 0 & -\frac{1}{C_{\mathrm{fp}}} \end{bmatrix}$$

Thereby, based on (11), the parallel converter average model represented as a signal flow graph is shown in the dotted area ofFig.3 (a). In addition, the voltage and current controllers into the*dq*0 axes are presented.

Where*Gp*PI*v* (*d*), *Gp*PI*v* (*q*), and *p*PI*v* (0) represent the transfer functions of the PI voltage controllers (outer loops); *Gp*Pi (*d*), *Gp*Pi (*q*), and *Gp*Pi (0) are the transfer functions of the proportional current controllers (inner loops); and*D*pd, *D*pq, and *D*p0 are the duty cycles. The current and voltage coupling between the *dq*axes shown in the averagemodel of Fig.3 (a) is eliminated by using the scheme presented inFig.3 (b), where the dotted blocks represent the decoupling effects, which are implemented in the block diagram shown inFig.3 (a).

Thus, based on Fig.3(a), the transfer functions of the closed-loop system can be represented by (3.12) and (13), where*Kpp*(*d,q*), *Kip*(*d,q*), and *Kip*(0) are the proportional and integral gains of the controllers (outer voltage control loop), *Kp*PI(*d,q*)and *Kp*PI(0) are the proportional gains (inner current-control loop), and $v^*_{L(d,q,0)}(s)$ represents the continuousvoltage references in the dq0 coordinates.

The currents of the filter capacitors icfp(d,q,0) shown inFig.3(a) are estimated considering the derivatives of the measured output voltages (vLa,b,c)and the respective capacitances(Cfpa,b,c)

$$\frac{v_{L(d,q)}(s)}{v^*_{L(d,q)}(s)} = \frac{X_{1(d,q)}s^2 + X_{2(d,q)}s + X_{3(d,q)}}{Y_{1(d,q)}s^3 + Y_{2(d,q)}s^2 + Y_{3(d,q)}s + Y_{4(d,q)}} \quad (12)$$

$$\frac{v_{L(0)}(s)}{v^*_{L(0)}(s)} = \frac{X_{1(0)}s^2 + X_{2(0)}s + X_{3(0)}}{Y_{1(0)}s^3 + Y_{2(0)}s^2 + Y_{3(0)}s + Y_{4(0)}} \quad (13)$$

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IV. STABILITY ANALYSIS OF THE SYSTEM

The stability study of the UPQC system, which involves the series and parallel converters. The aim of this study was to verify the ability of the system to remain stable even under load disturbances.

a) Series APF

Considering the signal flow graph of the current controller and the series converter average model shown in Fig.2 (a), the closed-loop transfer function in the d-q coordinates can be represented by (4). Thereby, the stability analysis of the series converter involves only the second-order denominator (λi) of (4). By applying the Routh–Hurwitz stability criterion, the necessary and sufficient condition for ensuring the series converter stability is that all the coefficients of λi must have the same sign. As can be noted, all the coefficients are positive, meaning that the series converter control is always stable. In addition, load transients only affect the generation of the series current references. Therefore, since the reference currents are always sinusoidal, it is possible to assume that the series converter remains acting as a sinusoidal current source even when load transients occur.

b)Parallel APF

Considering the signal flow graph of the voltage controllers and the parallel converter average model shown in Fig.3 (a), the closed-loop transfer functions in the dq0 coordinates can be represented by (12) and (13). Considering that the PI controller gains KpPI = KpPI(d,q) = KpPI(0)/4,Kpp = Kpp(d,q) = Kpp(0), and Kip = Kip(d,q) = Kip(0),the same transfer function is obtained for each control loop implemented in the d, q, and 0 coordinates as given by (14), allowing the study of the voltage control loops by means of a unique transferfunction Gv (s). In addition, it is assumed that the individual control loops in the dq0 coordinates are obtained taking into account the coupling effects between the d-q coordinates shown in Fig.3.

$$G_v(s) = \frac{v_{L(d,q,0)}(s)}{v^*_{L(d,q,0)}(s)} = \frac{(1+K)\left[X_{1(d,q,0)}s^2 + X_{2(d,q,0)}s + X_{3(d,q,0)}\right]}{Y_{1(d,q,0)}s^3 + Y_{2(d,q,0)}s^2 + Y_{3(d,q,0)}s + Y_{4(d,q,0)}} \quad (14)$$

Where

$$X_{1(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}C_{\mathrm{fp}}Kp_{\mathrm{PI}}$$
$$X_{2(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}}Kp_p$$
$$X_{3(d,q,0)} = Y_{4(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}}Ki_p$$
$$Y_{1(d,q,0)} = C_{\mathrm{fp}}L_{\mathrm{fp}}$$
$$Y_{2(d,q,0)} = C_{\mathrm{fp}}(K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}} + R_{\mathrm{fp}})$$
$$Y_{3(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}}Kp_p + 1.$$

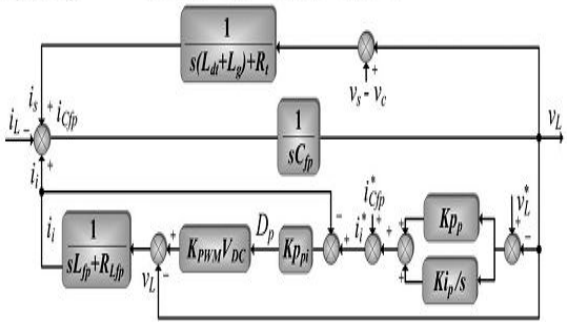

Fig.3. Parallel converter equivalent model used to stability analysis for thedq0 voltage control loops

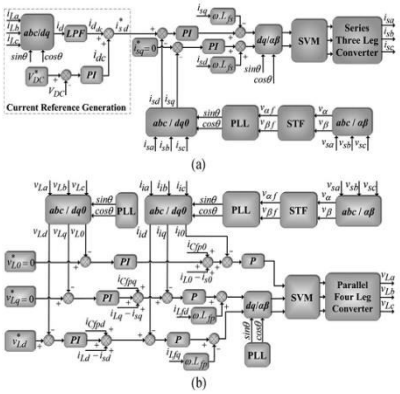

Fig.4. Signal flow graphs of the reference generation and control scheme of both series and parallel PWM converters: (a) reference current generation and the input current controllers; (b) output voltage controllers.

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However, it is not possible to analyze how the load current transients will interfere in the controls of the UPQC output voltages only by using the transfer function Gv (s). Thus, Fig.4presents the block diagram, which is based on the control loops shown in Fig.3 (a), as well as the aforementioned considerations. Thus, the load current (iL) is considered as an input of the system, whereas the voltage (vL) is the output. In addition, in order to obtain an adequate representation of the system, the source current (is) is calculated from both the output voltage(vL) and input voltage (vs), taking into account the leakage inductances and resistances of the series coupling transformers (Ldt and Rt), as well as the grid equivalent inductances(Lg). Thereby, from Fig. 3.4, the closed-loop transfer function Giv(s) = vL (d, q, 0) (s) /iL (d, q, 0) (s) can be obtained by (15).By applying the Routh–Hurwitz stability criterion, two conditions must be met: 1) all the polynomial coefficients of the denominator must have the same sign and 2) the inequalityY2Y3 > Y1Y4 must be respected. Therefore, by inspecting the denominator of (15), the first condition is always met. On the other hand, the second condition can be met by adjusting the PIcontroller gains. Thus, taking into account the aforementioned conditions, the system will always be stable, even when load transients occur

$$G_{vi}(s) = \frac{v_{L(d,q,0)}(s)}{i_{L(d,q,0)}(s)} = \frac{X_1 s^2 + X_2 s + X_3}{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4} \quad (15)$$

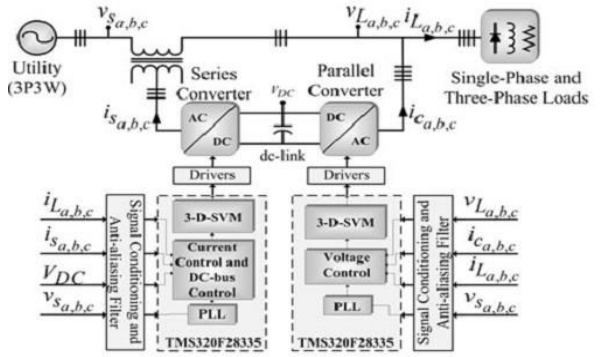

Fig.5. UPQC implementation

V. CONTROL REFERENCES OF THE SERIES AND PARALLEL CONVERTERS

The strategies used to generate the sinusoidal reference quantities used to control the series and the parallel converters are presented. As aforementioned, both the current and voltage control references are controlled to be in phase with the utility voltages. Since the controlled voltages and currents are sinusoidal quantities, a significant advantage is attained when the dual compensating strategy is compared with the conventional strategy, whose controlled quantities are always non-sinusoidal. This advantage is highlighted mainly because the control references into the SRF-based controllers are continuous, leading to reduced errors in the steady state of the PIcontrollers.

a) Series Converter Reference Currents

The current-control loop of the series converter is shown in the signal flow graph of Fig.5 (a). The continuous reference current in the SRF direct axis d is defined byi_{sd}^*, which is able to make the serial converter synthesize the sinusoidal input currents (isa, isb, isc). As can be noted, the three-dimensional space vector modulation (3-D-SVM) technique is used in the series converter.

The reference current i_{sd}^* is obtained by measuring the load currents (iLa, iLb, iLc) and converting them to the rotating reference frame. Thus, the direct current (id) is achieved by means of (16) and (17), whereas the utility phase-angle θused to calculate the coordinates of the unit vectors sin θ and cos θ,is obtained from the three-phase PLL system. Next, a low-pass filter (LPF) is employed to obtain the direct component (id_{dc}), which represents, in the SRF, the active portions of the load currents (iLa, iLb, iLc). In other words, id_{dc} represents the positive sequence components of the load currents

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$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{La}} \\ i_{\mathrm{Lb}} \\ i_{\mathrm{Lc}} \end{bmatrix} \quad (16)$$

$$i_d = i_\alpha \cos\theta + i_\beta \sin\theta \quad (17)$$

The control of the power balance flow through the UPQC must betaking into account in order to maintain the dc-bus voltage constant. Thereby, the final reference currenti_{sd}^* is calculated byusing (18), where idc is added to iddc. Thus, idc represents the control action of the dc-bus voltage controller that compensates the inherent losses of the filter elements and semiconductor devices. In addition, idc controls the balance of the power flow through the UPQC when different amplitudes between the input voltages (vsa, vsb, vsc) and output voltages (vLa, vLb, vLc) occur.

$$i_{\mathrm{sd}}^* = i_{\mathrm{dc}} + i_{d_{\mathrm{dc}}} \quad (18)$$

The reference current of the quadrature axisi_{sq}^* and i_{s0}^* areset to zero since the series converter synthesizes only positive sequence components (active currents), such that sinusoidal and balanced currents are achieved.

b) Parallel Converter Reference Voltages

The voltage control loop of the parallel converter is shown in the signal flow graph of Fig.5 (b). The reference voltage in theSRF direct axis d is defined byv_{Ld}^*. Its constant and continuousvalue represents the ac voltages (vLa, vLb, vLc) provided to theload. The reference voltages of the quadrature axis q v_{Lq}^*andv_{L0}^* are set to zero since sinusoidal and balanced voltages aredesirable. As can be noted, the 3-D-SVM technique is employed in the parallel converter.

VI. FUZZY LOGIC CONTROLLER

The Fuzzy control is a methodology to represent and implement a (smart) human's knowledge about how to control a system. A fuzzy controller is shown in Figure.6. The fuzzy controller has several components:

- A rule base that determines on how to perform control
- Fuzzification that transforms the numeric inputs so that the inference mechanisms can understand.
- The inference mechanism uses information about the current inputs and decides the rules that are suitable in the current situation and can form conclusion about system input.
- Defuzzification is opposite of Fuzzification which converts the conclusions reached by inference mechanism into numeric input for the plant.

The fuzzy logic controller provides an algorithm, which converts the expert knowledge into an automatic control strategy. Fuzzy logic is capable of handling approximate information in a systematic way and therefore it is suited for controlling nonlinear systems and is used for modeling complex systems, where an inexact model exists or systems where ambiguity or vagueness is common. The fuzzy control systems are rule-based systems in which a set of fuzzy rules represent a control decision mechanism for adjusting the effects of certain system stimuli. With an effective rule base, the fuzzy control systems can replace a skilled human operator. The rule base reflects the human expert knowledge, expressed as linguistic variables, while the membership functions represent expert interpretation of those variables.

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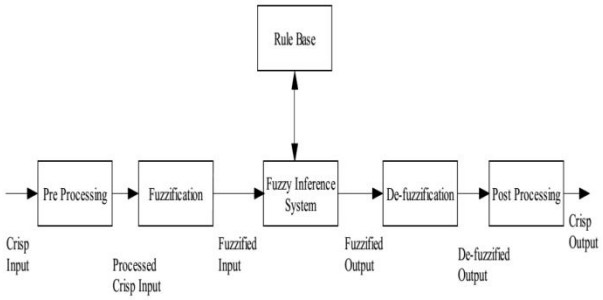

Fig.6: Block diagram of fuzzy control system

Fig.6. shows the block diagram of fuzzy control system. The crisp inputs are supplied to the input side Fuzzification unit. The Fuzzification unit converts the crisp input in to fuzzy variable. The fuzzy variables are then passed through the fuzzy rule base. The fuzzy rule base computes the input according to the rules and gives the output. The output is then passed through de-fuzzification unit where the fuzzy output is converted to crisp output.

Scaling Factor in Fuzzy Logic Controller

Scaling factor in a fuzzy logic controller is very important. Selection of suitable values for scaling factors are made based on the knowledge about the process to be controlled and sometimes through trial and error to achieve the best possible control performance. This is so because, unlike conventional non-fuzzy controllers to date, there is no well-defined method for good setting of scaling factors for fuzzy logic controllers. But the scaling factors are the main parameters used for tuning the fuzzy logic controller because changing the scaling factors changes the normalized universe of discourse, the domains, and the membership functions of input /output variables of fuzzy logic controller.

Fuzzy logic is a form of logic that is the extension of boolean logic, which incorporates partial values of truth. Instead of sentences being "completely true" or "completely false," they are assigned a value that represents their degree of truth. In fuzzy systems, values are indicated by a number (called a truth value) in the range from 0 to 1, where 0.0 represents absolute false and 1.0 represents absolute truth. Fuzzification is the generalization of any theory from discrete to continuous. Fuzzy logic is important to artificial intelligence because they allow computers to answer 'to a certain degree' as opposed to in one extreme or the other. In this sense, computers are allowed to think more 'human-like' since almost nothing in our perception is extreme, but is true only to a certain degree.

Table I : IF-THEN rules for fuzzy inference system

u(t)		e(t)						
		NB	**NM**	**NS**	**ZO**	**PS**	**PM**	**PB**
Δe(t)	**NB**	NB	NB	NB	NB	NM	NS	ZO
	NM	NB	NB	NB	NM	NS	ZO	PS
	NS	NB	NB	NM	NS	NS	PS	PS
	ZO	NB	NM	NS	ZO	ZO	PM	PM
	PS	NM	NS	ZO	PS	PS	PB	PB
	PM	NS	ZO	PS	PM	PM	PB	PB
	PB	ZO	PS	PM	PB	PB	PB	PB

The fuzzy rule base can be read as follows
IF e(t) is NB and Δe(t) is NB **THEN** u(t) is NB
IF e(t) is <negative big> and Δe(t) is <negative big>**THEN** u(t) is <negative big>.

VII. MATLAB/SIMULINK RESULTS

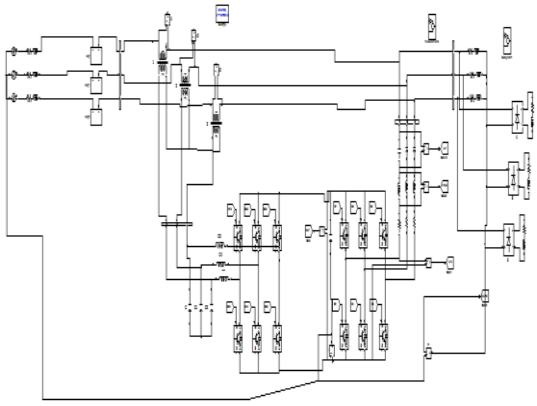

Fig.7. MATLAB/SIMULINK circuit of P4W distribution system based on UPQC topology connected to 3P3W power system

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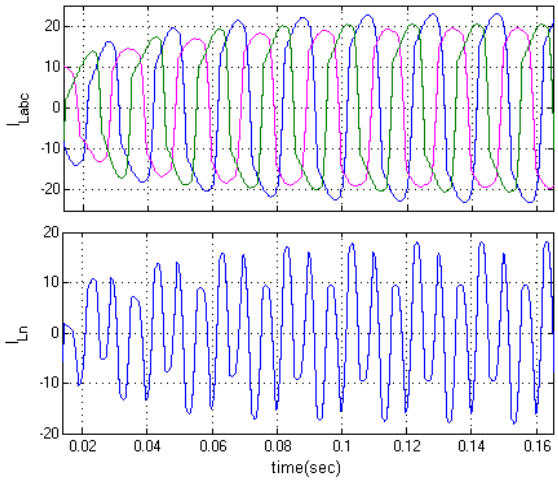


Fig.8. Output waveform of Load currents

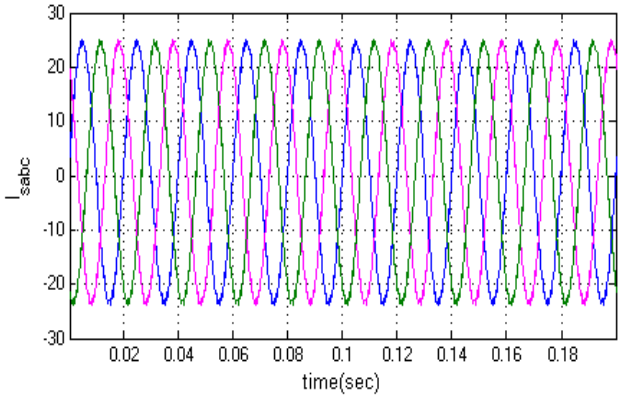


Fig.9. Output waveform of Compensated source currents

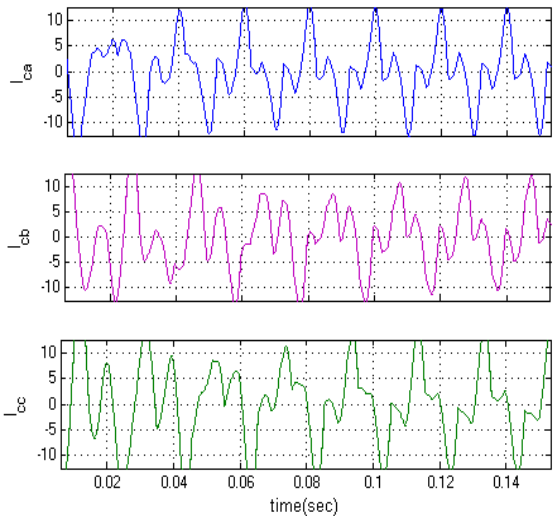
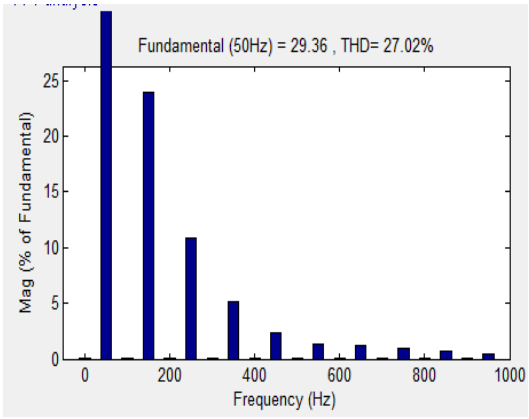
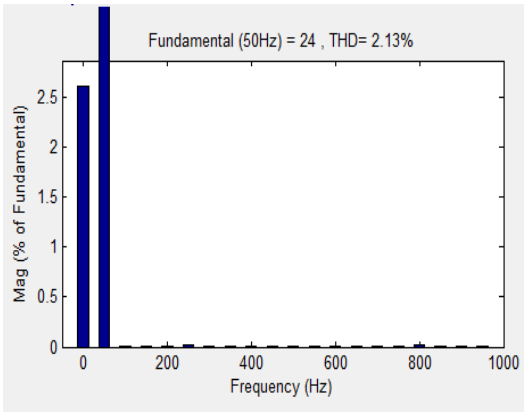


Fig.10. Output waveform of parallel converter currents



(a) Load current THD



(b) Source current THD

Fig.11. Simulation waveform for Source current THD at PI Controller

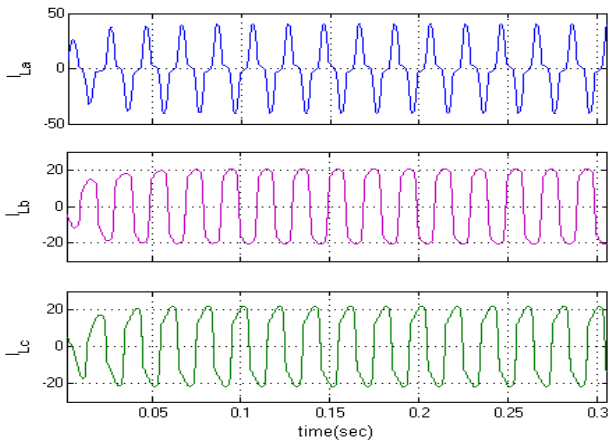


Fig.12. Output waveform of parallel converter Load currents

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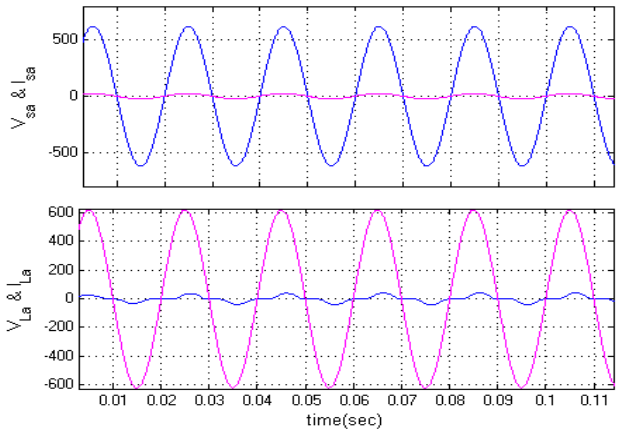

Fig.13. Output waveform of phase "a" load current, source current, utility voltage and load voltage

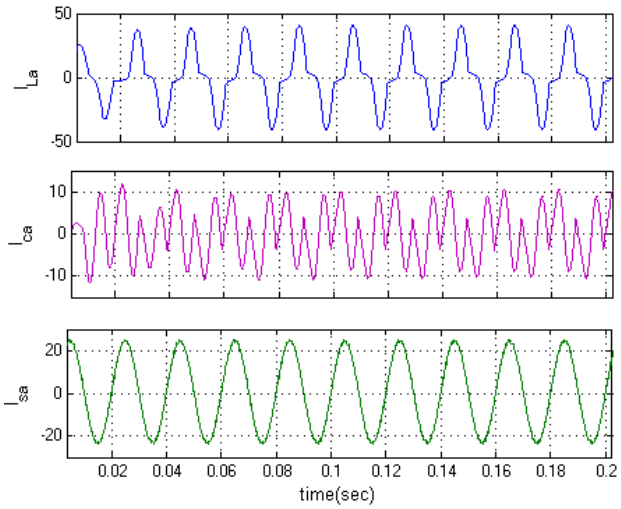

Fig.14. Output waveform of phase "a": load current, parallel converter current and source current

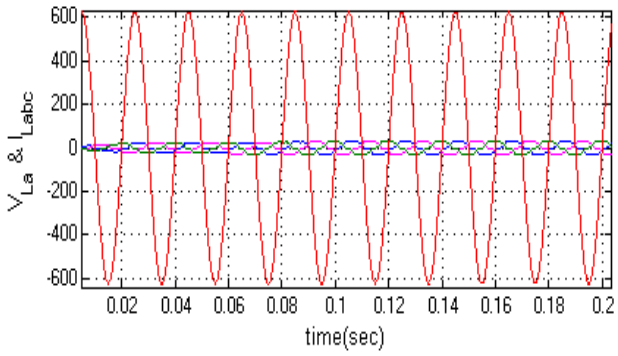

Fig.15. Output waveform of Load currents

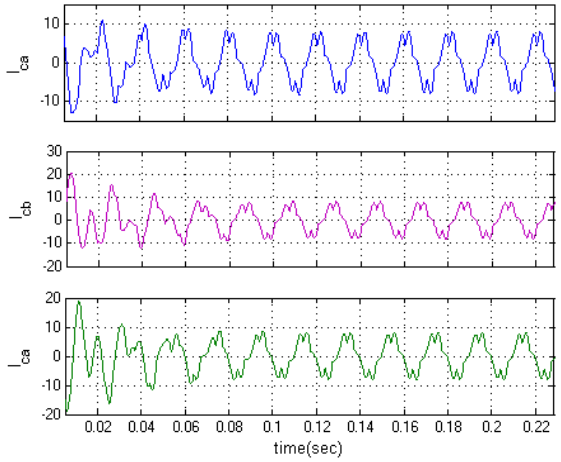

Fig.16. Output waveform of Parallel converter currents

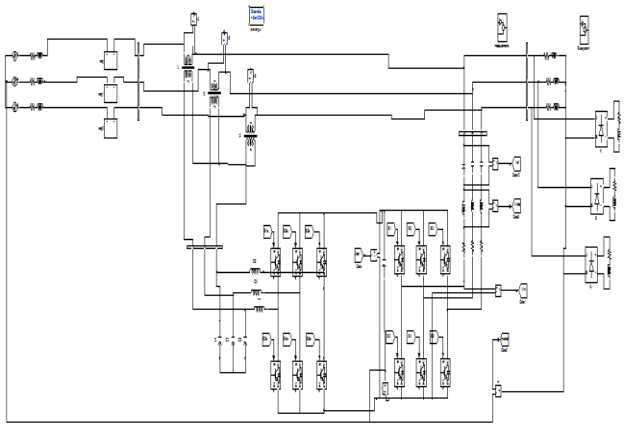

Fig.17. MATLAB/SIMULINK circuit of P4W distribution system based on UPQC topology connected to 3P3W power system with FUZZY logic control

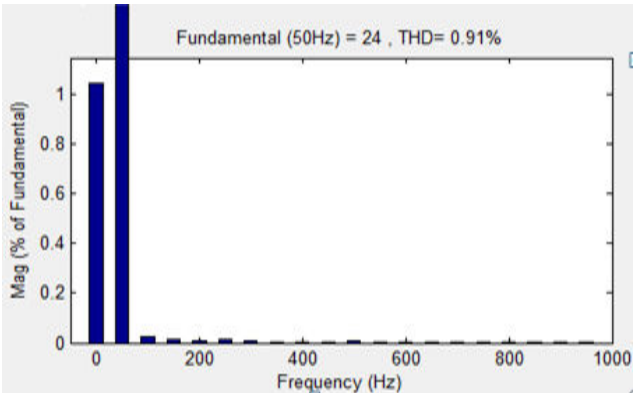

Fig.18. Simulation waveform for Source current THD at Fuzzy Logic Controller

VIII. CONCLUSION

The power quality problems in distributionsystems are not new but customer awareness of theseproblems increased recently. It is very difficult tomaintain electric power quality at acceptable limits.One modern and very promising solution that dealswith both load current and supply voltageimperfections is the Unified Power Quality
Conditioner (UPQC). This paper presented review onthe UPQC to enhance the electric power quality atdistribution level. The UPQC is able to compensatesupply voltage power quality issues such as, sags,swells, unbalance, flicker, harmonics, and for loadcurrent power quality problems such as, harmonics,unbalance, reactive current and neutral current. UPQC using Fuzzy Controller (FC) has been investigatedfor compensating reactive power and harmonics. It is clearfrom the simulation results that the UPQC using FC issimple, and is based on sensing the line currents only.

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