International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

IJIEMR Transactions, online available on 7th Febraury 2018. Link :
http://www.ijiemr.org/downloads.php?vol=Volume-7&issue=ISSUE-02

Title: A Grid connected Dual Voltage source Inverter with power quality Improvement features.

Volume 07, Issue 02, Page No: 54 – 65.

Paper Authors

***Y.DHANA LAKSHMI, MIKKILI.SURESH.**

* Dept of EEE, Sri Mittapalli Engineering College.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

A GRID CONNECTED DUAL VOLTAGE SOURCE INVERTER WITH POWER QUALITY IMPROVEMENT FEATURES.

***Y.DHANA LAKSHMI, **MIKKILI.SURESH**
*M-Tech Student Scholar, Dept of EEE, Sri Mittapalli Engineering College, Tummalapalem; Guntur (Dt); A.P, India.
**Associate Professor, Dept of EEE, Sri Mittapalli Engineering College,Tummalapalem; Guntur (Dt); A.P, India.

ABSTRACT:
Dual voltage source inverter (DVSI) scheme to enhance the power quality and reliability of the micro-grid system. The proposed scheme is comprised of inverters, which enables the micro-grid to exchange power generated by the distributed energy resources (DERs) and also to compensate the local unbalanced and nonlinear. The control algorithms are developed based on instantaneous symmetrical component theory (ISCT) to operate DVSI in grid sharing and grid injection modes. The advantages are increasing system reliability, lower bandwidth requirement of the main inverter, lower cost due to reduction in filter size and better utilization of micro grid while using reduced dc-link voltage rating for the main inverter. These important features make DVSI scheme a promising option for micro grid supplying sensitive loads. The above discussed inverter is fed to a induction motor drive and the performance of the motor is analyzed for Grid-Connected Dual Voltage Source Inverter**.**

Keywords: Dual inverter, (ISCT), micro grid, power quality

1.INTRODUCTION

To drive the power system there are many models or pattern with more renewable energy sources interlinked with the network by using distributed generation (DG). These DG units can control of local generation, storage facilities from a micro-grid. A micro-grid, power can be taken from the different renewable energy sources such as fuel cells, photovoltaic systems, and wind energy systems are merged to grid and loads using (PEC) power electronic converters. To exchange the power from micro-grid to grid and connected load by using an interactive grid inverter. This micro-grid inverter can either work in a grid sharing mode or in grid injecting mode, the grid sharing is done while supplying a part of local load, the grid injecting is done by injecting power to the main grid.Another important aspect is maintaining power quality it has to be done when the micro grid is connected to the main grid. The number of feeder impedance in the distribution systems, the propagation of these harmonic currents distorts the voltage at the point of common coupling (PCC). The micro grid generating power from main voltage source inverter (MVSI) as real power and the compensation of reactive, harmonic, and unbalanced load compensation which performed by (AVSI) auxiliary voltage source inverter. An important advantage of MVSI that it can always be used to inject real power to the grid with rated capacity and it also as sufficient renewable power is available at the dc link.

The two inverters is supplies total power to the load and also reduces the switching losses across the semiconductor switches. By this reduction of losses will increase the system reliability when it compares to single inverter. In this scheme a smaller size modular inverters are used. Because these inverters can operate at high switching frequencies with a reduced size

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

of interfacing inductor, so that the filter cost gets reduced. The main inverter which supplies the real power to track the fundamental positive sequence of current and also the inverter reduces the bandwidth requirement of the main inverter.

The inverters in the present scenario use two separate dc links. Since the auxiliary inverter is supplying zero sequence of load current. In MVSI the single dc storage capacitor with three-phase three-leg inverter structure can be used. It reduces the dc-link voltage requirement of the main inverter. Thus, the use of AVSI and DVSI inverters in the system structure which provides the system reliability, micro-grid power is utilized better and also reduces the voltage rating of the grid. Control algorithms is developed (ISCT) to operate DVSI in grid connected mode when considering non stiff grid voltage. The dq0 transformation method is used to extract the fundamental positive sequence of PCC voltage q0 transformation. The control strategies are measured with the parallel inverters connected to a three phase four-wire distribution system.

II. DUAL VOLTAGE SOURCE INVERTER

A.System Topology

The proposed DVSI topology is shown in Fig.1. It consists of a neutral point clamped (NPC) inverter to realize AVSI and a three-leg inverter for MVSI [18]. These are connected to grid at the PCC and supplying a nonlinear and unbalanced load. The function of the AVSI is to compensate the reactive, harmonics, and unbalance components in load currents. Here, load currents in three phases are represented by i_{la}, i_{lb}, and i_{lc}, respectively. Also, $i_{g(abc)}$,$i_{\mu gm(abc)}$, and $_{i\mu gx(}$abc) show grid currents, MVSI currents, and AVSI currents in three phases, respectively. The dc link of the AVSI utilizes a split capacitor topology, with two capacitors C1 and C2. The MVSI delivers the available power at distributed energy resource (DER) to grid.

The DER can be a dc source or an ac source with rectifier coupled to dc link. Usually, renewable energy sources like fuel cell and PV generate power at variable low dc voltage, while the variable speed wind turbines generate power at variable ac voltage. Therefore, the power generated from these sources use a power conditioning stage before it is connected to the input of MVSI. In this study, DER is being represented as a dc source. An inductor filter is used to eliminate the high-frequency switching components generated due to the switching of power electronic switches in the inverters [19]. The system considered in this study is assumed to have some amount of feeder resistance Rg and inductance Lg. Due to the presence of this feeder impedance, PCC voltage is affected with harmonics [20].

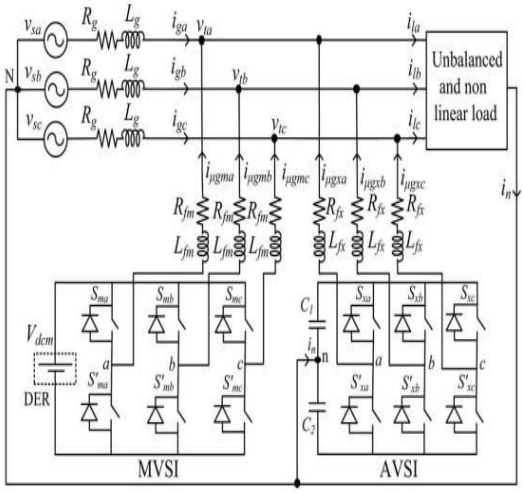

Fig.1. Topology of proposed DVSI scheme.

B. Design of DVSI Parameters

i) AVSI: The important parameters of AVSI like dc-link voltage (V_{dc}), dc storage capacitors (C_1 and C_2), interfacing inductance (L_{fx}), and hysteresis band ($\pm h_x$) are selected based on the design method of split capacitor DSTATCOM topology [16]. The dc-link voltage across each capacitor is taken as 1.6 times the peak of phase voltage. The total dc-link voltage reference (V_{dcref}) is found to be 1040 V.

Values of dc capacitors of AVSI are chosen based on the change in dc-link voltage during

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

transients. Let total load rating is S kVA. In the worst case, the load power may vary from minimum to maximum, i.e., from 0 to S kVA. AVSI needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in deviation of capacitor voltage from its reference value. Assume that the voltage controller takes n cycles, i.e., nT seconds to act, where T is the system time period. Hence, maximum energy exchange by AVSI during transient will be nST. This energy will be equal to change in the capacitor stored energy. Therefore

$$\frac{1}{2}C_1(V_{\text{dcr}}^2 - V_{\text{dc1}}^2) = nST \tag{1}$$

where V_{dcr} and V_{dc1} are the reference dc voltage and maximum permissible dc voltage across C1 during transient, respectively. Here, S = 5 kVA, V_{dcr} = 520 V, $V_{dc1} = 0.8 * V_{dcr}$ or $1.2 * V_{dcr}$, n = 1, and T = 0.02 s. Substituting these values in (1), the dclink capacitance (C1) is calculated to be 2000 µF. same value of capacitance is selected for C2.

The interfacing inductance is given by

$$L_{fx} = \frac{1.6\,V_m}{4\,h_x f_{\max}} \tag{2}$$

Assuming a maximum switching frequency (f_{max}) of 10 kHz and hysteresis band (h_x) as 5% of load current (0.5 A), the value of L_{fx} is calculated to be 26 mH.

ii) MVSI: The MVSI uses a three-leg inverter topology. Its dc-link voltage is obtained as $1.15 * V_{ml}$, where V_{ml} is the peak value of line voltage. This is calculated to be 648 V. Also, MVSI supplies a balanced sinusoidal current at unity power factor. So, zero sequence switching harmonics will be absent in the output current of MVSI. This reduces the filter requirement for MVSI as compared to AVSI [21]. In this analysis, a filter inductance (L_{fm}) of 5mH is used.

C. Advantages of the DVSI Scheme

The various advantages of the proposed DVSI scheme over a single inverter scheme with multifunctional capabilities [7]–[9] are discussed here as follows:

1) Increased Reliability: DVSI scheme has increased reliability, due to the reduction in failure rate of components and the decrease in system down time cost [13]. In this scheme, the total load current is shared between AVSI and MVSI and hence reduces the failure rate of inverter switches. Moreover, if one inverter fails, the other can continue its operation. This reduces the lost energy and hence the down time cost. The reduction in system down time cost improves the reliability.

2) Reduction in Filter Size: In DVSI scheme, the current supplied by each inverter is reduced and hence the current rating of individual filter inductor reduces. This reduction in current rating reduces the filter size. Also, in this scheme, hysteresis current control is used to track the inverter reference currents. As given in (2), the filter inductance is decided by the inverter switching frequency. Since the lower current rated semiconductor device can be switched at higher switching frequency, the inductance of the filter can be lowered. This decrease in inductance further reduces the filter size.

3) Improved Flexibility: Both the inverters are fed from separate dc links which allow them to operate independently, thus increasing the flexibility of the system. For instance, if the dc link of the main inverter is disconnected from the system, the load compensation capability of the auxiliary inverter can still be utilized.

4) Better Utilization of Microgrid Power: DVSI scheme helps to utilize full capacity of MVSI to transfer the entire power generated by DG units as real power to ac bus, as there is AVSI for harmonic and reactive power compensation. This increases the active power injection capability of DGs in microgrid [22].

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

5) Reduced DC-Link Voltage Rating: Since, MVSI is not delivering zero sequence load current components, a single capacitor three-leg VSI topology can be used. Therefore, the dclink voltage rating of MVSI is reduced approximately by 38%, as compared to a single inverter system with split capacitor VSI topology

III. CONTROL STRATEGY FOR DVSI SCHEME

A. Fundamental Voltage Extraction

The control algorithm for reference current generation using ISCT requires balanced sinusoidal PCC voltages. Because of the presence of feeder impedance, PCC voltages are distorted. Therefore, the fundamental positive sequence components of the PCC voltages are extracted for the reference current generation. To convert the distorted PCC voltages to balanced

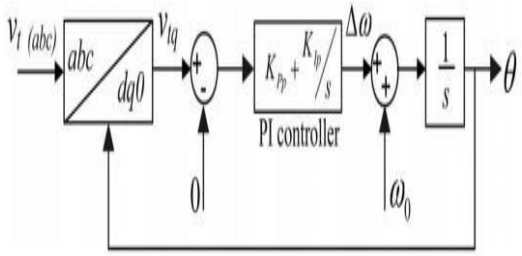

Fig.2. Schematic diagram of PLL

sinusoidal voltages, dq0 transformation is used. The PCC voltages in natural reference frame (v_{ta}, v_{tb}, and v_{tc}) are first transformed into dq0 reference frame as given by

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \quad (3)$$

Where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

In order to get θ, a modified synchronous reference frame (SRF) phase locked loop (PLL) [23] is used. The schematic diagram of this PLL is shown in Fig. 2. It mainly consists of a proportional integral (PI) controller and an integrator. In this PLL, the SRF terminal voltage in q-axis (v_{tq}) is compared with 0 V and the error voltage thus obtained is given to the PI controller. The frequency deviation Δω is then added to the reference frequency ω_0 and finally given to the integrator to get θ. It can be proved that, when, $\theta = \omega_0 t$ and by using the Park's transformation matrix (C), q-axis voltage in dq0 frame becomes zero and hence the PLL will be locked to the reference frequency (ω_0). As PCC voltages are distorted, the transformed voltages in dq0 frame (v_{td} and v_{tq}) contain average and oscillating components of voltages. These can be represented as

$$v_{td} = \bar{v}_{td} + \tilde{v}_{td}, \quad v_{tq} = \bar{v}_{tq} + \tilde{v}_{tq} \quad (4)$$

where $\bar{v}_{td}$ and $\bar{v}_{tq}$ represent the average components of vtd and vtq, respectively. The terms $\tilde{v}_{td}$ and $\tilde{v}_{tq}$ indicate the oscillating components of vtd and vtq, respectively. Now the fundamental positive sequence of PCC voltages in natural reference frame can be obtained with the help of inverse dq0 transformation as given by

$$\begin{bmatrix} v^+_{ta1} \\ v^+_{tb1} \\ v^+_{tc1} \end{bmatrix} = C^T \begin{bmatrix} \bar{v}_{td} \\ \bar{v}_{tq} \\ 0 \end{bmatrix} \quad (5)$$

These voltages v^+_{ta1} v^+_{tb1} and v^+_{tc1} are used in the reference current generation algorithms, so as to draw balanced sinusoidal currents from the grid.

B.Instantaneous Symmetrical Component Theory

ISCT was developed primarily for unbalanced and nonlinear load compensations by active power filters. The system topology shown in Fig. 3 is used for realizing the reference current for the compensator [15]. The ISCT for load

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

compensation is derived based on the following three conditions.

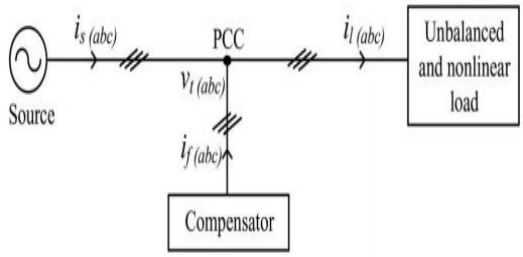

Fig.3. Schematic of an unbalanced and nonlinear load compensation scheme

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{6}$$

2) The phase angle between the fundamental positive sequence voltage(v_{ta1}^{+}) and source current (i_{sa}) is φ

$$\angle v_{ta1}^{+} = \angle i_{sa} + \phi \tag{7}$$

3) The average real power of the load (Pl) should be supplied by the source

$$v_{ta1}^{+}\, i_{sa} + v_{tb1}^{+}\, i_{sb} + v_{tc1}^{+}\, i_{sc} = P_l \tag{8}$$

Solving the above three equations, the reference source currents can be obtained as

$$i_{sa}^{*} = \left(\frac{v_{ta1}^{+} + \beta(v_{tb1}^{+} - v_{tc1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l$$
$$i_{sb}^{*} = \left(\frac{v_{tb1}^{+} + \beta(v_{tc1}^{+} - v_{ta1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l$$
$$i_{sc}^{*} = \left(\frac{v_{tc1}^{+} + \beta(v_{ta1}^{+} - v_{tb1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \tag{9}$$

.

where $\beta = Tan\emptyset/\sqrt{3}$ The term φ is the desired phase angle between the fundamental positive sequence of PCC voltage and source current. To achieve unity power factor for source current, substitute β = 0 in (9). Thus, the reference source currents for three phases are given by

$$i_{s(abc)}^{*} = \left(\frac{v_{t(abc)1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \tag{10}$$

where i_{sa}^{*}, i_{sb}^{*},and $i_{sc}^{*}$are fundamental positive sequence of load currents drawn from the source, when it is supplying an average load power Pl. The power Pl can be computed using a moving average filter with a window of one-cycle data points as given below

$$P_l = \frac{1}{T} \int_{t_1 - T}^{t_1} (v_{ta1}^{+}\, i_{la} + v_{tb1}^{+}\, i_{lb} + v_{tc1}^{+}\, i_{lc}) dt \tag{11}$$

where t_1 is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i_{f\,(abc)}^{*} = i_{l\,(abc)} - i_{s\,(abc)}^{*} \tag{12}$$

Equation (12) can be used to generate the reference filter currents using ISCT, when the entire load active power, Pl is supplied by the source and load compensation is performed by a single inverter. A modification in the control algorithm is required, when it is used for DVSI scheme. The following section discusses the formulation of control algorithm for DVSI scheme. The source currents, $i_{s(abc)}$ and filter currents $i_{f(abc)}$ will be equivalently represented as grid currents $i_{g(abc)}$ and AVSI currents $i_{\mu gx(abc)}$), respectively, in further sections.

C.Control Strategy of DVSI

Control strategy of DVSI is developed in such a way that grid and MVSI together share the active load power, and AVSI supplies rest of the power components demanded by the load.

1)Reference Current Generation for Auxiliary Inverter:

The dc-link voltage of the AVSI should be maintained constant for proper operation of the auxiliary inverter. DC-link voltage variation occurs in auxiliary inverter due to its switching and ohmic losses. These losses termed as Ploss should also be supplied by the grid. An

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

expression for Ploss is derived on the condition that average dc capacitor current is zero to maintain a constant capacitor voltage [15]. The deviation of average capacitor current from zero will reflect as a change in capacitor voltage from a steady state value. A PI controller is used to generate Ploss term as given by

$$P_{\text{loss}} = K_{Pv}\, e_{vdc} + K_{Iv} \int e_{vdc} dt \tag{13}$$

where $e_{vdc} = V_{dcref} - v_{dc}$, v_{dc} represents the actual voltage sensed and updated once in a cycle. In the above equation, K_P v and K_{Iv} represent the proportional and integral gains of dc-link PI controller, respectively. The Ploss term thus obtained should be supplied by the grid, and therefore AVSI reference currents can be obtained as given in (14). Here, the dc-link voltage PI controller gains are selected so as to ensure stability and better dynamic response during load change [24]

$$\begin{aligned} i^*_{\mu gxa} &= i_{la} - \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \\ i^*_{\mu gxb} &= i_{lb} - \left(\frac{v^+_{tb1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \\ i^*_{\mu gxc} &= i_{lc} - \left(\frac{v^+_{tc1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \end{aligned} \tag{14}$$

2) Reference Current Generation for Main Inverter:

The MVSI supplies balanced sinusoidal currents based on the available renewable power at DER. If MVSI losses are neglected, the power injected to grid will be equal to that available at DER ($P_{\mu g}$). The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (a, b, and c)

$$i^*_{\mu gm(abc)} = \left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right) P_{\mu g} \tag{15}$$

where $P_{\mu g}$ is the available power at the dc link of MVSI. The reference currents obtained from (14) to (15) are tracked by using hysteresis band current controller (HBCC). HBCC schemes are based on a feedback loop, usually with a two-level comparator. This controller has the advantage of peak current limiting capacity, good dynamic response, and simplicity in implementation [14]. A hysteresis controller is a high-gain proportional controller. This controller adds certain phase lag in the operation based on the hysteresis band and will not make the system unstable. Also, the proposed DVSI scheme uses a first-order inductor filter which retains the closed-loop system stability [25]. The entire control strategy is schematically represented in Fig.3.4. Applying Kirchhoff's current law (KCL) at the PCC in Fig.4

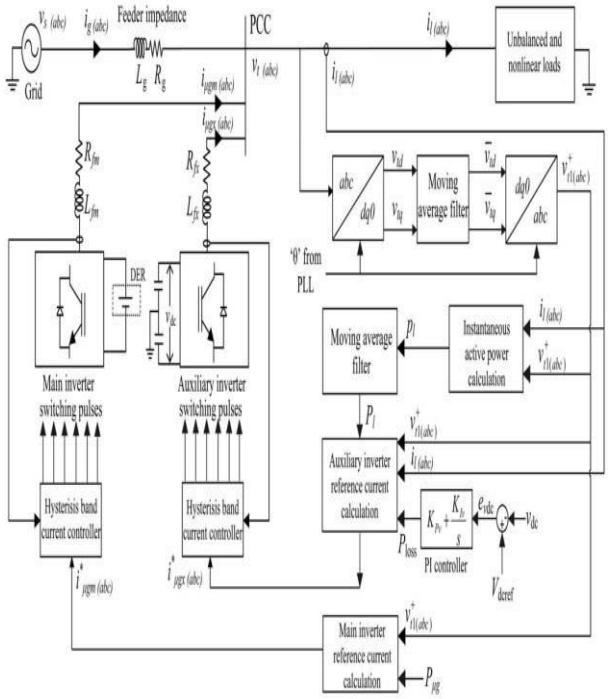

Fig.4. Schematic diagram showing the control strategy of proposed DVSI scheme.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

$$i_{\mu g x\, j} = i_{l\, j} - (i_{g\, j} + i_{\mu g m\, j}), \quad \text{for } j = a, b, c. \tag{16}$$

By using (14) and (16), an expression for reference grid current in phase-a (i^*_{ga})can be obtained as

$$i^*_{ga} = \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}} \right) [(P_l + P_{\text{loss}}) - P_{\mu g}] \tag{17}$$

It can be observed that, if the quantity (P_l + P_{loss}) is greater than Pμg, the term [(P_l + P_{loss}) − $P_{μg}$] will be a positive quantity, and i^*_{ga} .will be in phase with v^+_{ta1}. This operation can be called as the grid supporting or grid sharing mode, as the total load power demand is shared between the main inverter and the grid. The term, P_{loss} is usually very small compared to Pl. On the other hand, if (P_l + P_{loss}) is less than Pμg, then [(P_l + P_{loss}) − $P_{μg}$] will be a negative quantity, and hence i^*_{ga}. Will be in phase opposition with v^+_{ta1}. . This mode of operation is called the grid injecting mode, as the excess power is injected to grid.

IV. INDUCTION MOTOR

An asynchronous motor type of an induction motor is an AC electric motor in which the electric current in the rotor needed to produce torque is obtained by electromagnetic induction from the magnetic field of the stator winding. An induction motor can therefore be made without electrical connections to the rotor as are found in universal, DC and synchronous motors. An asynchronous motor's rotor can be either wound type or squirrel-cage type.

Three-phase squirrel-cage asynchronous motors are widely used in industrial drives because they are rugged, reliable and economical. Single-phase induction motors are used extensively for smaller loads, such as household appliances like fans. Although traditionally used in fixed-speed service, induction motors are increasingly being used with variable-frequency drives (VFDs) in variable-speed service. VFDs offer especially important energy savings opportunities for existing and prospective induction motors in variable-torque centrifugal fan, pump and compressor load applications. Squirrel cage induction motors are very widely used in both fixed-speed and variable-frequency drive (VFD) applications. Variable voltage and variable frequency drives are also used in variable-speed service.

In both induction and synchronous motors, the AC power supplied to the motor's stator creates a magnetic field that rotates in time with the AC oscillations. Whereas a synchronous motor's rotor turns at the same rate as the stator field, an induction motor's rotor rotates at a slower speed than the stator field. The induction motor stator's magnetic field is therefore changing or rotating relative to the rotor. This induces an opposing current in the induction motor's rotor, in effect the motor's secondary winding, when the latter is short-circuited or closed through external impedance. The rotating magnetic flux induces currents in the windings of the rotor; in a manner similar to currents induced in a transformer's secondary winding(s). The currents in the rotor windings in turn create magnetic fields in the rotor that react against the stator field. Due to Lenz's Law, the direction of the magnetic field created will be such as to oppose the change in current through the rotor windings. The cause of induced current in the rotor windings is the rotating stator magnetic field, so to oppose the change in rotor-winding currents the rotor will start to rotate in the direction of the rotating stator magnetic field. The rotor accelerates until the magnitude of induced rotor current and torque balances the applied load. Since rotation at synchronous speed would result in no induced

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

rotor current, an induction motor always operates slower than synchronous speed. The difference, or "slip," between actual and synchronous speed varies from about 0.5 to 5.0% for standard Design B torque curve induction motors. The induction machine's essential character is that it is created solely by induction instead of being separately excited as in synchronous or DC machines or being self-magnetized as in permanent magnet motors.

For rotor currents to be induced the speed of the physical rotor must be lower than that of the stator's rotating magnetic field (n_s); otherwise the magnetic field would not be moving relative to the rotor conductors and no currents would be induced. As the speed of the rotor drops below synchronous speed, the rotation rate of the magnetic field in the rotor increases, inducing more current in the windings and creating more torque. The ratio between the rotation rate of the magnetic field induced in the rotor and the rotation rate of the stator's rotating field is called slip. Under load, the speed drops and the slip increases enough to create sufficient torque to turn the load. For this reason, induction motors are sometimes referred to as asynchronous motors. An induction motor can be used as an induction generator, or it can be unrolled to form a linear induction motor which can directly generate linear motion.

Synchronous Speed:

The rotational speed of the rotating magnetic field is called as synchronous speed.

$$Ns = \frac{120 \times f}{P} \quad (RPM) \tag{18}$$

Where, f = frequency of the supply

P = number of poles

Slip:

Rotor tries to catch up the synchronous speed of the stator field, and hence it rotates. But in practice, rotor never succeeds in catching up. If rotor catches up the stator speed, there won't be any relative speed between the stator flux and the rotor, hence no induced rotor current and no torque production to maintain the rotation. However, this won't stop the motor, the rotor will slow down due to lost of torque, and the torque will again be exerted due to relative speed. That is why the rotor rotates at speed which is always less the synchronous speed.

The difference between the synchronous speed (Ns) and actual speed (N) of the rotor is called as slip.

$$\% \text{ slip} \quad s = \frac{Ns - N}{Ns} \times 100 \tag{19}$$

V. SIMULATION RESULTS

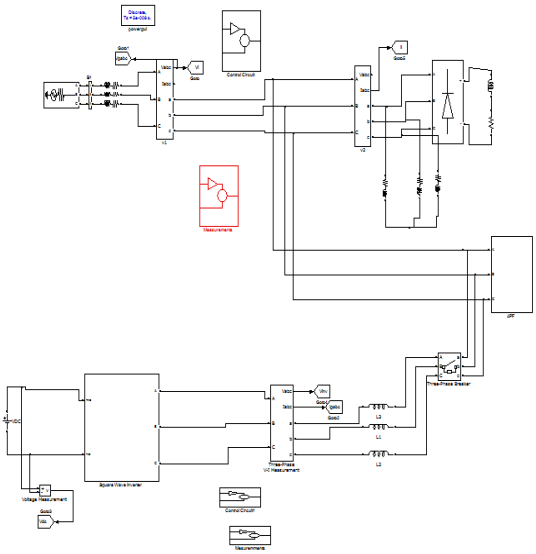

Fig.5 Simulink model diagram of the proposed DVSI scheme

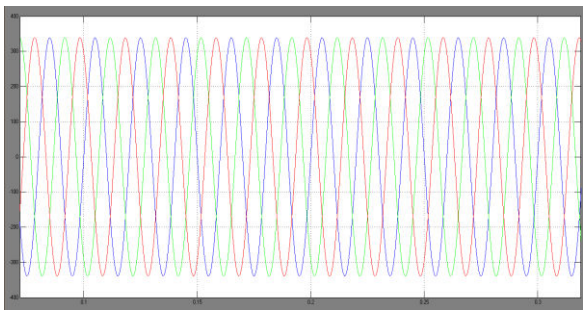

Fig.6 without DVSI scheme fundamental positive sequence of PCC voltages.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

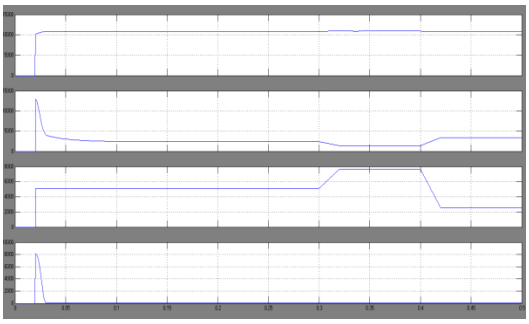

Fig.7 Active power sharing: (a) load active power; (b) active power supplied by grid; (c) active power supplied by MVSI; and (d) active power supplied by AVSI.

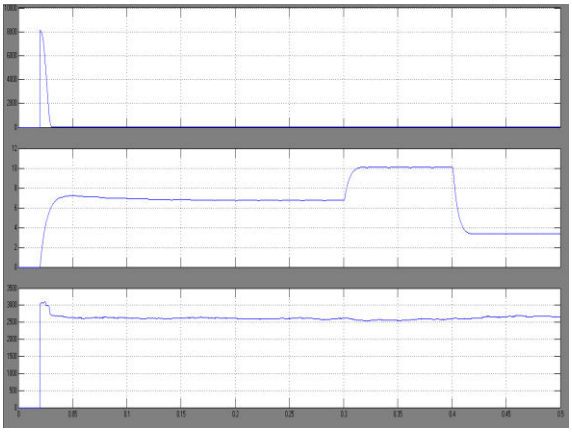

Fig.8 Reactive power sharing: (a) load reactive power; (b) reactive power supplied by AVSI; and (c) reactive power supplied by MVSI.

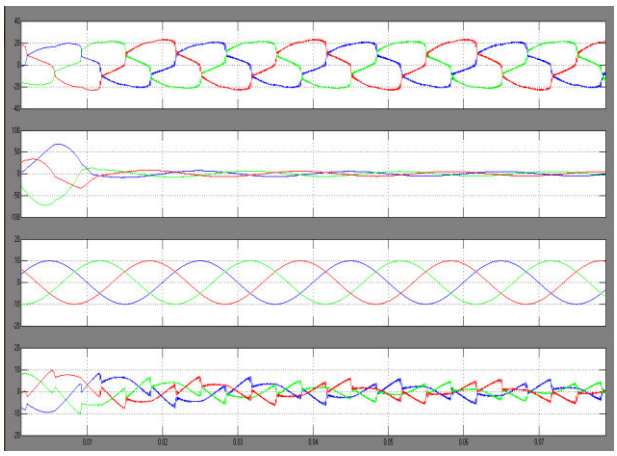

Fig.9 Simulated performance of DVSI scheme: (a) load currents; (b) grid currents; (c) MVSI currents; and (d) AVSI currents.

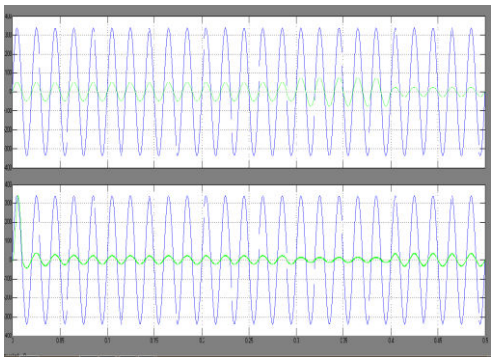

Fig. 10 Grid sharing and grid injecting modes of operation: (a) PCC voltage and grid current (phase-a) and (b) PCC voltage and MVSI current (phase-a).

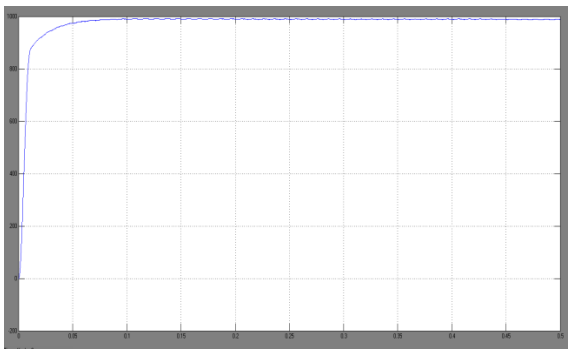

Fig. 11 DC-link voltage of AVSI

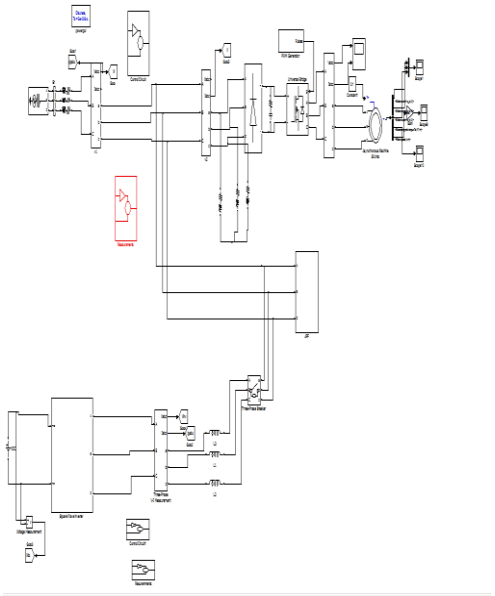

Fig. 12 Simulink model diagram of the proposed DVSI scheme with induction motor drive

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

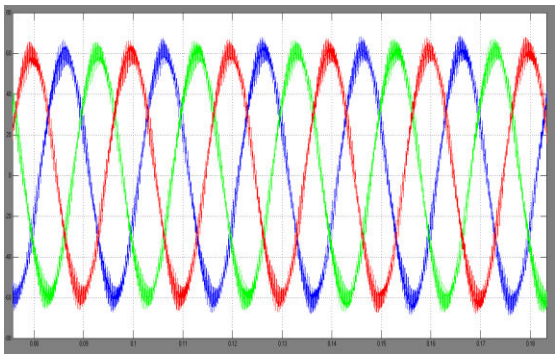

Fig.13 Stator current Characteristics Of Induction motor

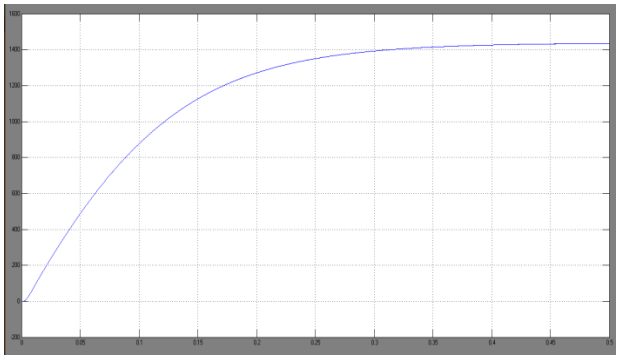

FIGURE 14 Speed of the induction motor.

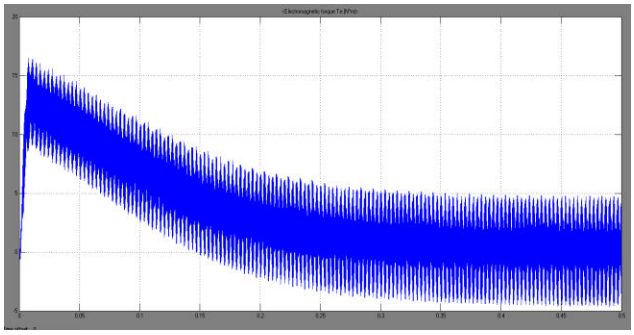

Fig.15 Torque characteristics of the induction motor.

VI. CONCLUSION

A DVSI module is published for micro grid systems to enhance the power quality. Control algorithms are improved to generate reference currents for DVSI using ISCT. The proposed module has the stability to transfer power from distributed generators (DGs) and also used to compensate the local unbalanced and nonlinear load. The performance of the proposed module has been valued through simulation and experimental results. As compared to a single inverter with multifunctional capabilities, a DVSI has many advantages such as, improving system reliability, initial cost due to the reduction in filter size, and the inverter utilized fully with capacity to inject real power from DGs to micro grid. Overall, the use of three-phase, three- wire topology for the main inverter redacts the dc-link voltage requirement. Thus, a DVSI module is a suitable interacting option for micro grid to supply sensitive loads. In this paper, a new inverter topology for induction motor drive has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability.

REFERENCES

[1] A. Kahrobaeian and Y.-R. Mohamed, "Interactive distributed generation interface for flexible micro-grid operation in smart distribution systems," IEEE Trans. Sustain. Energy, vol. 3, no. 2, pp. 295–305, Apr. 2012.

[2] N. R. Tummuru, M. K. Mishra, and S. Srinivas, "Multifunctional VSC controlled microgrid using instantaneous symmetrical components theory," IEEE Trans. Sustain. Energy, vol. 5, no. 1, pp. 313–322, Jan. 2014.

[3] Y. Zhang, N. Gatsis, and G. Giannakis, "Robust energy management for microgrids with high-penetration renewables," IEEE Trans. Sustain. Energy, vol. 4, no. 4, pp. 944–953, Oct. 2013.

[4] R. Majumder, A. Ghosh, G. Ledwich, and F. Zare, "Load sharing and power quality enhanced operation of a distributed microgrid," IET Renewable Power Gener., vol. 3, no. 2, pp. 109–119, Jun. 2009.

[5] J. Guerrero, P. C. Loh, T.-L. Lee, and M. Chandorkar, "Advanced control architectures for intelligent microgrids—Part II: Power

quality, energy storage, and ac/dc microgrids," IEEE Trans. Ind. Electron., vol. 60, no. 4, pp. 1263–1270, Dec. 2013.
[6] Y. Li, D. Vilathgamuwa, and P. C. Loh, "Microgrid power quality enhancement using a three-phase four-wire grid-interfacing compensator," IEEE Trans. Ind. Appl., vol. 41, no. 6, pp. 1707–1719, Nov. 2005.
[7] M. Schonardie, R. Coelho, R. Schweitzer, and D. Martins, "Control of the active and reactive power using dq0 transformation in a three-phase grid-connected PV system," in Proc. IEEE Int. Symp. Ind. Electron., May 2012, pp. 264–269.
[8] R. S. Bajpai and R. Gupta, "Voltage and power flow control of grid connected wind generation system using DSTATCOM," in Proc. IEEE Power Energy Soc. Gen. Meeting—Convers. Del. Elect. Energy 21st Century, Jul. 2008, pp. 1–6.
[9] M. Singh, V. Khadkikar, A. Chandra, and R. Varma, "Grid interconnection of renewable energy sources at the distribution level with power-quality improvement features," IEEE Trans. Power Del., vol. 26, no. 1, pp. 307–315, Jan. 2011.
[10] H.-G. Yeh, D. Gayme, and S. Low, "Adaptive VAR control for distribution circuits with photovoltaic generators," IEEE Trans. Power Syst., vol. 27, no. 3, pp. 1656–1663, Aug. 2012.
[11] C. Demoulias, "A new simple analytical method for calculating the optimum inverter size in grid-connected PV plants," Electr. Power Syst. Res., vol. 80, no. 10, pp. 1197–1204, 2010.
[12] R. Tonkoski, D. Turcotte, and T. H. M. EL-Fouly, "Impact of high PV penetration on voltage profiles in residential neighborhoods," IEEE Trans. Sustain. Energy, vol. 3, no. 3, pp. 518–527, Jul. 2012.
[13] X. Yu and A. Khambadkone, "Reliability analysis and cost optimization of parallel-inverter system," IEEE Trans. Ind. Electron., vol. 59, no. 10, pp. 3881–3889, Oct. 2012.
[14] M. K. Mishra and K. Karthikeyan, "Design and analysis of voltage source inverter for active compensators to compensate unbalanced and nonlinear loads," in Proc. IEEE Int. Power Eng. Conf., 2007, pp. 649–654.
[15] A. Ghosh and A. Joshi, "A new approach to load balancing and power factor correction in power distribution system," IEEE Trans. Power Del., vol. 15, no. 1, pp. 417–422, Jan. 2000.
[16] U. Rao, M. K. Mishra, and A. Ghosh, "Control strategies for load compensation using instantaneous symmetrical component theory under different supply voltages," IEEE Trans. Power Del., vol. 23, no. 4, pp. 2310–2317, Oct. 2008.
[17] P. Rodriguez et al., "A stationary reference frame grid synchronization system for three-phase grid-connected power converters under adverse grid conditions," IEEE Trans. Power Electron., vol. 27, no. 1, pp. 99–112, Jan. 2012.

Authors Details

Miss.Y DHANA LAKSHMI recieved the Bachelor of technology degree in Electrical and Electronics Engineering from JNTU K in 2011. Currently she is persuing M.Tech in Sri Sri Mittapalli college of Engineering, Tummalapalem, Guntur, A.P, INDIA,.Her Areas of interests are inPower systems,Power Electronic control .

SURESH.MIKKILI is working as Associate Professor in Sri Mittapalli College of Engineering Tummalapalem, Guntur; A.P. He is having 13 years of teaching experience. He received his B.Tech degree from Narasaraopeta Engineering College Narasaraopeta and M.Tech from National Institute of Technology NIT Warangal with Specialization of Power Electronics and Drives. Currently he is pursuing Ph.D in JNTU Anantapur Specialization in Hybrid Systems. His research interests include Renewable Energy Conversion Power Converters, and Multilevel Inverter.