International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

COPY RIGHT

IJIEMR Transactions, online available on 5th Febraury 2018. Link :
http://www.ijiemr.org/downloads.php?vol=Volume-7&issue=ISSUE-02

Title: Fuzzy Controlled Single Phase to 3 Phase Converter with Reduced Switch Count.

Volume 07, Issue 02, Page No: 41 – 53.

Paper Authors

*** Mrs.G.JAJI SUDHA, Mr.K. RAMESH BABU , Mr.Ch.RAMBABU.**

* Dept of EEE, Sri Vasavi Engineering College.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

To Secure Your Paper As Per UGC Guidelines We Are Providing A Electronic Bar Code

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

FUZZY CONTROLLED SINGLE PHASE TO 3 PHASE CONVERTER WITH REDUCED SWITCH COUNT

[1] Mrs.G.JAJI SUDHA, [2]Mr.K. RAMESH BABU , [3]Mr.Ch.RAMBABU
[1]PG Scholar, Department of Electrical & Electronics Engineering, Sri Vasavi Engineering College, Pedatadepalli, Tadepalligudem, West Godavari (Dt); A.P, India.
[2] Assistant Professor, Department of Electrical & Electronics Engineering, Sri Vasavi Engineering College, Pedatadepalli, Tadepalligudem, West Godavari (Dt); A.P, India.
[3]Ph.D,HOD, Department of Electrical & Electronics Engineering, Sri Vasavi Engineering College, Pedatadepalli, Tadepalligudem, West Godavari (Dt); A.P, India.

ABSTRACT-
In this project Fuzzy controlled single phase to 3 phase converter with reduced switch count is presented. A single-phase to three-phase drive system composed of two parallel single-phase rectifiers, a three-phase inverter, and an induction motor. Parallel converters can be used to improve the power capability, reliability, efficiency and redundancy. Parallel converter techniques can be employed to improve the performance of active power filters, uninterruptable power supplies, fault tolerance of doubly fed induction generators and three phase drives. The proposed topology permits to reduce the rectifier switch currents, the harmonic distortion at the input converter side, and presents to reduce the rectifier switch currents, the total harmonic distortion (THD). This paper addresses two topologies of power converter to 1ph-to-3th conversion system. Fuzzy logic controllers are the one to sense the output continuously and correct the output at the instant if any disturbance occurred. Even with the increase in the number switches, the total energy loss of the proposed system is lower than that of conventional system. The model of the system will be derived. A suitable control strategy and pulse width modulation technique (PWM) will be developed. The overall system performance is evaluated by using MATLAB/SIMULINK software.
Keywords- Key words-Ac-dc-ac power converter, Fuzzy logic controller, parallel Converter, Fault Identification System (FIS), Pulse Width Modulation Technique (PWM).

I. INTRODUCTION

Several solutions have been proposed when the objective is to supply a three-phase motor from single-phase ac mains. It is quite common to have only a single phase power grid in residential [1-2], commercial, manufacturing, and mainly in rural areas, while the adjustable speed drives may request a three-phase power grid. Single-phase to three-phase ac–dc–ac conversion usually employs a full-bridge topology, which implies in ten power switches. This converter is denoted here as conventional topology. Parallel converters have been used to improve the power capability, reliability, efficiency, and redundancy. Parallel converter techniques can be employed to improve the performance of active power filters, uninterruptible power supplies (UPS) [3], fault tolerance of doubly fed induction generators, and three-phase drives. Usually the operation of converters in parallel requires a transformer for isolation. However, weight, size, and cost associated with the transformer may make such a solution undesirable. When an isolation transformer is not used, the reduction of circulating currents among different converter stages is an important objective in the system design [4]. The 1phto-3ph converter based on a controlled rectifier is composed of five legs (ten controlled power devices), as shown in Fig. 1(a). It is denominated conventional 5L converter.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

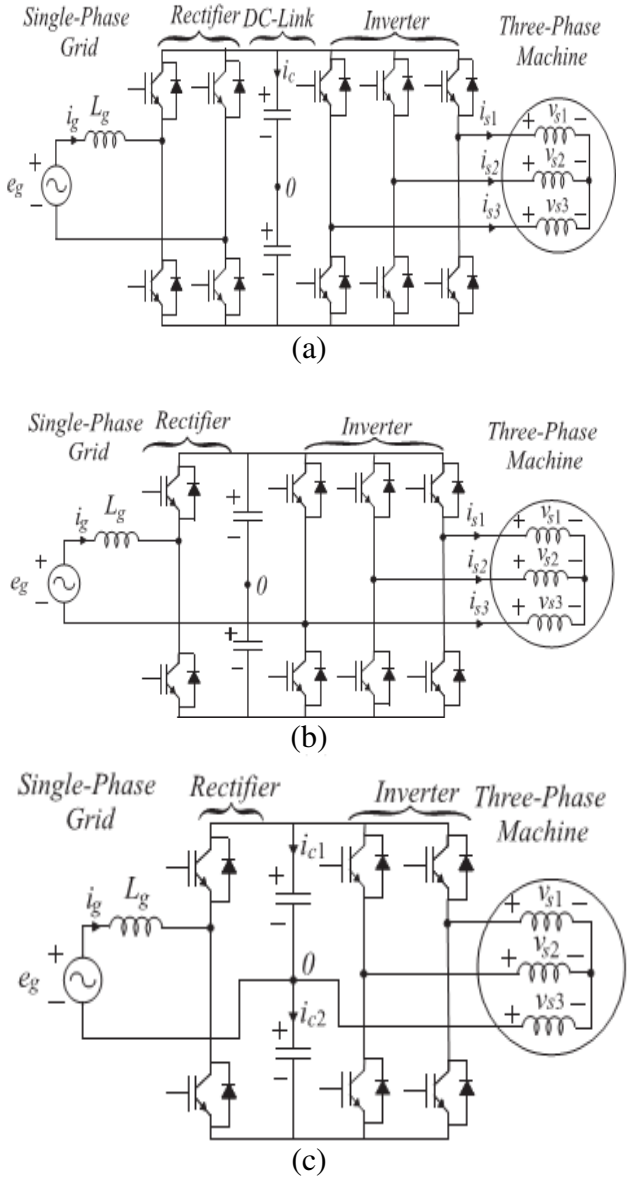


Fig.1.Conventional 1ph-to-3ph converter systems. (a) Five-leg (5L) converter. (b) Four-leg (4L) converter. (c) Three-leg (3L) converter.

Within that range of possibility, we can highlight the configurations with four legs (composed of a full-bridge rectifier and a three-leg inverter with a shared leg), denominated here conventional 4L converter [see Fig. 1(b)], and the configuration using three legs (composed of a half-bridge rectifier and two-leg inverter), denominated here conventional 3L converter [see Fig. 1(c)]. The 4L converter is proposed in [5-6].

The 4L converter uses less switches than the full-bridge 5L converter, but its dc-link voltage rating is equal to the 3L converter. For the 4L converter, using constant frequency output voltage and suitable control strategy, the dc-link voltage rating is the same as the conventional 5L counterpart [9]. The conventional 3L power converter uses only six power switches instead of ten of the conventional full-bridge 5L power converter. However, it increases the harmonic distortion of input current and twice of the dc-link voltage is required [7-8].

In this paper, a single-phase to three-phase drive system composed of two parallel single-phase rectifiers and a three-phase inverter is proposed. The proposed system is conceived to operate where the single-phase utility grid is the unique option available. Compared to the conventional topology, the proposed Fuzzy logic [9-10] system permits: to reduce the rectifier switch currents; the total harmonic distortion (THD) of the grid current with same switching frequency or the switching frequency with same THD [11] of the grid current by using fuzzy logic controller; and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart. The aforementioned benefits justify the initial investment of the proposed system, due to the increase of number of switches.

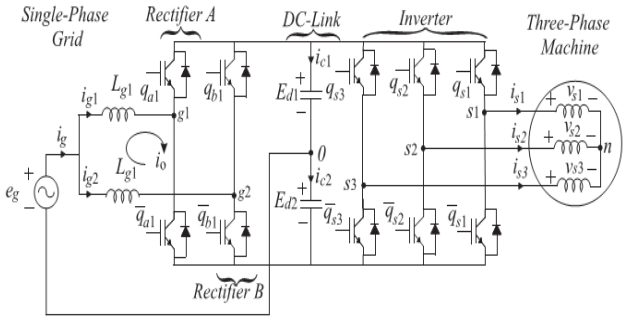
To overcome the conduction and switching losses generated by earlier converter designs, we propose a new modular fuzzy logic controller based converter design which increases the performance of system. The objective is to produce high-efficiency, voltage and current of a system with help of Fuzzy Logic Controller [12]. The requirement of continuous and controlled flow of voltage has met with the support of fuzzy logic controller

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

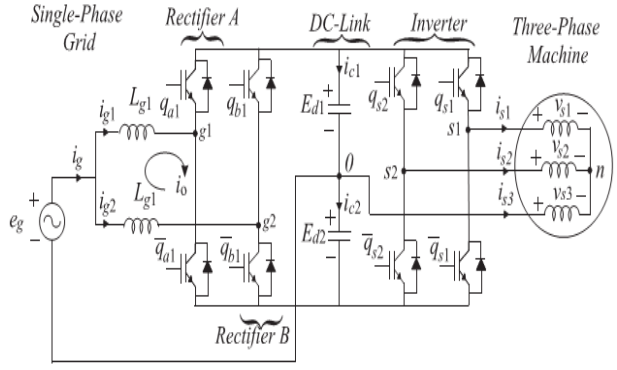
and the capacitors present with the schematic design which helps this requirement to be met in an efficient way. The conduction losses are reduced by using fuzzy logic controller in closed loop condition which reduces the switching losses and increases the output energy [13]. The proposed modular fuzzy logic controller based converter is implemented in MATLAB simulation platform and the output performance is analyzed.

II. SYSTEM MODEL

The P5L configuration presented in Fig.2 (a) is composed of two single-phase half-bridge rectifiers (rectifiers A and B), a dc-link, a three-phase inverter and a three-phase motor or a three-phase load. On the other hand, the P4L configuration [see Fig.2 (b)] is composed of a two-leg inverter instead three-leg inverter of the P5L converter.



(a)



(b)

Fig.2. Proposed 1ph-to-3ph converter using a half-bridge rectifier circuit (a) Parallel five-leg (P5L) converter, (b) Parallel four-leg (P4L) converter

A) Rectifier Model

From Fig.2, the following model is derived:

$$e_g = r_{g1} i_{g1} + l_{g1} \frac{di_{g1}}{dt} + v_{g10} \quad (1)$$

$$e_g = r_{g1} i_{g2} + l_{g1} \frac{di_{g2}}{dt} + v_{g20} \quad (2)$$

$$i_g = i_{g1} + i_{g2} \quad (3)$$

Where r_{g1} represents the resistance of the inductor filter L_{g1}, l_{g1} represents the inductance of the inductor filter L_{g1}, v_{g10}, and v_{g20} are the pole voltages of the rectifiers A and B, respectively, i_g is the grid current and i_{g1} and i_{g2} are the input currents of the rectifiers A and B, respectively.

The previous model can also be expressed by using the circulating current i_o introduced by

$$i_{g1} = \frac{i_g}{2} + i_o \quad (4)$$

$$i_{g2} = \frac{i_g}{2} - i_o \quad (5)$$

From (1) to (5), the complete system model is given by

$$e_g = \left(\frac{r_{g1}}{2}\right) i_g + \left(\frac{l_{g1}}{2}\right) \frac{di_g}{dt} + v_g \quad (6)$$

$$v_o = r_{g1} i_o + l_{g1} \frac{di_o}{dt} \quad (7)$$

With

$$i_o = \frac{i_{g1} - i_{g2}}{2} \quad (8)$$

$$v_g = \frac{v_{g10} + v_{g20}}{2} \quad (9)$$

$$v_o = \frac{-v_{g10} + v_{g20}}{2}. \quad (10)$$

From (6) to (10), it is clear that the grid and circulating currents depend on the voltages v_g and v_o, respectively. Then, the rectifier pole voltages can be calculated from desired

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

voltages (v_g and v_o) to control these currents. Considering circulating current null and the equivalent inductor $L_g = L_{g1}/2$ equal to that of the conventional converter, the front-end model of the configurations presented in Fig.2 is identical to that of the conventional 5L converter.

B) Inverter Model

The inverter model for the P5L configuration is given by

$$v_{s1} = v_{s10} - v_{n0} \quad (11)$$

$$v_{s2} = v_{s20} - v_{n0} \quad (12)$$

$$v_{s3} = v_{s30} - v_{n0} \quad (13)$$

Where v_{s10}, v_{s20}, and v_{s30} are the pole voltages of the inverter, v_{s1}, v_{s2}, and v_{s3} are the voltages of the three-phase load, and v_{n0} is the voltage between the point n and the dc-link midpoint 0. While the model of inverter of the P4L configuration is given by

$$v_{s13} = v_{s10} \quad (14)$$

$$v_{s23} = v_{s20} \quad (15)$$

Where v_{s13} and v_{s23} are line voltages of the three-phase load.

III. CONTROL STRATEGY

The control system of the proposed converters has the same objectives of the conventional one, i.e., dc-link voltage and power factor control from rectifier circuit and load voltage control from inverter circuit. Additionally, the proposed control system needs to regulate the circulating current between the parallel half-bridge rectifiers. Fig.3 shows the control block diagram of the P5L and P4L converters proposed in this paper. The capacitor dc-link voltage E_d (E_{d1} + E_{d2}) is adjusted to its reference value utilizing a proportional integral (PI) type controller. This controller provides the amplitude of the reference grid current. To control power factor and harmonics at the grid side, the instantaneous reference grid current must be synchronized with the grid voltage e_g based on phase locked loop scheme. Control of the grid current is implemented using a synchronous controller (a resonant controller type) described. The block R_g represents this controller. It defines the reference grid voltage.

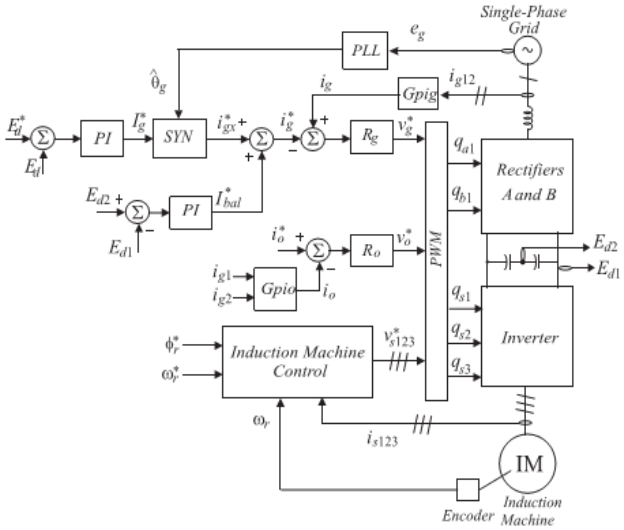


Fig.3. Control block diagram used for configurations P5L and P4L.

The circulating current (i_o) is obtained by block G_{pio} from the measured rectifiers currents i_{g1} and i_{g2}. This block is based on (8). The circulating current is compared to its reference (= 0). The error is the input of a synchronous controller (R_o), and gives in its output the voltage. Due to different dead-time switches, non-sinusoidal grid voltage or different capacitance, the voltage balance between the split capacitors obtained naturally may not be satisfactory. Some works have proposed solutions to voltage balance between the split capacitors of the half-bridge rectifier. One way to minimize the voltage imbalance between split capacitors is to add a current balance value in the reference grid current. The difference in voltage between the split capacitors (Ed1−Ed2) is input of the conventional PI controller. This controller provides the reference current balance value (). The reference grid current is achieved by adding with (i∗g = +), as discussed. The voltage balance between the split capacitors is

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

carried out, but it is necessary to apply a small distortion in the reference grid current. When a three-phase motor is used, control can be performed by the field-oriented control (FOC) technique as shown or volt/hertz control.

IV. PWM STRATEGY

The PWM methods can be based on classic sinusoidal modulation, scalar as well as on vector modulation approach. In sinusoidal modulation, the gating signals are obtained by comparing reference pole voltages with a triangular carrier signal. In this paper, the PWM strategy for the rectifiers A and B will be based on sinusoidal modulation. The gating signals are obtained by comparing reference pole voltages with one or two high-frequency triangular carrier signals, i.e., a single or double carriers PWM implementation. In the case of double carrier approach (interleaved technique), the phase shift of the two triangular carrier signals is 180^0. The reference pole voltages of the rectifiers are obtained as follows.

Considering that and are the reference voltages determined by the current controllers, from (9) and (10), we found

$$v_g^* = \frac{v_{g10}^* + v_{g20}^*}{2} \tag{16}$$

$$v_o^* = \frac{-v_{g10}^* + v_{g20}^*}{2}. \tag{17}$$

Writing (16) and (17) in matrix form

$$\begin{bmatrix} v_g^* \\ v_o^* \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} v_{g10}^* \\ v_{g20}^* \end{bmatrix} \tag{18}$$

The gating signals are directly calculated from the reference pole voltages (and), solving (18), we obtain

$$v_{g10}^* = v_g^* - v_o^* \tag{19}$$

$$v_{g20}^* = v_g^* + v_o^*. \tag{20}$$

Suitable modulation is obtained when $-/2 \leq \leq /2$ and $- /2 \leq \leq /2$. Where is the reference dc-link voltage with = +. The three-phase inverter (P5L configuration) can be commanded by using an adequate PWM strategy for the three-phase voltage source inverter. While for the two-leg inverter (P4L converter), the PWM can be obtained with a similar technique presented.

V. DC- LINK CAPACITOR

A) DC-Link Capacitor Voltage

Considering that all the voltages are purely sinusoidal, the voltage limits conditions of each configuration. Where V_g represents the amplitude of rectifier voltage, whereas V_s denotes the amplitude of the load phase voltage. If the input voltage is equal to output voltage (i.e., $V_g = V_s$), the conventional 5L converter has the best dc-link voltage rating. The proposed P5L converter has the dc-link voltage 15% bigger than the conventional 5L one. While conventional 3L and proposed P4L converters require twice the dc-link voltage of the conventional 5L one.

On the other hand, when the output voltage is double the input voltage (i.e., $V_s = 2V_g$), the proposed P5L converter can operate with the same dc-link voltage of the conventional 5L converter.

B) DC-Link Capacitor Current

From Fig.2 (a), the dc-link capacitor current for the P5L converter can be given by

$$i_{c1} = \sum_{k=1}^{2} \frac{\tau_{gk}}{T_s} i_{gk} - \sum_{j=1}^{3} \frac{\tau_{sj}}{T_s} i_{sj} \tag{21}$$

$$i_{c2} = -\sum_{k=1}^{2} \left(1 - \frac{\tau_{gk}}{T_s}\right) i_{gk} + \sum_{j=1}^{3} \left(1 - \frac{\tau_{sj}}{T_s}\right) i_{sj} \tag{22}$$

Where τ_{gk} and τ_{sj} are the time intervals in which switches q_{gk} and q_{sj} are closed (with k = 1, 2 and j = 1, 2, 3), respectively, and T_s is the sampling time. Assuming that the reference pole voltages are constant over T_s, the time intervals τ_{gk} and τ_{sj} can be written as a function

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

of the reference pole voltages. For instance, τ_{gk} is given by

$$\tau_{gk} = \left(\frac{v^*_{gk0}}{E^*_d} + \frac{1}{2} \right) T_s \tag{23}$$

Thus, from (21)–(23), the dc-link capacitor current is given by

$$i_{c1} = \frac{i_g}{2} + \sum_{k=1}^{2} \frac{v^*_{gk0}}{E^*_d} i_{gk} - \sum_{j=1}^{3} \frac{v^*_{sj0}}{E^*_d} i_{sj} \tag{24}$$

$$i_{c2} = -\frac{i_g}{2} + \sum_{k=1}^{2} \frac{v^*_{gk0}}{E^*_d} i_{gk} - \sum_{j=1}^{3} \frac{v^*_{sj0}}{E^*_d} i_{sj} \tag{25}$$

If the reference pole voltages are defined by (19) and (20) and the rectifier currents by (4) and (5), then the capacitor currents i_{c1} and i_{c2} can be written as follows:

$$i_{c1} = \frac{i_g}{2} + \frac{v^*_g}{E^*_d} i_g - \frac{2v^*_o}{E^*_d} i_o - \sum_{j=1}^{3} \frac{v^*_{sj}}{E^*_d} i_{sj} \tag{26}$$

$$i_{c2} = -\frac{i_g}{2} + \frac{v^*_g}{E^*_d} i_g - \frac{2v^*_o}{E^*_d} i_o - \sum_{j=1}^{3} \frac{v^*_{sj}}{E^*_d} i_{sj} \tag{27}$$

The first component of the capacitor currents, for the P5L converter, is due to the grid connection at the midpoint of the dc-link, the second component is due to the single-phase voltage source, with twice of the grid frequency. The third component is a consequence of the circulating current. Although there is no low-frequency circulating current (eliminated by the controller), it may exist with high-frequency circulating current due to the interleaving technique. The last term is due to the three-phase inverter. A similar analysis may be obtained with the P4L converter, but in this case, there is a load current component (i_{s3}) due to the load connection at the midpoint dc-link, as shown in the following equations:

$$i_{c1} = \frac{i_g}{2} + \frac{i_{s3}}{2} + \frac{v^*_g}{E^*_d} i_g - \frac{2v^*_o}{E^*_d} i_o - \sum_{j=1}^{2} \frac{v^*_{sj0}}{E^*_d} i_{sj} \tag{28}$$

$$i_{c2} = -\frac{i_g}{2} - \frac{i_{s3}}{2} + \frac{v^*_g}{E^*_d} i_g - \frac{2v^*_o}{E^*_d} i_o - \sum_{j=1}^{2} \frac{v^*_{sj0}}{E^*_d} i_{sj} \tag{29}$$

Another common feature among the studied configurations is a component in frequency of 120 Hz due to a single-phase power supply. Moreover, the proposed configurations have a reduction at high-frequency components in capacitor currents, especially when double-carrier PWM is applied. For instance, the RMS capacitor current of the P5L converter (with interleaved technique) decreases by33%compared to the conventional 5L converter.

VI. HARMONIC DISTORTION

In this paper, the weighted total harmonic distortion factor (WTHD) has been used to evaluate the distortion of the converter voltage, because it is superior to the total harmonic distortion factor to measure the quality of a non-sinusoidal waveform. The WTHD is defined by

$$\text{WTHD} = \frac{\sqrt{\sum_{h=2}^{N_h} \left(\frac{V_h}{h} \right)^2}}{V_1} \tag{30}$$

Where V_1 is the amplitude of the fundamental voltage component, V_h is the amplitude of hth component voltage harmonic, and N_h is the number of harmonics taken into consideration.

VII. CONVERTER LOSSES

Several studies have been performed in order to determine the power losses in the power switches (IGBTs and MOSFETs). Two solutions are generally applied: 1) the experimental measurement of power loss, with the aim of constructing mathematical functions from a regression model and 2) determining losses using linear IGBT and diode models. In this paper, the losses estimation is obtained through of the regression model, which has been achieved by experimental tests. The tests were performed for different values of currents and temperatures. All data of losses have been

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

employed to obtain the regression model, as presented. Such a regression model provides polynomial equations for the losses.

The instantaneous losses function of an IGBT dual module CM50DY-24H manufactured by POWEREX driven by driver SKHI-10 manufactured by SEMIKRON was determined. Then, digital simulation provided by PSIM simulation software was used to calculate the power losses in converters. The polynomial equations were implemented using a DLL (dynamic-link library) written in C (programming language).

VIII. FUZZY LOGIC CONTROLLER

A)Fuzzification:

The first step in the design of a fuzzy logic controller is to define membership functions for the inputs. Seven fuzzy levels or sets are chosen and defined by the following library of fuzzy-set values for the error e and change in error. They are as follows

- NB negative big
- NM negative medium
- NS negative small
- ZE zero equal
- PS positive small
- PM positive medium
- PB positive big

❖ The number of fuzzy levels is not fixed and depends on the input resolution needed in an application.

❖ The larger the number of fuzzy levels, the higher is the input resolution.

❖ The fuzzy controller utilizes triangular membership functions on the controller input. The triangular membership function is chosen due to its simplicity. For a given crisp input, fuzzifier finds the degree of membership in every linguistic variable.

❖ Since there are only two overlapping memberships in this specific case, all linguistic variables except two will have zero membership.

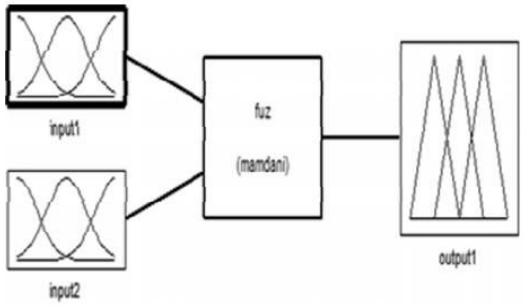


Fig.4.Block diagram of the Fuzzy Logic Controller (FLC) for proposed converter.

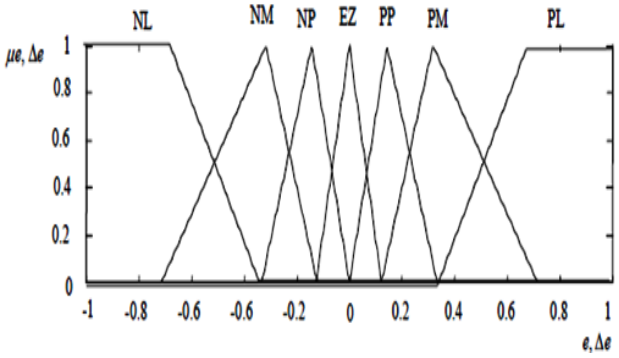


Fig.5. Membership functions for Input, Change in input, Output.

Rule Base: the elements of this rule base table are determined based on the theory that in the transient state, large errors need coarse control, which requires coarse in-put/output variables; in the steady state, small errors need fine control, which requires fine input/output variables. Based on this the elements of the rule table are obtained as shown in Table 1, with 'Vdc' and 'Vdc-ref' as inputs.

• When the output of the converter is far from the set point, the change of duty cycle must be large so as to bring the output to the set point quickly.

• When the output of the converter is approaching the set point, a small change of duty cycle is necessary.

• When the output of the converter is near the set point and is approaching it rapidly, the duty cycle must be kept constant so as to prevent overshoot.

• When the set point is reached and the output is still changing, the duty cycle must be

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

changed a little bit to prevent the output from moving away.

• When the set point is reached and the output is steady, the duty cycle remains unchanged. When the output is above the set point, the sign of the change of duty cycle must be negative, and vice versa.

TABLE 1: Rules for Fuzzy System

Δe \ e	NL	NM	NS	EZ	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	EZ
NM	NL	NL	NL	NM	NS	EZ	PS
NS	NL	NL	NM	NS	EZ	PS	PM
EZ	NL	NM	NS	EZ	PS	PM	PL
PS	NM	NS	EZ	PS	PM	PL	PL
PM	NS	EZ	PS	PM	PL	PL	PL
PL	NL	NM	NS	EZ	PS	PM	PL

IX. MATLAB/SIMULINK RESULTS

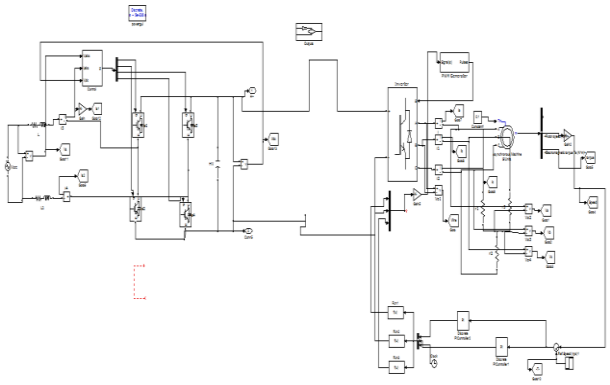


Fig.6 MATLAB/SIMULINK circuit for 1ph-to-3ph converter using a half-bridge rectifier with Parallel five-leg converter

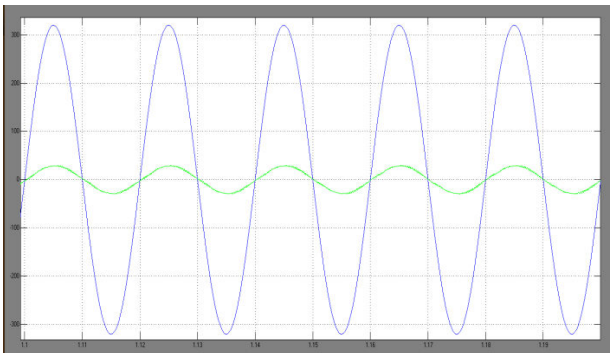


Fig.7 Voltage and current output waveform

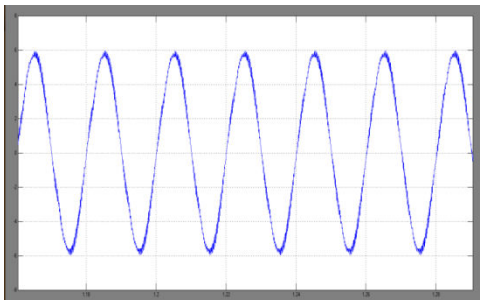


Fig.8 Output waveform of Rectifier Input Current i_{g1}

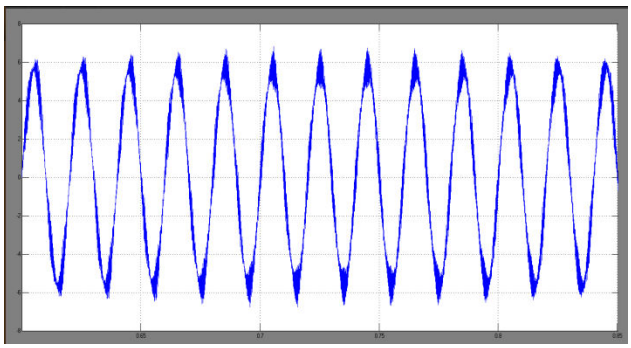


Fig.9 Output waveform of Rectifier Input Current i_{g2}

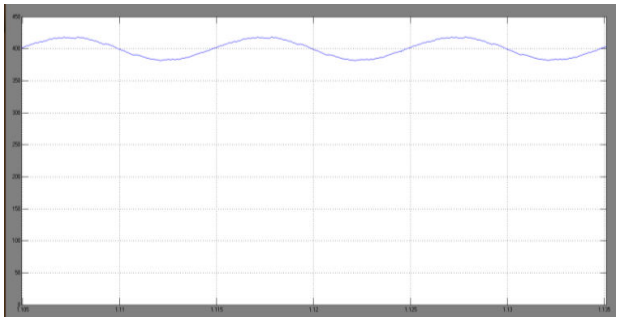


Fig.10 Dc-link total output voltage

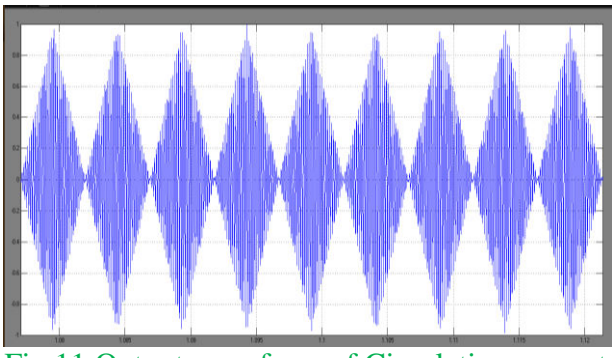


Fig.11 Output waveform of Circulating current

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

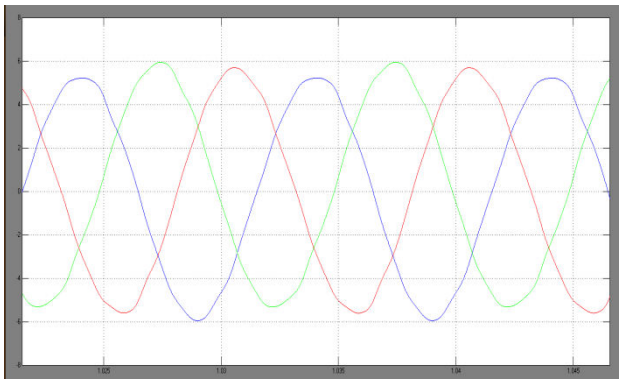


Fig.12 Output waveform of Load currents $i_{S1,}$ i_{S2} and i_{S3}

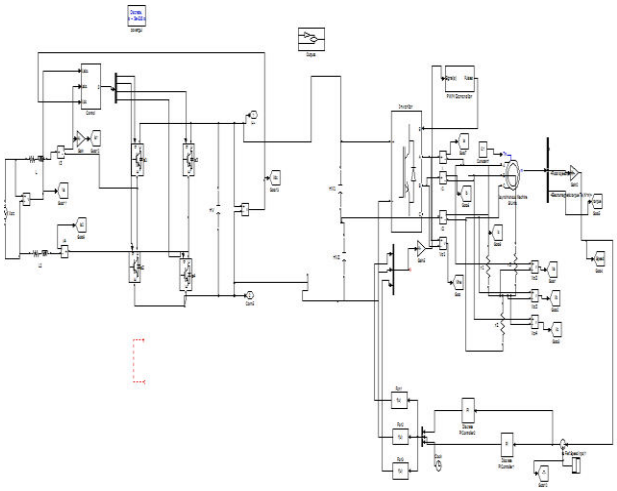


Fig.13 MATLAB/SIMULINK circuit for 1ph-to-3ph converter using a half-bridge rectifier with Parallel four-leg converter

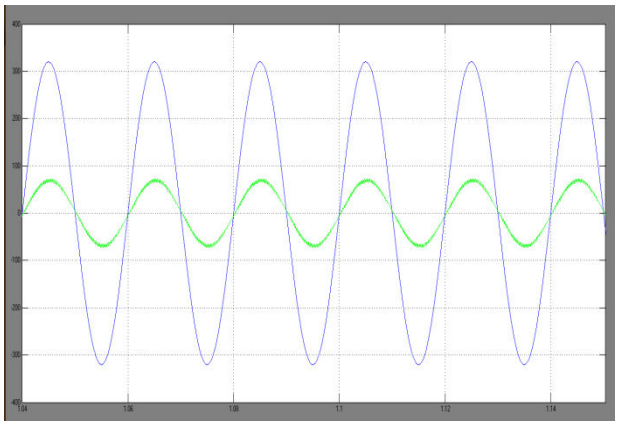


Fig.14 Output waveform of Voltage and Current

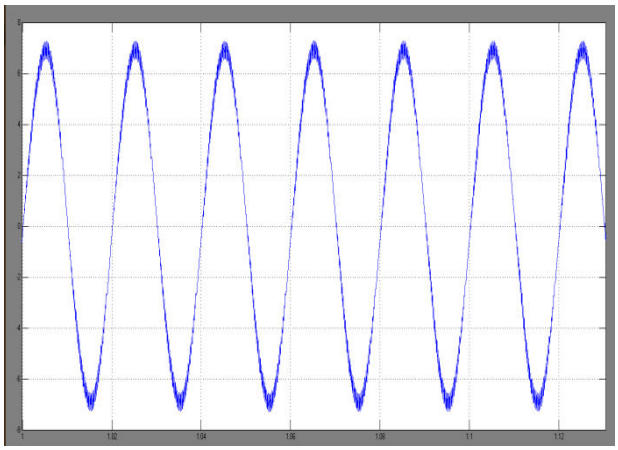


Fig.15 Output waveform of Rectifier Input Current i_{g1}

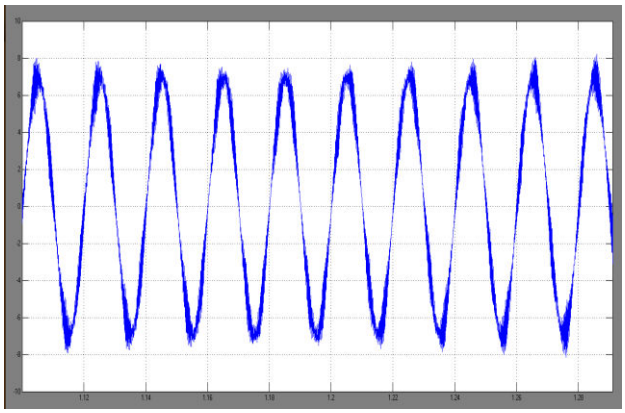


Fig.16 Output waveform of Rectifier Input Current i_{g2}

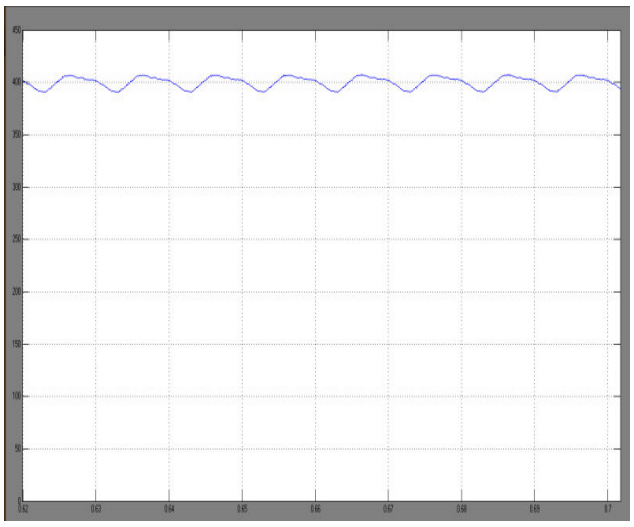


Fig.17 Dc-link total output voltage

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

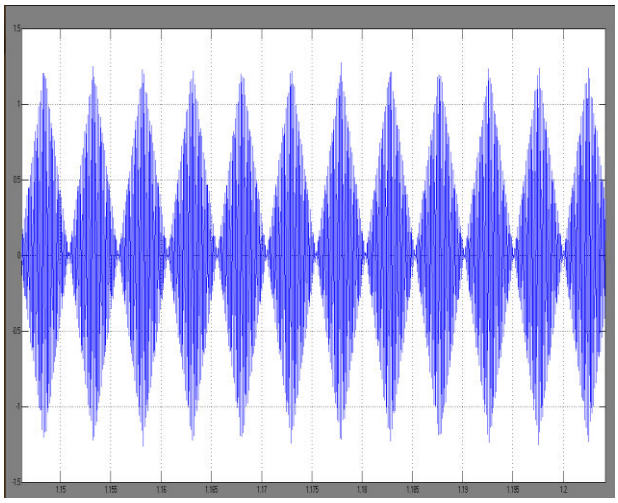


Fig.18 Output waveform of Circulating current

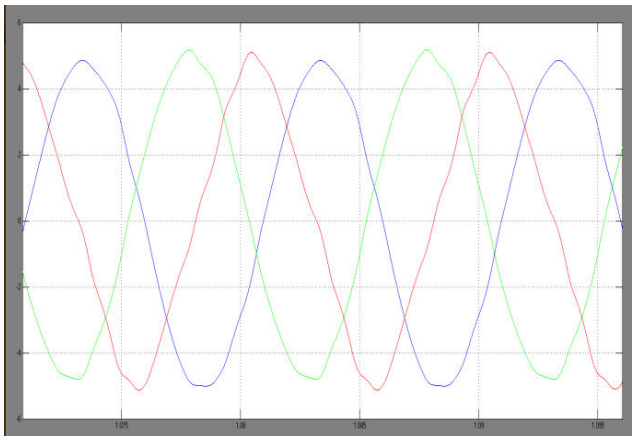


Fig.19 Output waveform of Load currents $i_{S1,}$ i_{S2} and i_{S3}

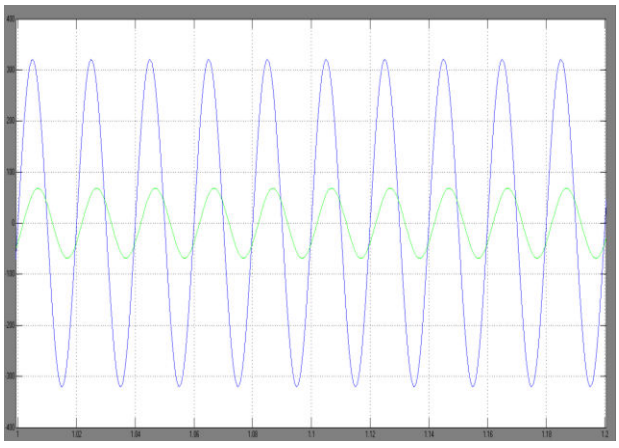


Fig.20 Output waveform of Voltage and Current

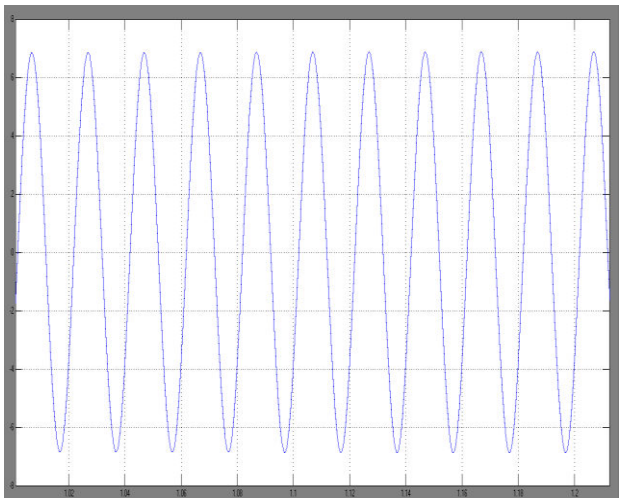


Fig.21 Output waveform of Rectifier Input Current i_{g1}

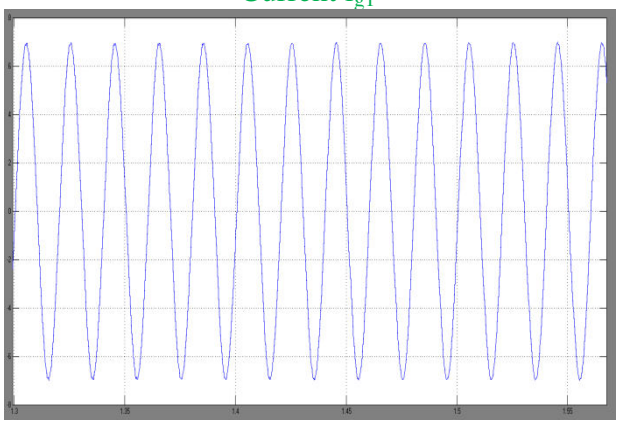


Fig.22 Output waveform of Rectifier Input Current i_{g2}

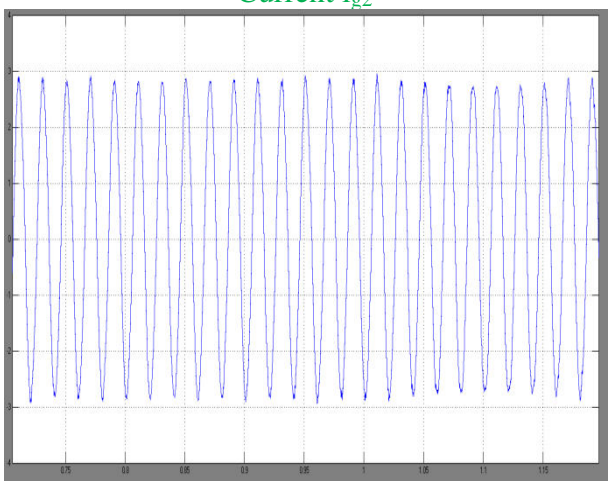


Fig.23 Output waveform of Circulating current

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

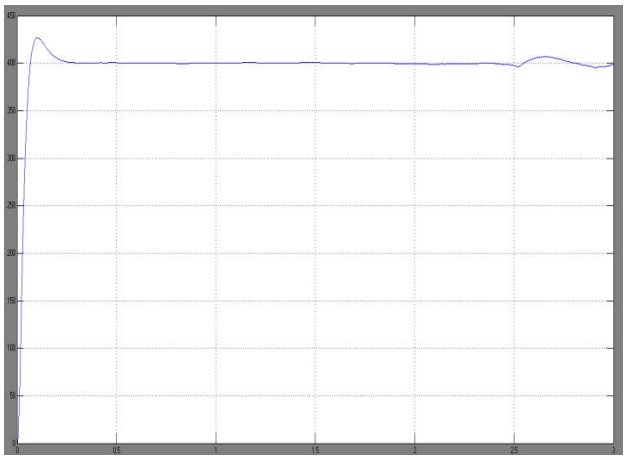


Fig.24 Output waveform of DC-link voltage

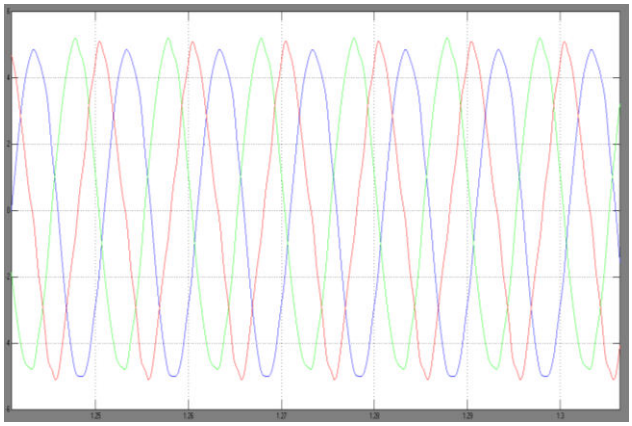


Fig.25 Output waveform of Load currents i_{S1}, i_{S2} and i_{S3}

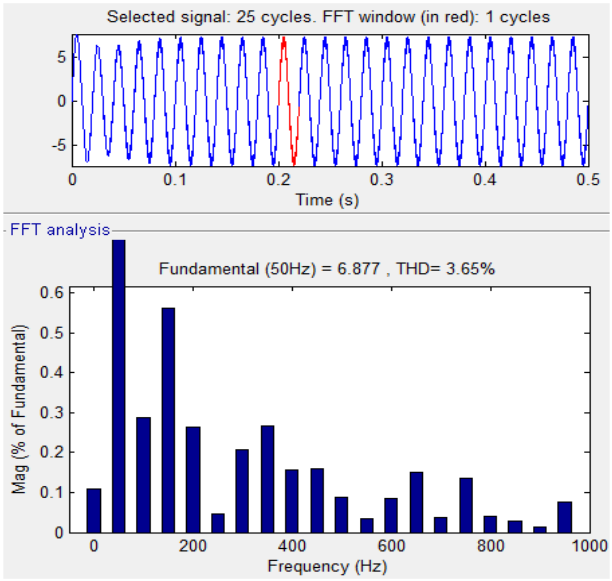


Fig.26 THD plot of i_{S1} by using PI controller

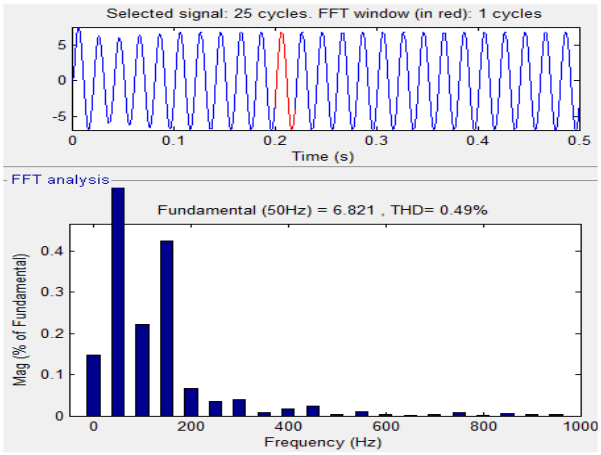


Fig.27 THD plot of i_{S1} by using Fuzzy controller

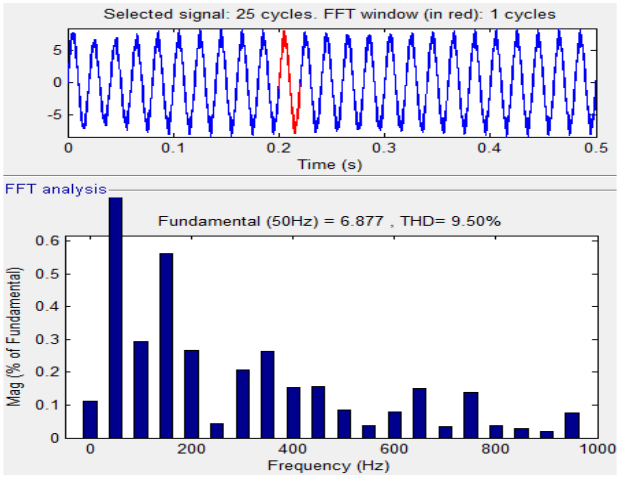


Fig.28 THD plot of i_{S2} by using PI controller

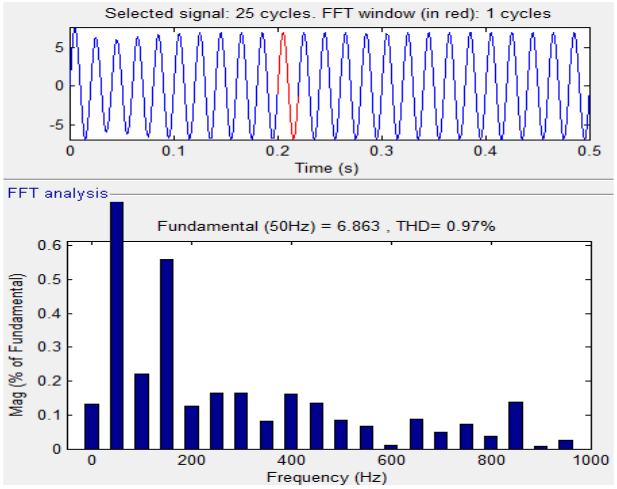


Fig.28 THD plot of i_{S2} by using Fuzzy controller

X. CONCLUSION

The proposed Fuzzy Controlled Single Phase to 3 Phase Converter with Reduced Switch Count was simulated with MATLAB / SIMULINK software. In the proposed model the switching losses are reduced with the help of fuzzy logic controller and conduction losses are reduced by adapting the switch as auxiliary circuit. The proposed design has produced very good results and the output voltage and current produced are high. The efficiency produced by the fuzzy based converter design has been evaluated for various input and output values of voltage and current output. The system combines two parallel rectifiers without the use of transformers. The system model and the control strategy, including the PWM technique, have been developed. The proposed system permits to reduce the rectifier switch currents, the THD of the current and to increase the fault tolerance characteristics.

REFERENCES

[1] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems—An overview," in Proc. IEEE Int. Symp. Ind. Electron., 1998, vol. 1, pp. 224–229.

[2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid connected inverters for photovoltaic modules," IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[3] P. K. Hinga, T. Ohnishi, and T. Suzuki, "A new PWM inverter for photovoltaic power generation system," in Conf. Rec. IEEE Power Electron. Spec. Conf., 1994, pp. 391–395.

[4] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

[5] M. Saeedifard, R. Iravani, and J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 452–466, Feb. 2009.

[6] P.-T. Cheng, C.-C. Hou, and J.-S. Li, "Design of an auxiliary converter for the diode rectifier and the analysis of the circulating current," IEEE Trans. Power Electron., vol. 23, no. 4, pp.1658–1667, Jul. 2008.

[7] H. Cai, R. Zhao, and H. Yang, "Study on ideal operation status of parallel inverters," IEEE Trans. Power Electron., vol. 23, no. 6, pp.2964–2969, Nov. 2008.

[8] P. Enjeti and A. Rahman, "A new single phase to three phase converter with active input current shaping for low cost AC motor drives," IEEE Trans. Ind. Appl., vol. 29, no. 2, pp. 806–813, Jul./Aug. 1993.

[9] J. Itoh and K. Fujita, "Novel unity power factor circuits using zero-vector control for single-phase input systems," IEEE Trans. Power Electron., vol. 15, no. 1, pp. 36–43, Jan. 2000.

[10] B. K. Lee, B. Fahimi, and M. Ehsani, "Overview of reduced parts converter topologies for AC motor drives," in Proc. IEEE PESC, 2001, pp. 2019– 2024.

[11] R. Q. Machado, S. Buso, and J. A. Pomilio, "A line-interactive single-phase to three-phase converter system," IEEE Trans. Power Electron., vol. 21, no. 6, pp. 1628–1636, May 2006.

[12] M. N. Uddin, T. S. Radwan, and M. A.Rahman, "Fuzzy-logic-controller-based cost-effective four-switch three-phase inverter-fed motor drive system," IEEE Trans. Ind. Appl., vol. 42, no. 1,21–30, Jan./Feb. 2006.

[13] J. Holtz, "Pulse width modulation for electronic power conversion," Proc. IEEE, vol. 82, no.8, pp. 1194–1214, Aug. 1994.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

BIBLIOGRAPHY

Mrs G.JAJI SUDHA recieved the Bachelor of technology degree in Electrical and Electronics Engineering from JNTU in 2012. Currently she is persuing M.Tech in Sri Vasavi Engineering college,Tadepalligudem,A.P.Her Areas of interests are inPower systems,Power Electronic control .

Mr K.RAMESH BABU recieved the Bachelor of technology degree in Electrical and Electronics Engineering from JNTU in 2007. He received M.Tech degree from JNTU in 2010. He Working as a Assistant Professor in Sri Vasavi Engineering college,Tadepalligudem,A.P.His Areas of interests are inPower systems,Power Electronic control of drives.

Mr Ch.RAMBABU recieved the Bachelor of technology degree in Electrical and Electronics Engineering from Madras Univercity in 2000. He received M.Tech degree from JNTU Anantapur in 2005.He is a research student of JNTU Kakinada.He Working as a Associate Professor at Sri Vasavi Engineering college,Tadepalligudem,A.P.His Areas of interests are inPower systems control,Power Electronics and FACTS.