International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

IJIEMR Transactions, online available on 21th January 2018. Link :
http://www.ijiemr.org/downloads.php?vol=Volume-7&issue=ISSUE-01

Title: Implementation of Redundant Binary Partial Product for Multiplier to Optimize the Power.

Volume 07, Issue 01, Page No: 134 – 141.

Paper Authors

*** A.NAVEEN KUMAR, B.NAGAVENI.**

* Ashoka Institute of Engineering and Technology.

USE THIS BARCODE TO ACCESS YOUR ONLINE PAPER

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

IMPLEMENTATION OF REDUNDANT BINARY PARTIAL PRODUCT FOR MULTIPLIER TO OPTIMIZE THE POWER

***A.NAVEEN KUMAR, **B.NAGAVENI**
*PG Scholar(Vlsi), Ashoka Institute of Engineering and Technology
**Assistant Professor(Vlsi), Ashoka Institute of Engineering and Technology

ABSTRACT:
Adders are the key element of the arithmetic unit, especially fast parallel adder. Redundant Binary Signed Digit (RBSD) adders are designed to perform high-speed arithmetic operations. Generally, in a high radix modified Booth encoding algorithm the partial products are reduced in multiplication process. Due to its high modularity and carry-free addition, a redundant binary (RB) representation can be used when designing high performance multipliers. The conventional RB multiplier re-quires an additional RB partial product (RBPP) row, because an error-correcting word (ECW) is generated by both the radix-4 Modified Booth encoding (MBE) and the RB encoding. This incurs in an additional RBPP accumulation stage for the MBE multiplier. In this paper, a new RB modified partial product generator (RBMPPG) is proposed; it removes the extra ECW and hence, it saves one RBPP accumulation stage. Therefore, the proposed RBMPPG generates fewer partial product rows than a conventional RB MBE multiplier. Simulation results show that the proposed RBMPPG based designs significantly improve the area and power consumption when the word length of each operand in the multiplier is at least 32 bits.

Key Words: Redundant binary, modified Booth encoding, RB partial product generator, RB multiplier.

I. INTRODUCTION

The digital multiplier is a ubiquitous arithmetic unit in microprocessors, digital signal processors, and emerging media processors. It is also a kernel operator in application- specific data path of video and audio codes, digital filters, computer graphics, and embedded systems. Compared with many other arithmetic operations, multiplication is time-consuming and power hungry. The critical paths dominated by digital multipliers often impose a speed limit on the entire design. Hence, VLSI design of high-speed multipliers, with low energy dissipation, is still a popular research subject. Redundant binary (RB) representation is one of the signed digit representations first introduced by Avizienis [9] in 1961 for fast parallel arithmetic.Many algorithms and architectures have been proposed to design high-speed and low-power multipliers [1-13]. A normal binary (NB) multiplication by digital circuits includes three steps. In the first step, partial products are generated; in the second step, all partial products are added by a partial product

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

reduction tree until two partial product rows remain.

In the third step, the two partial product rows are added by a fast carry propagation adder. Two methods have been used to perform the second step for the partial product reduction. A first method uses 4-2 compressors, while a second method uses redundant binary (RB) numbers [5-6]. Both methods allow the partial product reduction treeto be reduced at a rate of 2:1. The RB addition is carry-free, making it a promising substitute for two's complement multi-operand addition in a tree-structured multiplier. Similar to a normal binary (NB) multiplier, an RB multiplier is anatomized into three stages and consists of four modules: the Booth encoder, RB partial product generator (also known as decoder), RB partial product accumulator, and RB-to-NB converter.A Radix-4 Booth encoding or a modified Booth encoding (MBE) is usually used in the partial product generator of parallel multipliers to reduce the number of partial product rows by half [5-6] [10-13].

A RBPP row can be obtained from two adjacent NB partial product rows by inverting one of the pair rows [5-6]; an N-bit convention-al RB MBE (CRBBE-2) multiplier requires **N**/4 RBPP rows. An additional error-correcting word (ECW) is also required by both the RB and the Booth encoding [5-6] [14]; therefore, the number of RBPP accumulation stages (NRBPPAS) required by a power-of-two word-length (i.e., 2 -bit) multiplier is given by:
NRBPPAS = log (N /4 + 1)
= n − 1, if N = 2^n

This paper focuses on the RBPP generator for designing a 2 -bit RB multiplier with fewer partial product rows by eliminating the extra ECW. A new RB modified partial product generator based on MBE (RBMPPG-2) is proposed. In the proposed RBMPPG-2, the ECW of each row is moved to its next neighbor row. Furthermore, the extra ECW generated by the last partial product row is combined with both the two most significant bits (MSBs) of the first partial product row and the two least significant bits (LSBs) of the last partial product row by logic simplification.

Therefore, the proposed method reduces the number of RBPProws from **N** /4 + 1to **N** /4, i.e., a RBPP accumulation stage is saved. The proposed method is applied to 8×8-bit, 16×16-bit, 32×32-bit, and 64×64-bit RB multiplier designs; the designs are synthesized using the NanGate 45nm Open Cell Library. The proposed designs achieve significant reductions in area and power consumption compared with existing multipliers when the word length of each of the operands is at least 32 bits.

II. RELATED WORK

A high-radix Booth encoding technique can reduce the number of partial products. However, the number of expensive hard multiples (i.e., a multiple that is not a power of two and the operation cannot be per-formed by simple shifting and/or complementation) increases too [14-16]. Besli et al. [16] noticed that some hard multiples can be obtained by the differences of two sim-ple power-of-two multiplies. A new radix-16 Booth en-coding (RBBE-4) technique without ECW has been pro-posed in [14]; it avoids the issue of hard

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

multiples. A radix-16 RB Booth encoder can be used to overcome the hard multiple problem and avoid the extra ECW, but at the cost of doubling the number of RBPP rows.

Therefore, the number of radix-16 RBPP rows is the same as in the radix-4 MBE. However, the RBPP generator based on a radix-16 Booth encoding has a complex circuit structure and a lower speed compared with the MBE partial product generator [10] when requiring the same number of partial products

II. BLOCK DIAGRAM

The aim of this study is implementation of modified partial product generator for RB multipliers.

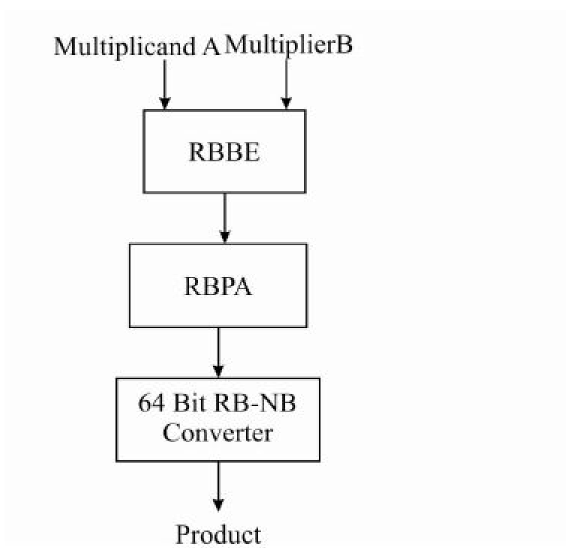


Fig.1.block diagram

A RB multiplier consists of a RB partial product (RBPP) generator, a RBPP reduction tree and a RB-NB converter. A Radix-4 Booth encoding or a modified Booth encoding (MBE) is usually used in the partial product generator of parallel multipliers to reduce the number of partial product rows by half [5-6] [10-13]. A RBPP row can be obtained from two adjacent NB partial product rows by inverting one of the pair rows.

2.1 RADIX -4 BOOTH ENCODING

Booth encoding has been proposed to facilitate the multiplication of two's complement binary numbers [17]. It was revised as modified Booth encoding (MBE) or radix-4 Booth encoding [18].The MBE scheme explained in the table, where A = aN-1 a N-2 …..a 2 a 1 a 0stands for the multiplicand, and B =b N-1 b N-2 ….b 2 b 1 b 0 stands the multiplier bits .The multiplier bits are grouped in set of three adjacent bits. The two side bits are overlapped with neighboring groups except the first multiplier bits group in which it is {b1, b0, 0}. Each group is decoded by selecting the partial product shown in Table I, where 2Aindicates twice the multiplicand, which can be obtained by left shifting. Negation operation is achieved by inverting each bit of A and adding ‘1’ (defined as correction bit) to the LSB [10-13].

TABLE I

MBE SCHEME

$b_{2i+1}, b_{2i}, b_{2i-1}$	Operation
000	0
001	$+A$
010	$+A$
011	$+2A$
100	$-2A$
101	$-A$
110	$-A$
111	0

1.2 RB PARTIAL PRODUCT GENERATOR

As two bits are used to represent one RB digit, then a RBPP is generated from two NB partial

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

products [1-6]. The addition of two N-bit NB partial products X and Y using two's complement representation can be expressed as follows

X +Y = X –Y -1

= (X ,Y-) -1

Where Y- is the inverse of Y.The RBPP is generated by inverting one of the two NB partial products and adding -1 to the LSB.. Each RB digit X ibelongs to the set{-1,0,1};this is coded by two bits (X i-, X i+) .RB numbers can be coded in several ways.Table 11 shows one specific RB encoding

TABLE II

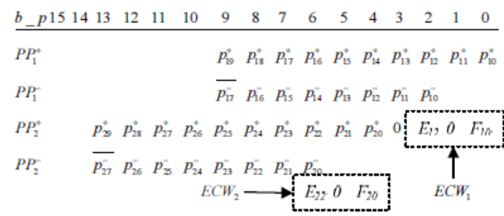
RB ENCODING USED IN THIS WORK [6]

X_i^+	X_i^-	RB digit (X_i)
0	0	0
0	1	$\bar{1}$
1	0	1
1	1	0

Both MBE and RB coding schemes introduce errors and two correction terms are required: 1) when the NB number is converted to a RB format, -1 must beaddedto the LSB of the RB number; 2) when the multiplicand is multiplied by -1 or -2 during the Booth encoding, the number is inverted and +1 must be added to the LSB of the partial product. A single ECW can compensate errors from both the RB encoding and the radix-4 Booth recoding.

2.2.1PROPOSED RB PARTIAL PRODUCT GENERATOR

A new RB modified partial product generator based on MBE (RBMPPG-2) is presented in this section; in this design, ECW is eliminated by incorporating it into both the two MSBs of the first partial product row (PP 1+) andthe two LSBs of the last partial product row (PP –(N/4)).



(a)

Fig.2(a)The first new RBMPPG-2 architecture for an 8-bit MBmultiplier

It is differ from conventional type by its error correcting vector. In this type error correcting vectors ECW1 is generated by PP1 and ECW2 is generated by PP2.

ECW1= 0 E12 0 F 10

ECW2= 0 E 22 0 F 20

To eliminate a RBPP accumulation, ECW 2 needs to be incorporated into PP1 and PP2.

F 20={-1 , b5 b4 b3=000,001,010,011,111

F20={0 , b 5b4b3=100,101,110

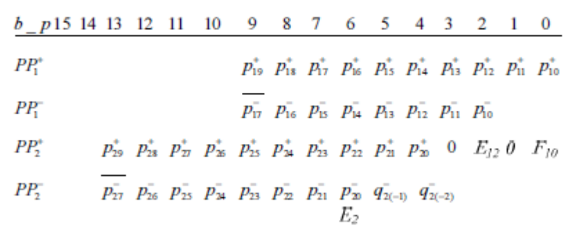
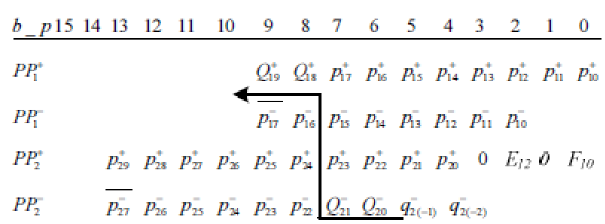


Fig 2(B)REVISED RBMPPG BY REPLACING E 22 AND F 20



(c)

Fig2(C)FINAL PROPOSED RBMPPG BY TOTALLY ELIMINATING ECW 2

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

Q 19+ ,Q 18+,Q 21-,Q20- are used to represent the modified partial products .By setting PP2+ to all ones and adding +1 to the LSB of the partial product ,F20 can then be determined only by b 5

F 20 = {-1, b 5 =0

F 20= {0, b 5 =1

As -1 can be coded as 111 in RB format,E 22 and F 20 can be represented by E 2 ,q 2(-2-) ,q 2(-1)- as follows

$$E_2 = \begin{cases} E_{22}, & F_{20} = 0 \\ E_{22} - 1, & F_{20} = -1 \end{cases}$$

$$q^-_{2(-2)} = q^-_{2(-1)} = \begin{cases} 0, & F_{20} = 0 \\ 1, & F_{20} = -1 \end{cases}$$

This is further explained by the truth table of E 22 ,F 20 and E 2 ,q 2- (-2) ,q 2- (-1) .

TABLE III

TRUTH TABLE OF E_2, $q^-_{2(-2)}$, $q^-_{2(-1)}$ AND p^-_{21}, p^-_{20}.

$b_7b_6b_5$	$E_{22}F_{20}$	$E_2q^-_{2(-2)}q^-_{2(-1)}$	p^-_{21}	p^-_{20}
0 0 0	0 $\bar{1}$	$\bar{1}$ 1 1	0	0
0 0 1	0 0	0 0 0	a_1	a_0
0 1 0	0 $\bar{1}$	$\bar{1}$ 1 1	a_1	a_0
0 1 1	0 0	0 0 0	a_0	0
1 0 0	1 $\bar{1}$	0 1 1	$\overline{a_0}$	1
1 0 1	1 0	1 0 0	$\overline{a_1}$	$\overline{a_0}$
1 1 0	1 $\bar{1}$	0 1 1	$\overline{a_1}$	$\overline{a_0}$
1 1 1	0 0	0 0 0	0	0

The relationships between Q 19+ ,Q 18+,Q 21- ,Q20- and P19+,P21-,P20- are summarized in table.

THE TRUTH TABLE OF Q^+_{19}, Q^+_{18}, Q^-_{21}, Q^-_{20}

$p^+_{19}p^+_{18}p^-_{21}p^-_{20}$	$Q^+_{19}Q^+_{18}Q^-_{21}Q^-_{20}$ (E_2=0)	$Q^+_{19}Q^+_{18}Q^-_{21}Q^-_{20}$ (E_2=1)	$Q^+_{19}Q^+_{18}Q^-_{21}Q^-_{20}$ (E_2= −1)
0100	0100	0101	0011
0101	0101	0110	0100
0110	0110	0111	0101
0111	0111	1000	0110
1000	1000	1001	0111
1001	1001	1010	1000
1010	1010	1011	1001
1011	1011	1100	1010

Logic functions of Q19+ ,Q18+,Q21-and Q20- can be expressed as follows

$$Q^+_{19} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^+_{19} + \overline{b_7}\,\overline{b_5} \cdot (p^+_{18} + p^-_{21} + p^-_{2}$$
$$p^+_{19}) + b_7\overline{b_6}b_5 \cdot (p^+_{18}p^-_{21}p^-_{20} \oplus p^+_{19})$$

$$Q^+_{18} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^+_{18} + \overline{b_7}\,\overline{b_5} \cdot (\overline{p^-_{21} + p^-_{20}} \oplus p$$
$$+ b_7\overline{b_6}b_5 \cdot (p^-_{21}p^-_{20} \oplus p^+_{18})$$

$$Q^-_{21} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^-_{21} + \overline{b_7}\,\overline{b_5} \cdot \overline{p^-_{21} \oplus p^-_{20}}$$
$$+ b_7\overline{b_6}b_5 \cdot p^-_{21} \oplus p^-_{20}$$

$$Q^-_{20} = (b_7 \oplus b_5 + b_7b_6b_5) \cdot p^-_{20} + \overline{b_7}\,\overline{b_5} \cdot \overline{p^-_{20}}$$
$$+ b_7\overline{b_6}b_5 \cdot \overline{p^-_{20}}$$

TABLE III

Therefore, the extra ECWN/4 is removed by the transformation of 4 partial product variables and one

partial product row is saved in RB multipliers with any power-of-two word-length.

2.3 RBPA

In the second stage, a 4-stage RBA summing tree is used to sum 16 RB partial products. Each RBA block contains 64 RB full adder (RBFA) cells and a varying number of RB half adder (RBHA) cells depending on where it is located**.** The proposed RBMPPG-2 can be applied to any bit RB multipliers with a reduction of a RBPP accumulation stage compared with conventional designs. Although the delay of RMPPG-2 increases by 1-stage of TG delay, the delay of one RBPP accumulation stage is significantly larger than a 1-stage TG delay. Therefore, the delay of the entire multiplier is reduced. The improved complexity, delay and power consumption are very attractive for the proposed design. The multiplier consists of the proposed RBMPPG-2, three RBPP accumulation stages, and one RB-NB converter. Eight RBBE-2 blocks generate the RBPP they are summed up by the RBPP reduction tree that has three RBPP accumulation stages. Each RBPP accumulation

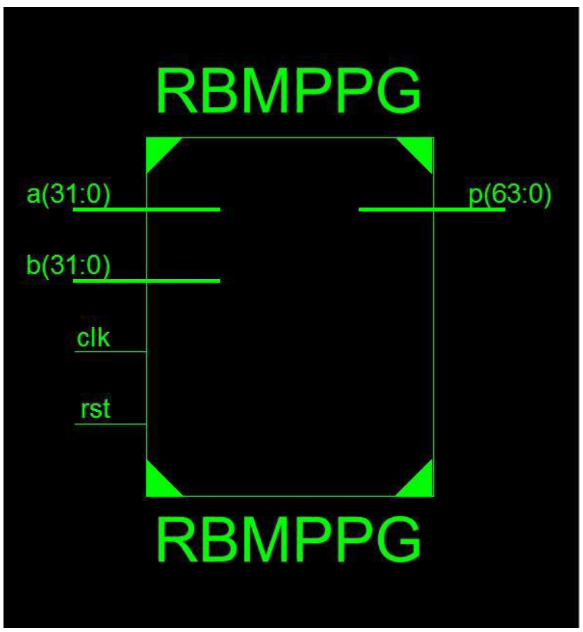
International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

block contains RB full adders (RBFAs) and half adders (RBHAs).

2.3RB –NB CONVERTER

The 64-bitRB-NB converter converts the final accumulation results into the NB representation, which uses a hybrid parallel prefix/carry select adder.

IV. RESULTS AND DISCUSSIONS



Block diagram

The performance of various 2n-bit RB multipliers using the proposed RBMPPG-2 is assessed; the results are compared with NBBE-2, CRBBE-2 and RBBE-4 [14] multipliers that are the latest and best designs found in the technical literature. All designs of RB multipliers use the RBFA and RBHA of [7]. An RB-NB converter is required in the final stage of the RB multiplier to convert the summation result in RB form to a two's complement number. It has been shown that the constant-time converter in [7] does not exist [19-21]. However, there is a carry-free multiplier that uses redundant adders in the reduction of partial products by applying on-the-fly conversion [22] in parallel with the reduction and generates the product without a carry-propagate adder. A hybrid parallel-prefix/carry-select adder [25] is used for the final RB-NB converter.

In the simulation of each design, a supply voltage of 1.25V and room temperature are assumed.

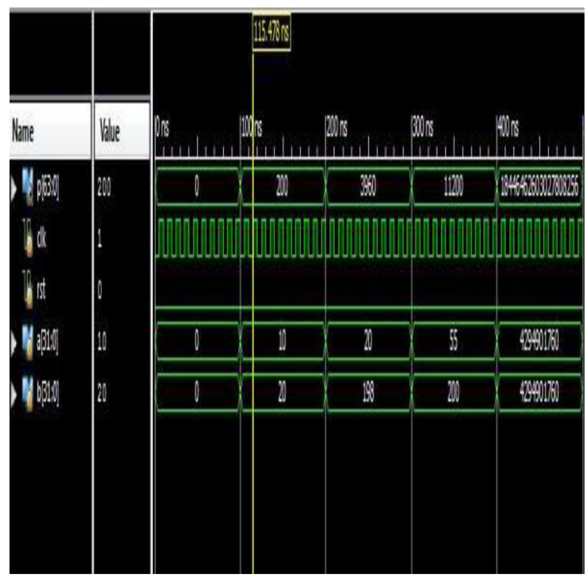
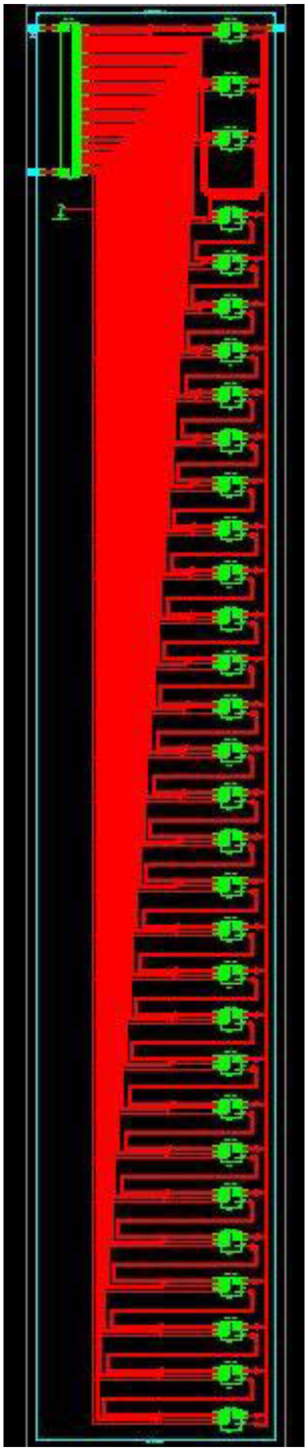


Fig 3(a) simulation result of proposed system

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	1136	704	161%
Number of 4 input LUTs	1983	1408	140%
Number of bonded IOBs	128	108	118%

Design summary

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org



RTL SCHEMATIC

Consider the delay first compared with CRBBE-2, the proposed designs can reduce the delay (for example up to 16.6% for the case of 8×8-bit multiplier; for all cases of word-length, the delay is reduced by at least 10%. Compared with RBBE-4, the proposed design can reduce the delay by up to 24.8% for the case of 32×32-bit and the delay is reduced by at least 17% for all cases of word-length. The delay improvement is achieved by the reduced critical path due to the elimination of one RBPP accumulation stage. Compared with CRBBE-2, the RB multiplier using the proposed RBMPPG-2 has the smallest area for all cases For 16×16-bit multipliers, the area of RBBE-4 RB multipliers is smaller than that of the proposed RB multipliers because RBBE-4 based designs don't require extra ECW, while the area is slightly increased by the modified partial product in the proposed RB multipliers

V. CONCLUSION

A new modified RBPP generator has been proposed in this paper; this design eliminates the additional ECW that is introduced by previous designs. Therefore, a RBPP accumulation stage is saved due to the elimination of ECW. The new RB partial product generation technique can be applied to any 2n-bit RB multipliers to reduce the number of RBPP rows from N/4 + 1 to N/4. Simulation results have shown that the performance of RB MBE multipliers using the proposed RBMPPG-2 is improved significantly in terms of delay and area. The proposed designs achieve significant reductions in area and power consumption when the word length is at least 32 bits.

VI. REFERENCES

[1]A. Avizienis, “Signed-digit number representations for fastparallel arithmetic,” IRE

Trans. Electron. Computers,vol. EC-10,pp. 389–400, 1961.

[2] N.Takagi, H. Yasuura, and S. Yajima, "High-speed VLSI multiplicationalgorithm with a redundant binary addition tree,"IEEE Trans. Computers, vol. C-34, pp. 789-796, 1985.

[3] Y. Harata, Y. Nakamura, H. Nagase, M. Takigawa, and N.Takagi, "A high speed multiplier using a redundant binaryadder tree," IEEE J. Solid-State Circuits, vol. SC-22, pp. 28-34,1987.

[4] H. Edamatsu, T. Taniguchi, T. Nishiyama, and S. Kuninobu, "A33 MFLOPS floating point processor using redundant binary representation," in Proc. IEEE Int. Solid-State Circuits Conf.(ISSCC), pp. 152–153, 1988.

[5] H. Makino, Y. Nakase, and H. Shinohara, "A 8.8-ns 54x54-bitmultiplier using new redundant binary architecture," in Proc.Int. Conf. Comput. Design (ICCD), pp. 202-205, 1993.

[6] H. Makino, Y. Nakase, H. Suzuki, H. Morinaka, H. Shinohara,and K. Makino, "An 8.8-ns 54×54-bit multiplier with highspeed redundant binary architecture," IEEE J. Solid-State Circuits,vol. 31, pp. 773-783, 1996.

[7] Y. Kim, B. Song, J. Grosspietsch, and S. Gillig, "A carry-free54b×54b multiplier using equivalent bit conversion algorithm,"IEEE J. Solid-State Circuits, vol. 36, pp. 1538–1545,2001.

[8] Y. HeandC.Chang, "A power-delay efficient hybrid carrylookaheadcarry-select based redundant binary to two's complementconverter," IEEE Trans. Circuits Syst. I, Reg. Papers,

[9] G. Wang and M. Tull, "A new redundant binary number to 2'scomplementnumber converter," in Proc. Region 5 Conference:Annual Technical and Leadership Workshop, pp. 141-143, 2004.

[10] W. Yeh and C. Jen, "High-speed Booth encoded parallel multiplierdesign," IEEE Trans. Computers, vol. 49, pp. 692-701,2000.

[11] S. Kuang, J. Wang, and C. Guo, "Modified Booth multiplierwith a regular partial product array," IEEE Trans. Circuits Syst.II, vol. 56, pp. 404-408, 2009.

[12] J. Kang and J. Gaudiot,"A simple high-speed multiplier design,"IEEE Trans. Computers, vol. 55, pp.1253-1258, 2006.

[13] F. Lamberti, N. Andrikos, E. Antelo, and P. Montuschi, "Reducingthe computation time in (short bit-width) two's complementmultipliers," IEEE Trans. Computers, vol. 60, pp. 148-156, 2011.

[14] Y. He and C. Chang, "A new redundant binary Booth encodingfor fast 2 -bit multiplier design," IEEE Trans. Circuits Syst. I,Reg. Papers, vol. 56, pp. 1192–1199, 2009.

[15] Y. He, C. Chang, J. Gu, and H. Fahmy, "A novel covalent redundantbinary Booth encoder," in Proc. IEEE Int. Symp. CircuitsSyst. (ISCAS), vol. 1, pp. 69–72, 2005.