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A NEW NESTED NEUTRAL POINT-CLAMPED (NNPC) INVERTER FOR A SIMPLE CAPACITOR VOLTAGE BALANCING

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ABSTRACT

Balancing of capacitor voltage by using logic switching table for nested neutral point clamped (NNPC) inverter is proposed in this thesis. NNPC inverter is a four level voltage source inverter in conversion of medium voltages, in range of (2.2-7.4kv) without using semiconductor devices in series it, to obtain high output voltage. NNPC network consists of two flying capacitors in each phase. So that inverter can operator balancing condition and voltage across each switching device can have same voltage drop, controlled maintained 1/3 DC supply voltage the balancing of capacitor voltage in this way makes the advantages of less switching losses, controlled and balancing the flying capacitor voltage. For this process a simply logic tables are constructed for balancing voltage controlled technique. So that in this way balance the capacitor voltage needs less calculation compared to other techniques. This method is also suitable to integrate with different modulation schemes like pulse width modulation space sector modulation and sinusoidal pulse width modulation etc., these results are verified by using simulation technique.

INTRODUCTION:

Nowadays, Multilevel inverters are very popular in medium voltage applications and motor drives due to reduction of harmonics, low voltage stress on switches, low switching frequency, and less switching losses [1]. The multilevel inverters categorized into neutral point clamped (NPC) inverter, flying capacitor (FC) inverter, cascaded Hbridge inverter, and modular multilevel converter [2]–[3]. Several control techniques and modulation strategies including capacitor voltage-balancing methods have been developed in the literature for multilevel inverters [4]. In this paper a new multilevel topology is proposed. i.e, nested neutral point clamped (NNPC) inverter shown in Fig. 1.

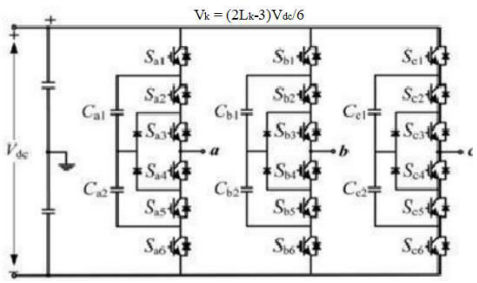

Fig. 1. Three phase nested neutral-point clamped (NNPC) inverter.

NESTED NEUTRAL POINT CLAMPED INVERTER

Operation of the NNPC inverter:

Figure(1) shows the three phase NNPC inverter .Each phase of NNPC consists of two FCS, six switches and two clamping diodes .keep the fcs voltage at Vdc/3 to produce four output levels in phase voltage so that all the switches can share equal voltage stress. Table 1 shows the output level Lk, phase voltage Vk and corresponding switching state Sk. The four different voltages -Vdc/2, -Vdc/6, Vdc/6 and Vdc/2 for levels 0,1, 2 and 3.The relation between Vk and Kk is given below.

Vk = (2Lk-3)Vdc/6

For level 3 and level 0, there is no unwanted switching state. for level 1 have two unwanted switching states 1A and 1B .the two unwanted switching states produce equal output voltage -Vdc/6 for different ON and OFF switching's .for level 2 also have

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two unwanted switching's states, they are 2A and 2B and produce equal output voltage Vdc/6 for different ON and OFF switching's.

Behaviour analysis of the capacitor voltages in the NNPC inverters:

The capacitors Ck1 and Ck2 are two series FCs in the phase K and Vcks are two voltages across each capacitor respectively .the behavior of capacitor voltages depends on the phase current Ik and switching states S k.

There are stages in the behavior of the capacitor voltage in the NNPC inverter.

Stage (1)

For level 0 and level 3, there is no problem on capacitor voltages because no current flows through capacitors as shown in figures 1.1 and 1.2

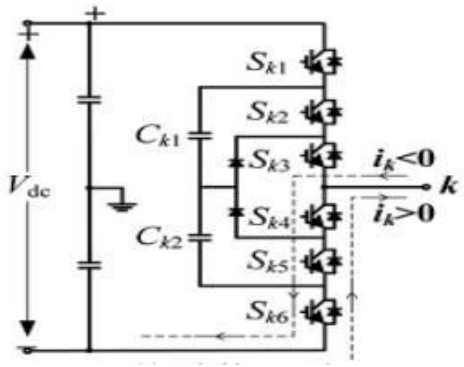

Figure 1.2 Switching state 0

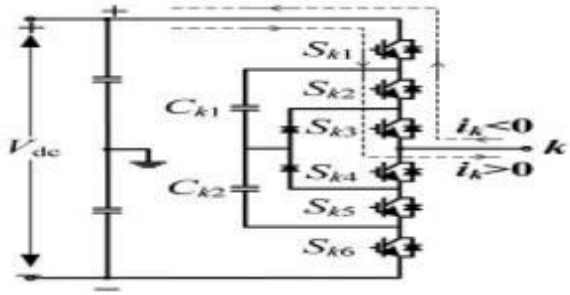

Figure 1.3 Switching state 3

Stage (2)

For level 1, the unwanted switching state 1A and ik>0, capacitor Ck2 discharges and capacitor Vck2 decreases.

If Ik <0, the capacitor Ck2 charges and Vck2 increases and there is no impact on capacitor Ck1,shown in figure 1.3.

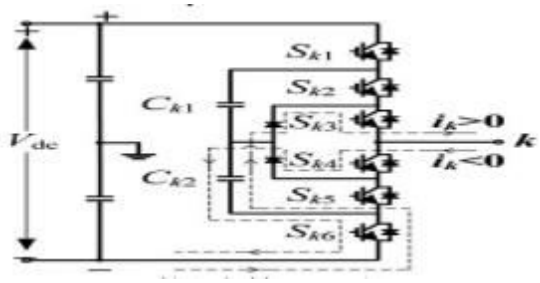

Figure 1.4 Switching state 1A

For switching state 1B

When Ik>0, the capacitor Ck1 and Ck2 charge and capacitor voltage Vck1 and Vck2 increases.

When Ik<0, the Ck1 and Ck2 discharge and Vck1 and Vck2 decrease shown in figure 1.4.

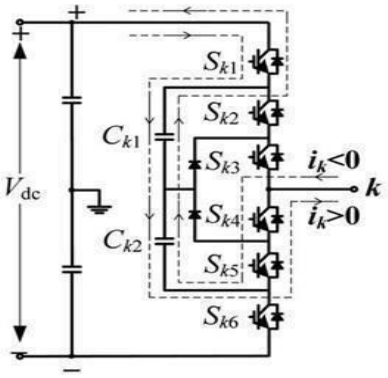

Figure 1.5 Switching state 1B.

Stage 3

For level 2A

When Ik>0, both capacitors Ck1 and Ck2 discharges and capacitor voltage Vck1 and Vck2 decrease.

When Ik<0, both capacitors Ck1 and Ck2 charge and capacitor voltage increase, as shown in figure 1.5.

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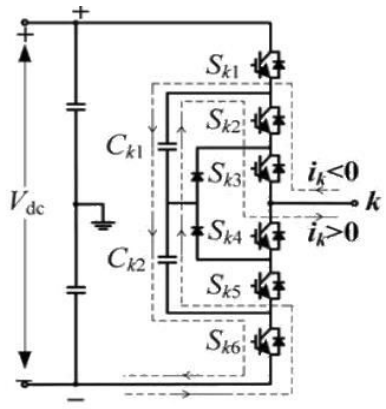

Figure 1.6 switching state 2A

For level 2B

When Ik>0, capacitor Ck1 is charge and voltage Vck1 increase.

When Ik<0, capacitor Ck1 is discharge and voltage Vck1 decrease, as shown in figure 1.6.

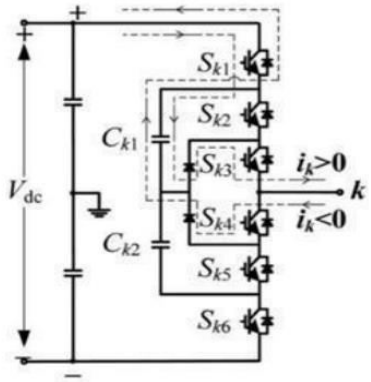

Figure 1.7 Switching state 2B.

The above switching state of each stage is based on the simple logic table as shown below.

Table (1)
Phase voltages and switching states in NNPC inverter

Phase voltage ,V k	Output voltage level, L k	Phase switching, Sk	states of each device					
			S1	S2	S3	S4	S5	S6
V dc/2	3	3	1	1	1	0	0	0
V dc/6	2	2A	0	1	1	0	0	1
		2B	1	0	1	1	0	0
-V dc/6	1	1A	0	0	1	1	0	1
		1B	1	0	0	1	1	0
V dc/2	0	0	0	0	0	1	1	1

Table (2)

The voltage across the flying capacitor under different phase current and switching states are summarizes in below Table2

Phase voltage V k	Output voltage level, L k	Phase current, I k	The behavior of flying capacitor voltage	
			Vck1	Vck2
dc/2	3		No change	No change
		>0	Decrease(2A	Decrease(2A

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dc/6	2		),Increase(2B)	),Nochange(2B)
		<0	Increase(2A),Decrease(2B)	Increase(2A),Nochange(2B)
Vdc/6	1		No change(1A), Increase(1B)	Decrease(1A),increase(1B)
			Nochange(1A),Decrease(1B)	Increase(1A),Decrease(1B)
Vdc/2	0	-	No change	No change

For balancing capacitor voltage we need to control NNPC inverters and FCs otherwise FC voltages will differ from their desired value, because there is no control over the currents flow out or into capacitors for balancing voltage the following condition is used.

$$Vcki = Vcki - Vdc/3$$

Where

Vcki=capacitor voltages

Vcki=change in capacitor voltage

K=a, b , c

i=1, 2

To balance capacitor voltage Vki is controlled nearer to zero.

How the switching states are selected,

Case (1) if Vcki>0

The switching state is selected in such way that the capacitor voltage should be decrease

Case (2)

If Vcki<0 the switching state is selected in such way that the capacitor voltage should be increased

The above operation is given below table how the capacitor voltage is decreased and increased based on the selected level.

Table 3 shows the logic controlling of the capacitor Vck1 is given below.

Table (3)

Simplified logic table for Balanced Capacitor Voltage Vck1

Input conditions		Output results The selected switching state (Sk) forcontrollingVck1
Lk	Vck1*Ik	
2	< 0	2B
	> 0	2A

Case (1) Vck1 <0,the switching state 2A is selected if ik <0,otherwise the switching state 2Bis selected if
ik>_0,

Case (2) Vck1>_0 the switching state 2B is selected if

ik<0 Otherwise the switching state 2A is selected if ik>_0

In this way the capacitor voltage vck1 is completely controlled, independently the flow of current direction in the inverter. Table (4) shows the controlling of capacitor

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voltage Vck2.

Table (4)

Logic table for balanced capacitor voltage Vck2

Input conditions		Output results
Lk	Vck 2*Ik	The selected switching state(Sk) for controlling Vck2
1	<0	1B
	>0	1A

Case (1) Vck2<0

The switching state 1A is selected if ik<0, otherwise the switching state 1B is selected if

ik>_0 Case (2) Vck2>_0

The switching state 1B is selected if ik<0, otherwise the switching state1A is selected if ik>_0

SIMULATION RESULTS:

EXISTING RESULTS:

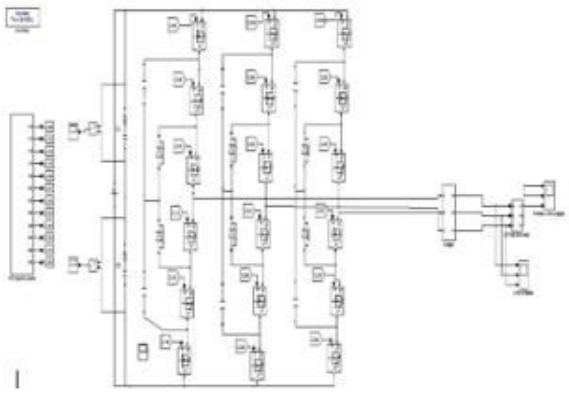

Figure 6.1 Matlab diagram of three phase NNPC inverter for controlling PMSM

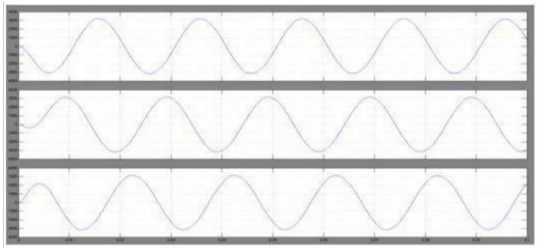

Figure 6.2 filtered voltages

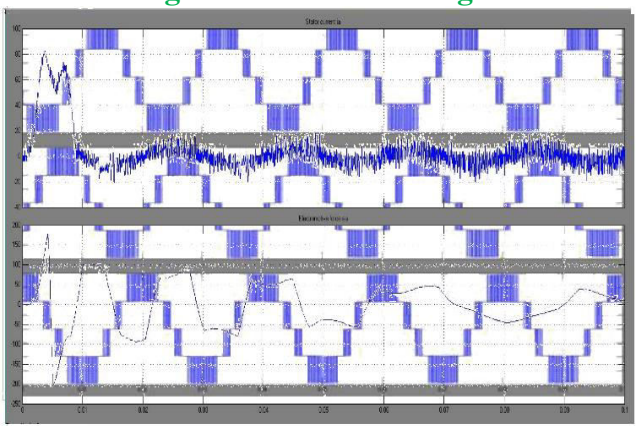

Figure 6.3 Output voltages of NNPC without filter

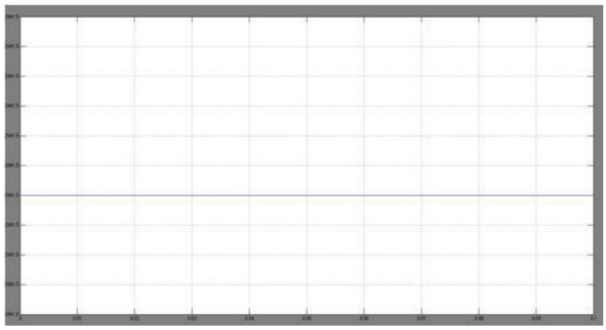

Figure 6.4 capacitor voltage

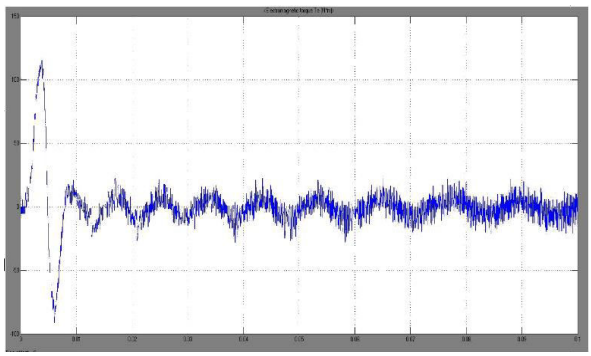

Figure 6.5 stator current and electromotive force (EMF) of PMSM

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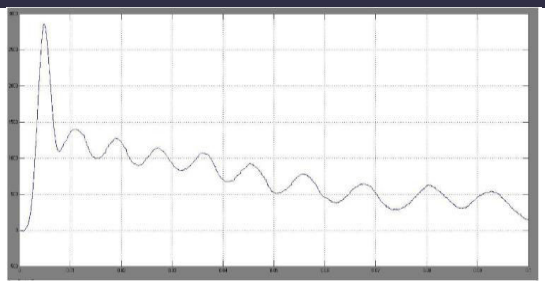

Figure 6.6 speed of the PMSM

CONCLUSION:

In this thesis we developed A capacitor voltage balancing system for four level NNPC inverter by using logic table switching's and controlling of flying capacitor voltage in the limited range by logical switching mode operation is purposed. The advantage of this motor reduces the phase switching state to control and balance FC voltage. So that number of computations is reduced and also this system is easy to use with different PWM techniques. The limitations of the method are capacitor size is going on researching. After developing a four level NNPC inverter output is connected to PMSM for controlling. The output of NNPC is filter with RC low pass filter for obtaining approximant sinusoidal input to the PMSM. Finally simulation results are obtain

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