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SYNCHRONIZATION OF GRID VOLTAGE WITH DISTRIBUTED GENERATION SYSTEMS UNDER GRID FAULT CONDITIONS

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ABSTRACT:
The actual grid code requirements for the grid connection of distributed generation systems, mainly wind and photovoltaic (PV) systems, are becoming very demanding. The transmission system operators (TSOs) are especially concerned about the low-voltage-ride-through requirements. Solutions based on the installation of STATCOMs and dynamic voltage regulators (DVRs), as well as on advanced control functionalities for the existing power converters of distributed generation plants, have contributed to enhance their response under faulty and distorted scenarios and, hence, to fulfill these requirements. In order to achieve satisfactory results with such systems, it is necessary to count on accurate and fast grid voltage synchronization algorithms, which are able to work under unbalanced and distorted conditions. This paper analyzes the synchronization capability of three advanced synchronization systems: the decoupled double synchronous reference frame phase-locked loop (PLL), the dual second order generalized integrator PLL, and the three-phase enhanced PLL, designed to work under such conditions. Although other systems based on frequency-locked loops have also been developed, PLLs have been chosen due to their link with dq0 controllers. In the following, the different algorithms will be presented and discretized, and their performance will be tested in an experimental setup controlled in order to evaluate their accuracy and implementation features

I. INTRODUCTION

THE importance of power quality (PQ) has risen very considerably over the last two decades due to a marked increase in the number of equipment which is sensitive to adverse PQ environments, the disturbances introduced by nonlinear loads, and the proliferation of renewable energy sources, among others. At least 50% of all PQ disturbances are of the voltage quality type, where the interest is the study of any deviation of the voltage waveform from its ideal. The best well-known disturbances are voltage sags and swells, harmonic and inter harmonic voltages, and, for three-phase systems, voltage imbalances. A voltage sag is normally caused by short-circuit faults in the power network or by the starting up of induction motors of large rating. The ensuing adverse consequences are a reduction in the energy transfers of electric motors and the disconnection of sensitive equipment and industrial processes brought to a standstill. A comprehensive description of voltage sags can be found.

Harmonics are produced by nonlinear equipment, such as electric arc furnaces, variable speed drives, large concentrations of arc discharge lamps, and loads which use power electronics. Harmonic currents generated by a nonlinear device or created as a result of existing harmonic voltages will exacerbate copper and iron losses in electrical equipment. In rotating machinery, they will produce pulsating torques and overheating. Voltage imbalances are normally brought about by unbalanced loads or unbalanced short-circuit faults, thus producing overheating in synchronous machines and, in some extreme cases, leading to load shutdowns and equipment failure. The DVR is essentially a voltage-source converter connected in series with the ac network via an interfacing transformer, which was originally conceived to amelio rate voltage sags.However, as shown in this paper, its range of applicability can be extended very considerably when provided with a suitable control scheme. The basic operating principle behind the DVR is the injection of an inphase

series voltage with the incoming supply to the load, sufficient enough to reestablish the voltage to its presag state. Its rate of success in combating voltage sags in actual installations is well documented, this being one of the reasons why it continues to attract a great deal of interest in industry and in academic circles. Research work has been reported on DVR two-level and multilevel topologies as well as on control and operation. The latter may be divided into several topics. 1) The configuration, whether two-level or multilevel, relates to the availability, or otherwise, of energy storage, the output filter, and the capacity to cancel out unbalanced voltages in three-phase four-wire systems. 2) The voltage-sag detection. Several techniques have been used to detect the instant of sag appearance, such as measurement of the peak value of the grid voltage. A comprehensive analysis of these techniques can be found. 3) The control strategy. The DVR may be operated to inject the series voltage according to several criteria, such as minimum energy exchange with the grid. The three most popular strategies to compensate voltage sags: 1) presag compensation. The injected DVR voltage is calculated to simply compensate the load voltage to its presag condition; 2) inphase compensation. The DVR voltage is always in phase with the grid voltage; and 3) optimal energy compensation. This strategy minimizes the energy transfer between the energy storage and the grid during steady-state operation. Although these are the best well-known control strategies, many efforts are being made to develop new ones to enable better DVR utilization, as amply discussed. 4) The design of the control law. The controller is normally designed with some specific aims firmly in mind, such as the kind of disturbances it should ameliorate, the velocity of time response, error in steady-state, etc. Most of the published work on DVR uses a simple proportional-integral (PI) control law implemented in a frame of reference which rotates with the frequency of the grid voltage. This basic approach is sufficient to enable voltage sag compensation, to warrant zero tracking error for the fundamental component, and to compensate certain kinds of unbalanced conditions. However, this simple control law is insufficient when dealing with high-performance applications and more complex controllers are required. The former reference adds resonant control filters to the existing PI control scheme in order to eliminate harmonic voltages. The main drawback of this structure is that one filter is required for each harmonic to be eliminated if the system is unbalanced and only half that number if the system is balanced. The latter reference takes the approach of adding a feed forward loop to the feedback PI controller in order to improve the control overall performance, taking into account the time delay of the sampled system and the DVR output filter constraints. This paper focuses on the design of a closed-loop control law for a two-level DVR, based on the so-called repetitive control, aiming at compensating key voltage-quality disturbances, namely, voltage sags, harmonic voltages, and voltage imbalances. Repetitive control was first introduced in to eliminate periodic disturbances and to track periodic reference signals with zero tracking error. A detailed analysis of various repetitive control Configurations is reported. The repetitive control was originally applied to eliminate speed fluctuations in electric motors but it has since been adopted in a wide range of power-electronics applications.a repetitive controller is applied to obtain an output voltage with low distortion in a constant voltage, constant frequency three-phase PWM inverter. In a repetitive controller is used to achieve zero tracking error in the output current of a three-phase rectifier in order to improve its power factor. A more recent example is found, where a repetitive controller is used in a parallel active filter to cancel out harmonic currents produced by a nonlinear load. The repetitive controller presented in this paper has a wider range of applicability; it is used in a DVR system to ameliorate voltage sags, harmonic voltages, and voltage imbalances

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within a bandwidth. Unlike other schemes, which also have a comparable range of applicability, only one controller is needed to cancel all three disturbances simultaneously. The control structure contains a grid voltage feed forward term to improve the system transient response, and a closed-loop control which comprises a feedback of the load voltage with the repetitive controller in order to warrant zero tracking error in steady state.

II. GRID SYNCHRONIZATION SPECIFICATIONS BASED ON GCR

Even though several works are published within the field of grid synchronization, almost all of them are centered on analyzing the individual dynamic performance of each proposal, without first determining a time response window within the dynamic behavior of the system under test, which would be considered to be satisfactory. In this paper, in order to evaluate the response of the grid synchronization topologies under test, a common performance requirement for all the structures has been established in this section, considering the needs that can be derived from the LVRT requirements.

Despite the fact that the detection of the fault can be carried out with simpler algorithms, as shown in [39] and [40], the importance of advanced grid synchronization systems lies in the necessity of having accurate information about the magnitude and phase of the grid voltage during the fault, in order to inject the reactive power required by the TSO.

In the German standard, it is stated that voltage control must take place within 20 ms after the fault recognition, by providing a reactive current on the low voltage side of the generatortransformertoatleast2%oftheratedcurrentforeach percent of the voltage dip, as shown in Fig. 1. 100% reactive power delivery must be possible, if necessary. A similar condition is given in the Spanish grid code, where the wind power plants are required to stop drawing inductive reactive power within 100 ms of a voltage drop and be able to inject full reactive power after 150 ms, as shown in Fig. 2.

Considering these demands, this paper will consider that the estimation of the voltage conditions will be carried out within 20–25 ms, as this target permits it to fulfill the most restrictive requirements, in terms of dynamical response, available in the grid codes. This condition will be extended to frequency estimation; although this parameter is more related to secondary control algorithms than LVRT, the same time window between 20 and 25 ms will be considered in this work for the detection of the disturbance.

III. DESCRIPTION OF THE THREE SYNCHRONIZATION SYSTEMS

Many of the positive-sequence detection algorithms are based on SRF PLLs. Despite having a good response under balanced conditions, their performance becomes insufficient in unbalanced faulty grids (95% of cases), and their good operation is highly conditioned to the frequency stability, which is incompatible with the idea of a robust synchronization system. Many authors have discussed different advanced models, which are able to overcome the problems of the classical PLL, using frequency and amplitude adaptive structures which are able to deal with unbalanced, faulty, and harmonic-polluted grids. In the framework of these topologies, three PLL structures will be discussed and evaluated in this paper.

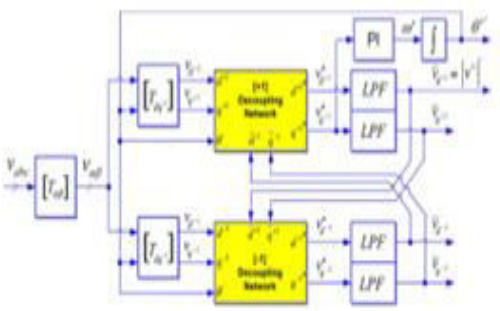

Fig 1DDSRF-PLL Block Diagram
CIRCUIT DIAGRAM

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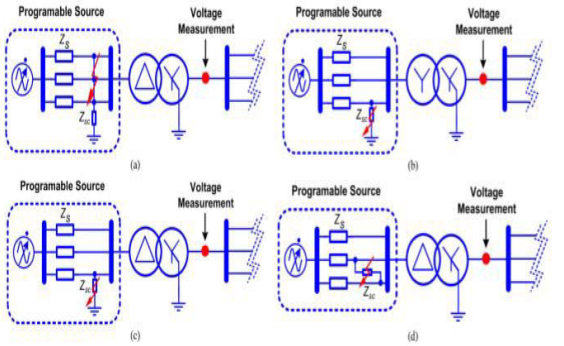

Fig. 11. Generation of grid voltage sags in the experimental setup. (a) Generation of a Type "A" voltage sag. (b) Generation of a Type "B" voltage sag. (c) Generation of a Type "C" voltage sag. (d) Generation of a Type "D" voltage sag.

TESTING SIGNALS AND EXPERIMENTAL SETUP

Following the representations in the discrete domain already deducted, the different PLL algorithms have been implemented in a control board based on a floating-point Texas Instruments TMS320F28335 DSP at 150 MHz (6.67-ns cycle time). Their capability to perform a fast and accurate synchronization has been tested in the laboratory under different grid faults cenarios, where the three-phase voltage waveforms experience transients due to the appearance of voltage sags, frequency variations, and harmonic pollution. These unbalanced and distorted input voltages were generated by means of an ac programmable source and an auxiliary transformer. The layout of the experimental workbench used in this paper is presented in Fig. 10.

Six representative faulty and distorted scenarios have been selected for evaluating the three synchronization systems under test.

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Voltagesags:InTableI,thecharacteristicsoffour selected voltage sags have been summarized. It is worth to mention

hat these sags are the most characteristic ones that affect wind power systems. In Table I, the magnitude and the phase of the symmetrical components of the voltage during the fault period are indicated in each case, assuming that the prefault voltage is always equal to V + = 100, V − =0, and V 0 =0 . As can be seen in the table, three of the proposed sags give rise to unbalanced voltages, as explained in [37] and [38], and, hence, to positive- and negative-sequence components. The presence of the negative sequence during the fault allows a more rigorous analysis of the synchronization capability of the different algorithms under test. Moreover, unbalanced faults constitute 95% of the voltage sags that affect distributed generation systems.

In order to obtain the aforementioned dips, different faults have been emulated with the programmable ac source at the primary winding of the transformer, asindicated inFig. Depending on the fault topology as well as on the connection of the transformer, the desired voltage waveforms at the measurement point, indicated in Table I, are finally obtained, acquired, and later processed by the DSP.

• Harmonic-polluted voltage (8% THD): According to the EN50160 standard, the THD of the voltage waveforms at the output of a generation facility cannot be higher than 8%. Considering this requirement, Table II shows the harmonic composition used for evaluating the performance of the grid synchronization systems under test when the grid voltages become distorted.

• Grid voltage frequency jumps: By means of the programmable source, a 10-Hz jump (from 50 to 60 Hz) in the frequency value of the positive sequence has been applied to analyze the response of the frequency adaptive structures under test.

In the following section, the responses of the DDSRF PLL, DSOGI PLL, and 3PhEPLL under these transient conditions will be compared.

Behavior in Case of Voltage Sags

1) Type "A" Sag Test:

This kind of voltage sag appears as a consequence of three-phase faults that give rise to high short circuit currents and, hence, to a balanced voltage drop in the network. As Fig. DDSRF PLL and the DSOGI PLL produce a good response, as both systems achieve a very fast detection (20 ms) of the positive-sequence components (less than two cycles). The response of the 3phEPLL,

depicted in Fig. 12(m), also shows a good response, but with a larger transient in the positive-sequence estimation.

2) Type "B" Sag Test:

This kind of fault permits analyzing the behavior of the PLLs under test in the presence of zerosequence components at the input. The Clarke transformation used in DSOGI PLL and DDSRF PLL to extract the αβ components enhances the response of this synchronization system when the faulty grid voltage presents zero-sequence components. Their responses, as shown in Fig. 12(f) and (j), are fast and accurate. On the other hand, the 3phEPLL does not cancel out the zero-sequence component from the input voltage, something which may affect the dynamics of the positive-sequence estimation loop. However, this effect is further attenuated by the computational unit, as Fig. shows; the steady-state response is also reached with no great delay, as detailed in showing the good behavior of this PLL under these conditions.

3) Type"C"and"D"SagTests:

These kinds of sags appear due to phase-to-ground and phase-to-phase short circuits at the primary winding of the transformer, respectively, as shown in Table I. In a distribution network, these distortions are more common than the previous ones, as they are the typical grid faults caused by lightning storms. As depicted in Fig., all three PLLs permit detecting the positive sequence between 20 and 30 ms; however, the 3ph EPLL has as lowers tabilization, as shown in Fig.. This effect is a bit more notice able with the"C"sag, where the combination of the phase jumpand the magnitude change of two phases occurs, as shown.

IV. CONCLUSION

This paper studied the behavior of three advanced grid synchronization systems. Their structures have been presented, and their discrete algorithms have been detailed. Moreover, their performances have been tested in an experimental setup, where these algorithms have been digitally implemented in a commercial DSP, allowing proof of their satisfactory response under balanced and distorted grid conditions.

The DDSRF PLL and the DSOGI PLL allow estimating the ISCs of a three-phase system working in the αβ reference frame, while the 3phEPLL uses the "abc" reference frame, thus working with three variables. As has been shown, this feature simplifies the structure of the DSOGI PLL and the DDSRF PLL, which allows reducing the computational burden, as compared to the 3phEPLL, without affecting its performance.

The synchronization capability of the three PLLs under test has been shown to be fast and accurate under faulty scenarios, allowing the detection of the positive sequence of the voltage in 20–25 ms in all cases; however, the simpler structure of the DDSRF and the DSOGI affords an easier tuning of their control parameters and, therefore, a more accurate control of their transient response.

The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater bandpass and low-pass filtering capabilities. Although the DSOGI also gives rise to reasonably good results, due to its inherent bandpass filtering structure, its response is more affected by harmonics.

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