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Paper Authors

*** B.RAHUL, M.DEVADAS, G.NIHARIKKA**

* Dept of ECE, Vaagdevi College of Engineering, Warangal.

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DESIGN OF 16 BITADDER FOR RESIDUE NUMBER SYSTEM USING A NOVEL MODULO 2N-2K-1

[1]B.RAHUL, [2]M.DEVADAS, [3]G.NIHARIKKA
[1]PG Scholar, Dept of ECE, Vaagdevi College of Engineering, Warangal.
[2]Associate Professor, Dept of ECE, Vaagdevi College of Engineering, Warangal.
[3]Assistant Professor, Dept of ECE, Vaagdevi College of Engineering, Warangal.

ABSTRACT –
To design a 16 bit adder using this novel modulo 2^n-2^k- 1 is nothing but introducing a carry correction term K to reduce area in terms of any bit adder. Here Conventional Carry Select Adder is used to design a novel modulo 2^n-1 and modified conventional carry select adder to design a novel modulo 2^n-2^k-1 adder and so on. XILINX using Spartan 2 devices is used to illustrate the area report which gives complete information regarding the no of slices available and used respectively. Power is analyzed in report views to make this modulo adder more efficient respectively.

Keywords- area, power, CSA, MCSA

1. INTRODUCTION

normally in calculators modulo addition is performed by taking the sum of two numbers and dividing by 2 that willgenerate the result with quotient and remainder. The particular remainder is taken as the MOD value. If there is no remainder then there is no possibility of MOD application. In the design of novel modulo design residue number system is used to implement the design in binary representation .This novel modulo is implemented in MODELSIM which perform operation by taking each bit separately. The corresponding results are generated only after each clock cycle rate. The corresponding formulas which are applied to implement are shown in (1)

$$C=(A+B)_m=\begin{cases} A+B & A+B+T<2^n \\ (A+B+T)_m & A+B+T>2^n \quad (1) \end{cases}$$

The value of T is generally T=2^n-m. Here the value of n is 16 and the value of 2^{16} is 65,535. If both the bit integers of A and B is less than 65,535 then the first case is followed .If both the bit integers are greater than 65,535 then the second case shown in (1) is followed. T is the carry correction term used to implement the 16 bit adder respectively.

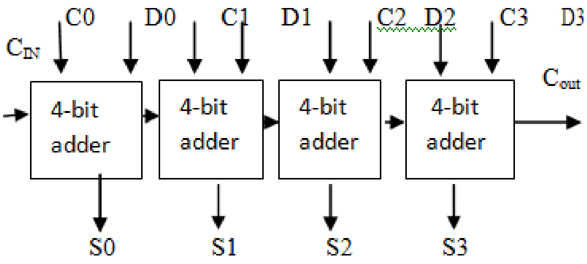
2. ADDER ARCHITECTURES

Adder architectures comprises of different set of adders which usually vary in architecture design and performance parameter. Normally area and speed efficiency should be simultaneously satisfied for the novel modulo. First adder architectures are discussed to find the adder which is suitable for 2^n-2^k-1 design modulo.

2.1 RIPPLE CARRY ADDER (RCA)

Ripple Carry Adder function is to ripple mostly from least significant to higher significant adder. Since the design is concerned with 16 bit only full adder has to be used. Full adder implies that three inputs are needed to get sum and carry.16 bit cannot be implemented in one clock cycle .This difficulty can be overcome by splitting into 4-bit adders which is shown in fig(1). Ripple carry addition performed in the first 4-bit will illustrate whether the carry correction term has to be used. If the carry in value is 0 then follow the first case of (1) .If the carry in value is 1 then follow the second case of (1).But this adder cannot be applied for the other set of 4-bit adders due to area increase.

In other words due to 4- bit adder increase delay path will be greater



2.1.Block Diagram of Ripple Carry Adder

2.2. CARRY SKIP ADDER (CSA):

The rippling pattern is almost similar to RCA but it usually generates worst case delay for the corresponding 4-bit adders. The main principle is only the carry is skipped over the entire group but not the operations which are involved in it. Sometimes while skipping the carry over the entire group, area will be doubled because some of the adders require two cycles for one bit operation.

CARRY LOOK - AHEAD ADDER (CLA)

Carry Look-Ahead is illustrated mainly in prefix tree structures due to cross- layer networks. Ripple carry addition cannot be performed for cross networks because cross networks usually originate from two different layers .In order to perform operation between two different layers only generation and propagation of bits is employed. The first layer bit can be taken as (g0,p0) and the second layer bit can be taken as (g1,p1).Then the corresponding operation has to be employed. Architecture of carry look ahead varies slightly from ripple carry adder in the generation of bit which is independent of the previous bit position. When this design is implemented in 2^n-2^k-1 modulo design first the word size followed by complexity increase would result in area increase obviously.

CARRY SELECT ADDER (CSA)

Generally in the first 4 bit addition with carry correction term will generate the carry value of 0 and without the carry correction term will generate the value 1.CSA function is to accept both the values of 0 and 1 and pass it to MUX to select the possible output.

3.1 ADD-ONE CIRCUIT

Suppose in the detection of the first 0 bit the invert operation has to be employed only if all the bits generated are 0. Otherwise all the bits has to be kept as non-invert and perform the operation IF there is no zero bit there is no possibility of detection then the normal sum is performed.

3.2 Binary To Excess-1 Converter

Digital electronics often employ the term binary to excess-3 converter. Generally in 4bit adder it has to be shifted to 3 bits. Some of the logic gates which are employed are and, not, ex- or. Binary to exces-1 will shift to 1 bit in order to convert the given 4 bit into 5 bit. Even though the use of MUX seems to be costly in terms of hardware description. Novel modulo needs to be implemented in terms of area and speed MUX is necessary for the implementation

The operation is illustrated below in the fig 2

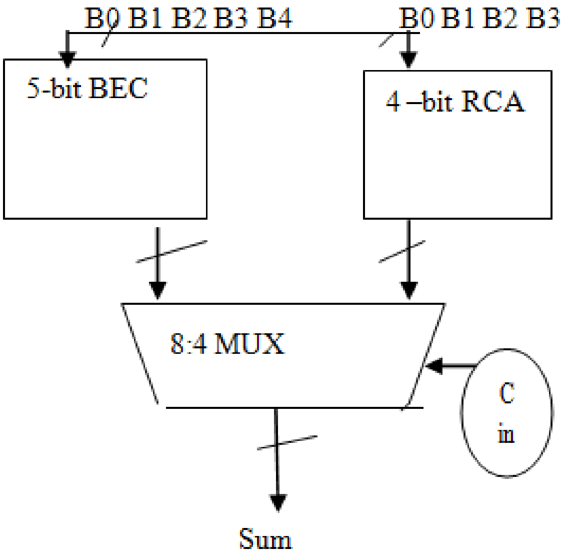


Fig.2 4 Bit Binary to Excess-1 Code Converter with 8:4Mux The main function of MUX is to select the most possible output from the given two values. 8:4 MUX receives the values from the two operations such as

RCA and BEC. First 4 bit addition has to be performed with RCA and the result outcome will be 4 bit. Second 4 bit has to be converted into 5-bit BEC. MUX will receive both 5bit and 4 bit RCA and generate 4 bit sum.

3.3 CONVENTIONAL CARRY SELECT ADDER FOR 2^n-1

$$(A+B)\ MOD\ (2^n-1) = \begin{cases} (A+B) & A+B<2^n \\ (A+B+1)MOD2^n & A+B>2^n \end{cases} \quad (2)$$

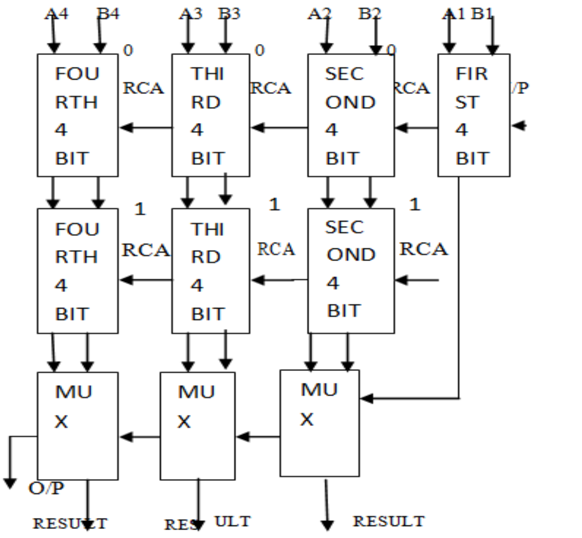


Fig.3. 16 Bits Conventional Carry Select Adder (CSA)

For First 4 bit normal RCA addition has to be performed normally and with A+B+1 term to get most possible outputs. If the carry value is 0 then A+B is employed and if the value is 1 then A+B+1 is employed for the other sets of 4-bit addition. Then 0 has to be fed into second, third, and final 4- bit.After completing the first stage process 1 has to be fed for the same operation in the second stage. MUX will select the most possible output from the two stages and final sum can be calculated.MUX will select the first stage o/p only when the Cin is 0 and second stage o/p is selected when Cin is 1.

3.4 MODIFIED CARRY SELECT ADDER FOR 2^n-2^k-1

In the case of MCSA the use of and, or, not can be significantly reduced than compared to CSA. The second stage of operation implies the area reduction than compared to second stage of CSA. The entire operation is illustrated in below fig

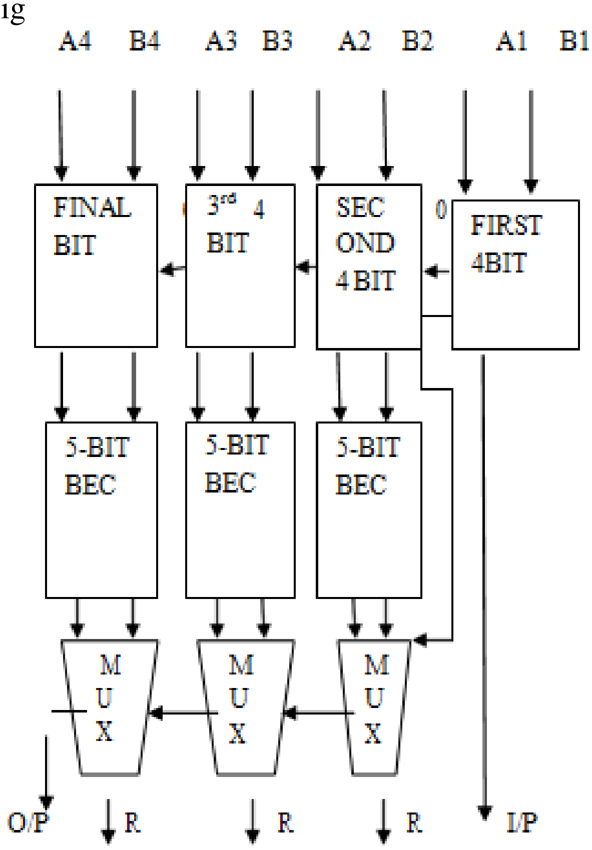


Fig.4. Modified Carry Select Adder (MCSA)

First 4 bits has to be taken and perform two additional operations with and without carry correction term. The carry correction term here is 15 because the value of k selected is 4. If the carry value is 0 then go for first case (A+B) then if the carry value is 1 then go for (A+B+T). Later 0 has to be fed into all the next 4 bits till the last for RCA operation. In the second stage 5-bit BEC has been implemented in order to reduce the extra addition in RCA.MUX will select the possible output from both the operations. In the first stage if the output is 0000.Then while employing BEC then the output becomes 00001 .Later during MUX operation

if the Cin is 0 then 0000 is selected otherwise 00001 is selected .

TABLE.1. 4 BIT RCA TO 5 BIT BEC

4 BIT RCA	5 BIT BEC
0000	00001
0010	00101
0011	00111

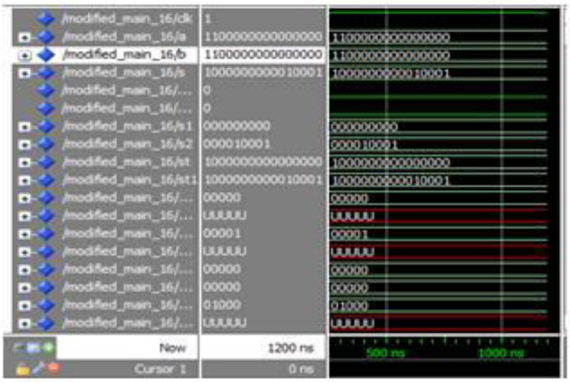
4. Results and Discussions

The area utilization synthesis for both the novel modulo 2^n- 2^k-1 and 2^n-1 adder is illustrated in table 3 respectively. The area synthesis report for both the design modulo implies that 2^n-2^k-1adder consumes lesser area than compared to 2^n-1 adder .The no of slices for the proposed design modulo has been illustrated in both table 2 respectively.

TABLE.2.AREA UTILIZATION FOR 2^n-2^k-1

Logic utilization	used	available	utilization
No of slice flip flop	29	1,536	1%
No of 4 i/p LUT	115	1,536	7%
No of bonded i/p	48	178	26%

From this table the area utilization for the proposed modulo has been significantly reduced based on several factors respectively.



```
/modified_main_16/clk     1
/modified_main_16/a       1100000000000000     1100000000000000
/modified_main_16/b       1100000000000000     1100000000000000
/modified_main_16/s       10000000000010001    10000000000010001
/modified_main_16/...     0
/modified_main_16/...     0
/modified_main_16/s1      000000000            000000000
/modified_main_16/s2      000010001            000010001
/modified_main_16/st      10000000000000000    10000000000000000
/modified_main_16/st1     10000000000010001    10000000000010001
/modified_main_16/...     00000                00000
/modified_main_16/...     UUUUU                UUUUU
/modified_main_16/...     00001                00001
/modified_main_16/...     UUUUU                UUUUU
/modified_main_16/...     00000                00000
/modified_main_16/...     00000                00000
/modified_main_16/...     01000                01000
/modified_main_16/...     UUUUU                UUUUU
Now                       1200 ns
Cursor 1                  0 ns
```

Fig.11 Simulation Using Model Sim

From the above simulation by generating a and b bits the following operations such as sum of two bits and the selection by using MUX operation and the final results are obtained respectively.

TABLE.3. Comparison of area between the design modulo 2^n-2^k-1 and 2^n-1 adder

Area utilization	2^n-2^k-1	2^n-1
Totalequivalent gate count for design	1,478	3,110
JTAGgate count for IOB	2,352	2,400
Peak memory usage	163 MB	165MB

Hence table 3 illustrates the total area reduction for both the design modulo .

6. CONCLUSION

In this paper the design modulo for novel 2^n-2^k-1 is discussed and proved that the design modulo is more efficient than compared to existing design modulo 2^n-1 respectively. However the speed and efficiency has also been simultaneously increased to make the process convenient. Therefore this design novel modulo is proved efficient to design any sort of adder architectures such as 32 bit and 64 bit respectively. The complete design is verified in VHDL. The basic design of RTL is verified using XILINX tool. . Hence the complete area utilization and optimization are illustrated using synthesis report and the final design is synthesized at SPARTAN-2 of 90nm technology. The reduced no of gates used in MCSA offers better area performance. In future BEC scheme can be illustrated in square root carry select adder to reduce area respectively.

REFERENCES

1. Kuldeep Rawat, Tarek Darwish and Magdy Bayoumi, “A low power and reduced area Carry

Select Adder”, 45th Midwest Symposium on Circuits and Systems, vol.1, pp. 467-470, March2002.

2. Youngjoon Kim and Lee-Sup Kim, “64-bit carry-select adder with reduced area”, Electronics Letters, vol.37, issue 10, pp.614 - 615 , May 2001.
3. B. Ramkumar, Harish M Kittur and P. Mahesh Kannan, “ASIC implementation of Modified Faster Carry Save Adder”, European Journal of Scientific Research, vol.42, pp.53-58, 2010.
4. Israel Koren , “Computer Arithmetic Algorithm”, A.K .Peters, 2nddn, 2002.
5. J. M. Rabaey, “Digital Integrated Circuits- A Design Perspective”, New Jersey, Prentice-Hall, 2001.
6. M. Moris Mano, “Digital Design”, Pearson Education, 3rd edition, 2002.
7. YajuaHe, Chip-Hong Chang and Jiangmin Gu, “An area efficient64-bit square root Carry-Select Adder for low power applications”, IEEE International Symposium on Circuits and Systems,vol.4,pp.4082-4085, May 2005.
8. Behnam Amelifard, Farzan Fallah and Massoud Pedram, “Closing the gap between Carry Select Adder and Ripple Carry Adder: a new class of low-power high-performance adders”, Sixth International Symposium on Quality of Electronic Design, pp.148-152. April 2005.
9. Yuke Wang, C. Pai, and Xiaoyu Song, „‟ The design of hybrid Carry- Look ahead/ Carry–Select Adders‟‟‟, IEEE transaction on Circuits and Systems II: Analog and Digital Processing, vol.49, pp.16-24, January 2002.
10. Youngjoon Kim and Lee-Sup Kim, “A low power carry select adder with reduced area”, IEEE International Symposium on Circuits and Systems, vol.4, pp.218-221, May 2001.
11. T.-Y.Chang and M.-J. Hsiao, “Carry-Select Adder using single Ripple- Carry Adder”, Electronics letters, vol.34, pp.2101-2103, October 1998.
12. D. J. Kinniment, “An evaluation of asynchronous addition”, IEEE transaction on very large scale integration (VLSI) systems, vol.4, pp.137-140, March 1996.
13. Hiroyuki Morinaka, Hiroshi Makino, Yasunobu Nakase, Hiroaki Suzuki and Koichiro Mashiko, “A 64bit Carry Look-ahead CMOS Adder using Modified Carry Select”, Proceeding of IEEE on Custom Integrated Circuits Conference, pp.585-588, May 1995.
14. June Wang, Zhongde Wang, G.A. Jullien and W.C. Miller, ““A real time analysis of Carry Look ahead Adders using enhanced multiple output domino logic”, IEEE International Symposium on Circuits and systems, vol.4, pp.59-62, June 1994
15. Richard P. Brent and H. T. Kung, “A Regular Layout for Parallel Adders”, IEEE transactions on Computers, vol.c-31, pp.260-264, March 1982 Akhilesh Tyagi, “A reduced-area scheme for Carry-Select Adders” , IEEE transaction on Computers, vol. 42, pp.1163-1170, October1993. multiple output domino logic”, IEEE International Symposium on Circuits and systems, vol.4, pp.59-62, June 1994.

16. David Jeff Jackson and Sidney Joel Hannah, “Modelling and Comparison of Adder Designs

with Verilog HDL", 25thSoutheastern Symposium on System Theory, pp.406-410, March1993.

17. Akhilesh Tyagi, "A Reduced Area Scheme for Carry-Select Adders", IEEE International Conference on Computer design, pp.255-258, Sept 1990.
18. Belle W.Y.Wei and Clark D.Thompson, "Area-Time Optimal Adder Design", IEEE transactions on Computers, vol.39, pp. 666-675, May1990.
19. O. J. Bedrij, "Carry-Select Adder", IRE transactions on Electronics Computers, vol.EC-11, pp. 340-346, June1962.