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HIGH SPEED VEDIC MULTIPLIER DESIGNS

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ABSTRACT
Multipliers are the key block in high speed arithmetic logic units, multiplier and accumulate units, digital signal processing units etc. With the increasing constraints on delay, more and more emphasis is being laid on design of faster multiplications. To enhance speed many modifications over the standard modified booth algorithm, Wallace tree methods for multiplier design have been made and several new techniques are being worked upon. Amongst these Vedic multipliers based on Vedic mathematics are presently under focus due to these being one of the fastest and low power multiplier. There are sixteen sutras in Vedic multiplication in which "Urdhva Tiryakbhyam" has been noticed to be the most efficient one in terms of speed. A large number of high speed Vedic multipliers have been proposed with Urdhva Tiryakbhyam sutra. Few of them are presented in this paper giving an insight into their methodology, merits and demerits. Compressor based Vedic Multipliers show considerable improvements in speed and area efficiency over the conventional ones.

INTRODUCTION
Vedic multipliers are based on Vedic Sutras. In Sanskrit word 'Veda' stands for 'knowledge'. Vedic mathematics is believed to be reconstructed from Vedas by Sri Bharti Krishna Tirathaji between the years 1911 to 1918 [1]. The Vedic mathematics has been divided into sixteen different Sutras which can be applied to any branch of mathematics like algebra, trigonometry, geometry etc. Its methods reduce the complex calculations into simpler ones because they are based on methods similar to working of human mind thereby making them easier. It has been seen that being coherent and symmetrical, they consume lesser power and acquire lower chip area [1]. Designs based on Vedic Mathematics have been used in many applications like ALU, MAC etc. and have shown better results [2-6]. ultiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation-Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit [1]. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [2]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications [2,3]. This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital

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systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, area and power consumption. The multiplier is afairly large block of a computing system. The amount of circuitry involved is directlyproportional to the square of its resolution i.e. A multiplier of size n bits has n2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation. That‟s why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations.Digital multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers[11]. Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. The computation time taken by the array multiplier is comparatively less because the partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array. Booth multiplication is another important multiplication algorithm. Large booth arrays are required for high speed multiplication and exponential operations which in turn require large partial sum and partial carry registers. Multiplication of two n-bit operands using a radix-4 booth recording multiplier requires approximately n / (2m) clock cycles to generate the least significant half of the final product, where m is the number of Booth recorder adder stages. Thus, a large propagation delay is associated with this case. Due to the importance of digital multipliers in DSP, it has always been an active area of research and a number of interesting multiplication algorithms have been reported in the literature..

VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical

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explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive rese arch in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful [2, 3].The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here.The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing [1,4].The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial-parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

The method can be extended for binary numbers. A simple 1-digit binary multiplication is described by AND gate operation. Using this and UT method 2X2 multiplication for a1a0 and b1b0 is implemented by 2 half adders and resultant bits are r2 (2 bits) r1r0 as shown in Fig. 3. The equations regarding this are given below.

r0 (1bit) = a0b0 (1)
r1 (1bit) =a0b1 +a1b0 (2)
r2 (2bit) = b1a1 +c1 (3)
Product = r2&r1&r0 (4)

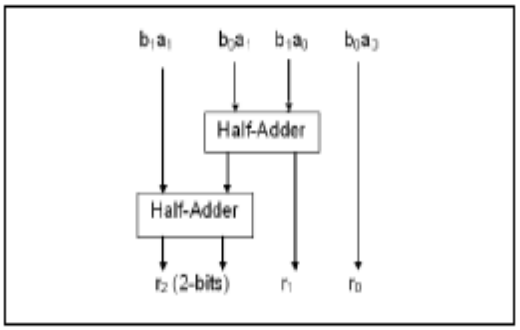

Fig.1 Block diagram for 2X2 Vedic Multiplier

LOW POWER AND HIGH SPEED VEDIC MULTIPLIER

Fast and low power 16-bit multiplier architecture was proposed by R.K, R.S, S. Sarkar, and Rajesh [15] replacing ripple carry adder with the carry Look ahead adder as in Fig 8. The adder architecture consisted of two parts- Carry generator and Carry propagator. These parts generates the N+1th carry bit with

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the help of the initial carry and thus this does not need to wait for Nth carry to propagate. Since the carry is generated in advance in this adder, it decreases the carry propagation time and thus this architecture improves the operational speed. Fig. 9(c) shows tree like circuit for CLA for n=8 which consists of A and B modules. [14] A module in Fig 9a gives pi (*i*th carry propagate) and gi (*i*th carry generate) and sum bits outputs for Ai and Bi inputs. B Module in Fig 9b gives Block carry propagate, Block carry generate and carry bits which are used for large i values. The worst propagation delay for n-bit CLA is two unit delays2 of the A-module + 2 log2n -1 unit delays of the B-module. The power dissipated and propagation delay time is 0.17 mW and 27.15 ns respectively. A comparison of propagation delay, power dissipation and the number of transistors, made between this architecture, Array multiplier and the Booth radix 4 multiplier, shows that the Vedic multiplier with carry Lookahead adder is better than the other two in speed and power dissipation. But the number of transistors used increases in the proposed architecture.

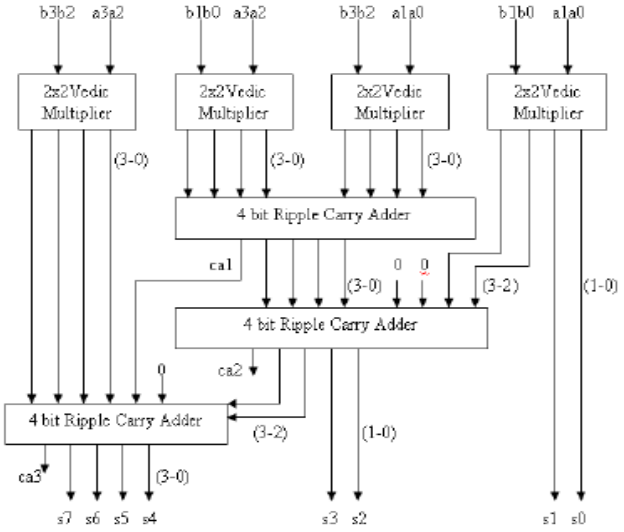

Fig.2. Block diagram for 4x4 Vedic multiplier using ripple carry adder.

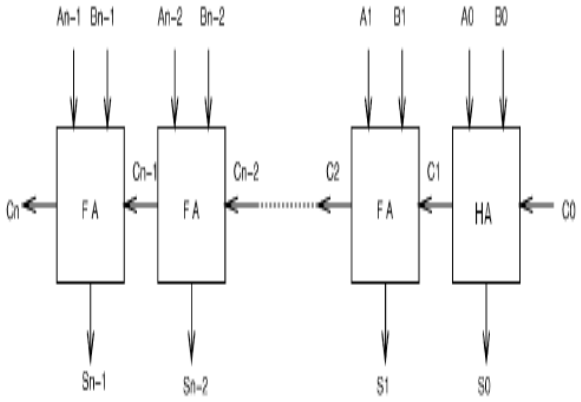

Fig. 7 Ripple carry adder

FAST VEDIC MULTIPLIER USING CARRY SAVE ADDER.

An effective design in speed had been proposed by Devika, Kabiraj and Rutuparna [9] for 8 and 16-bit multiplication. In this architecture, Adder Unit used is carry save. A MAC design implemented using this architecture, has shown better results Figure 10 depicts a block diagram for 4-bit Vedic multiplier with carry save adder. For N-bit multiplication, it requires N-bit carry save adder and N+1 bit Ripple carry adder. The carry save adder is used to add three or more N bit operands by generating the output of two N bit numbers in two sequences. One is having the N bit partial addition results and another is having the set of carry bits. Then a normal adder, generally Ripple carry adder is used to add these sets for the generation of final output. Unlike common adders like ripple carry adder, carry look ahead adder this adder does not has any carry propagation and has the propagation delay of am single full adder and delay does not change with the number of bits (n). Therefore for sufficiently large value of n, it is faster and smaller in size. Fig 11 a. depicts n bit CSA which uses n full adders and produces n bit sum 'S' and n bit carry 'C'.

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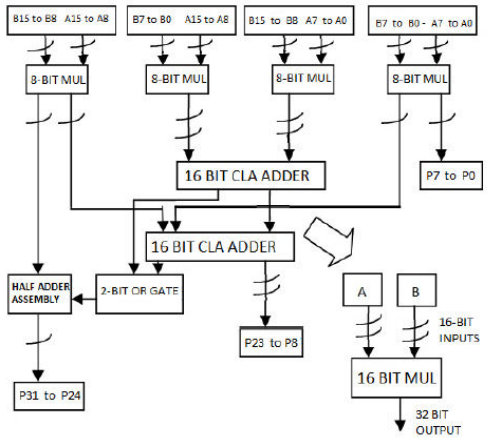

Fig. 3 Block diagram for 16-bit Vedic multiplier with CLA adder

VEDIC MULTIPLER USING MODIFIED CSA

A high speed and low power 16×16 Vedic Multiplier is designed by using low power andhigh speed modified carry select adder. Modified Carry Select Adder employ s a newly incremented circuit in the intermediate stages of the Carry Select Adder (CSA) which is known to be the fastest adder among the conventional adder structures. A Novel technique for digit multiplication namely Vedic multiplication has been introduced which is quite different from normal multiplication by shift and addition operations. Normally a multiplier is a key block in almost all the processors and also introduces high delay block and also a major power dissipation source. This paper presents a new design methodology for less delay and less power efficient Vedic Multiplier based up on ancient Vedic Mathematic techniques. For clear understanding, observe the block diagrams for 16x16 as shown in Figure8 and within the block diagram 16x16 totally there are four 8x8 Vedic multiplier modules, and three modified carry select adders which are of 16 bit size are used. The 16 bit modified carry select adders are used for addition of two 16 bits and likewise totally four are use at intermediate stages of multiplier.

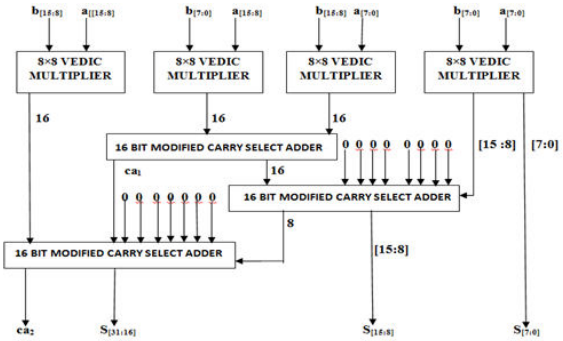

Fig.4 Block diagram for 4 bit multiplier using carry save adder

CONCLUSION AND FUTURE SCOPE

Vedic Multiplier is seen to be efficient in speed, power and area in digital designs with respect to other multipliers. Considering all the designs of it discussed above, we can conclude that the Compressor based Vedic multiplier with Urdhva Tiryakbhyam sutra is seen as a promising technique in terms of speed and area. The work can be further extended with the use of such multiplier in arithmetic logical unit, multiply accumulator unit designs and comparing the results with existing designs for the same.

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