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IMPLEMENTATION OF HIGH EFFICIENT THROUGHPUT AND LOW POWER DESIGN FOR HIGH ORDER FILTER USING DISTRIBUTED ARCHITECTURE

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ABSTRACT:

This paper presents the use of Distributed Arithmetic (DA) technique for implementing the design of raised cosine Finite Impulse Response (FIR) filter with modified coefficients. The filter impulse response is represented with a minimum number of non-zero coefficients through the use of a modification and optimization algorithm. The motivation behind using this algorithm with DA technique is that the number of computation alarithmetic, the addition operation, needed to get the filter out put is reduced to the maximum limit so that it doesn't affect the performance of Next Wireless generations system. The application of DA technique to design the modified filters coefficients results in a powerful design with high speed and much less area when compared with implementing the same filters with their original coefficients

1. INTRODUCTION:

The signal is mainly affected by the strong noise in digital Communication. So, the receiver system must have the capability to reduce this noise before decoding. Hence Matched Filters are used to maximize the SNR at the receiver. Matched filter is used in many areas, such as radar and image processing to improve SNR. The matched filter and pulse compression concepts are the basic of radar processing algorithms. Since radar return is always susceptible to noise and interference from all kinds of objects illuminated by the antenna beam, the receiver must be optimized. Pulse Compression involves using a matched filter to compress the energy in a signal into a relative narrow pulse. Pulse compression is the classical signal processing techniques to increase the range resolution of transmitted pulse without having to increase the peak transmit power. The LFM, or chirp waveform, has superior performance in pulse compression radar since they can be easily generated and processed.

Many diverse techniques and devices have been developed to provide the required pulse compression processing for these signals. However, the LFM has large side lobes with respect to the main lobe. Reducing the side lobes can be accomplished by linear filtering the output, i.e. applying window functions which are known as the spectrum weighting. The Distributed Arithmetic (DA) based higher order Matched FIR filter is implemented. For FIR filters, output is a linear convolution of weights and inputs.

Purpose:

To design an Nth-order FIR filter, the generation of each output sample takes N+1 multiply accumulate (MAC) operations. Multiplication is strongest operation because it is repeated addition. It requires large portion of chip area. Power consumption is more. Memory-based structures are more regular compared with the multiply

accumulate structures; and have many other advantages.

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Memory based structures are well-suited for many digital signal processing (DSP) algorithms, which involve multiplication with a fixed set of coefficients. For this Distributed Arithmetic architecture used in FIR filter. Distributed arithmetic is one way to implement convolution with multiplier less unit, where the MAC operations are replaced by a series of LUT access and summations. Basically, each look up table is a bunch of single bit memory cells storing individual bit values in each of the cells. Distributed Arithmetic provides cost-effective and area-time efficient computing structures.

2. MATCHED FILTER

A matched filter is a filter whose frequency response is designed to exactly match the frequency spectrum of the input signal. The operation of matched filters are the same as correlating a signal with a copy of itself. These filters are used as signal processors in communications receivers to calculate the correlation between the transmitted signal and the received signal. In signal processing, a matched filter is obtained by correlating a known signal, or template, with an unknown signal to detect the presence of the template in the unknown signal.

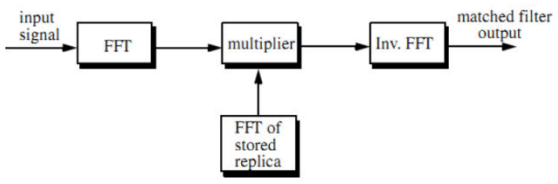

Figure1: Representing the Block Diagram of Matched Filter

This is equivalent to convolving the unknown signal with a conjugated time-reversed

version of the template. The matched filter is the optimal linear filter for maximizing the signal to noise ratio (SNR) in the presence of additive stochastic noise. Matched filters are commonly used in radar, in which a known signal is sent out, and the reflected signal is examined for common elements of the out-going signal.

To design such a filter, IIR or FIR digital filters can be employed [3]. By contrast to IIR filter, FIR filter generally has Linear-phase though it needs more memories and arithmetic operations while it is implemented. Thus, FIR is proposed to design matched filters because FPGA device has enough memories and logic elements (LE).

3. OVERVIEW TO WIRELESS MOBILE TECHNOLOGY:

The GSM family of technologies has provided the world with mobile communications since 1991. In over twenty years of development, GSM has been continually enhanced to provide platforms that deliver an increasingly broad range of mobile services as demand grows. Where the industry started with plain voice calls, it now has a powerful platform capable of supporting mobile broadband and multimedia services.

GSM is now used in 219 countries and territories serving more than three billion people and providing travellers with access to mobile services wherever they go.

GSM

An open, digital cellular technology used for transmitting mobile voice and data services

GPRS

A very widely deployed wireless data service, available now with most GSM networks

EDGE

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GSM Evolution (EDGE) technology provides up to three times the data capacity of GPRS

WCDMA

The air interface for one of the International Telecommunications Union's family of third-generation (3G) mobile communications systems.

HSPA

The set of technologies that enables operators to upgrade their existing 3G/WCDMA networks to carry more traffic and at faster speeds.

LTE

Designed to be backwards-compatible with GSM and HSPA, Long Term Evolution uses the OFDMA air interface, in combination with other technologies, to offer high throughput speeds and high capacity.

3.1 Importance of DA with High order filter in Wireless Technology:

The information transmitted through 4G WCDMA wireless systems will have a higher delay spread so the symbols tends to interfere which is called as inter symbol interference. Inter- symbol Interference (ISI) is an unavoidable consequence in wireless communication systems. Particularly in 4G systems with data rateat 100 Mbps interference of symbols are prone to occur. The main problem in 4G is that energy, which we wish to confine to one symbol, leaks into others due to high data rate.The simplest method, to reduce ISI is to slow down the signal transmission by introducing delay between multiple bits. The solution to counter ISI is pulse shaping, Root Raised

Cosine Filtering is one of the methods for pulse shaping.The following paper shows how the Root raised cosine filter can be implemented on hardware using the Distributed Arithmetic Algorithm.

3.2 Implemented Block Diagram:

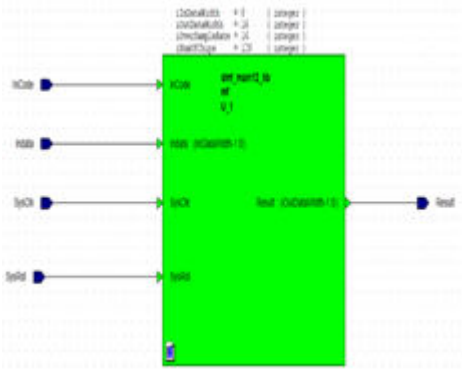


Figure 2: Representing the Interface Block Unit of Matched Filter in HDL designer series

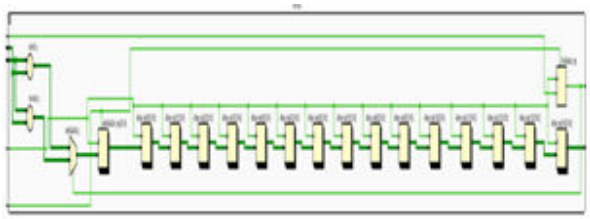
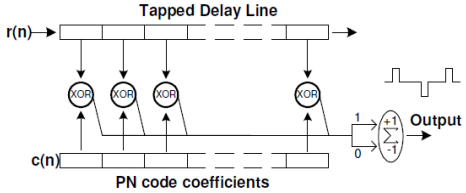


Figure 3: Representing the Schematic View for the block Diagram

3. IMPLEMENTATION OF DIGITAL MATCHED FILTER:

3.1 Existing Method's:

Digital Matched Filter Using PN sequence generation:



Consider the above diagram, which is proposes a system that involves the

implementation convolutions with respect to impulse response of the filter hence resulting a finite impulse response structure which convolves the tap coefficient sequence c(n), with the spread received sequence r(n) As the r(n) sequence slides through the tapped delay line, the asynchronous multiply and accumulate process calculates the correlation value. Thus, a new correlation value is calculated at each chip interval. The polarity of the correlation peak, determines the polarity of the de-spread data symbol.

The ideal matched filter considers an input stream of ±1. In the digital implementation of this system, the input sequence is a stream of zeros and ones. Thus, the proposed design uses XOR operations in the place of multiplications. Further, as illustrated by Figure 3, the accumulate process is altered so as to reproduce the bipolar correlation output that would result if ±1 inputs were used. The symbol-length PN code used was a 16 bit random sequence generated by MATLAB. Given a nominal data over-sampling rate of 16, a 256-tap DMF was needed. This was accomplished with the use of a 256-bit static register that holds over-sampled PN sequence, a 256 bit shift register to hold the data, 256 XOR gates, and a 256 bit parallel adder. The shift register used to shift in the input data could be reused in all of the DMF instantiations.

The output range of the 256- tap DMF is {-256, 256}. Large positive or negative correlation values signify the reception of a valid symbol. Thus, it can be intuitively justified to state that if a random sequence uncorrelated with the PN sequence were input to the DMF, the correlation value would be around zero. Since the input is random, it is fair to guess that half of the 256 XOR operations would result in high outputs and the rest in low outputs. An equal number of zeros and ones result in a zero output according to the scheme of Figure above.

3.2 Generation of Matched Filter Using Pulse Compression:

The pulse compression block is the first stage of the signal processing chain. At the input of the module, the received signal is very noisy and almost looks like white noise. The pulse compression technique tries to make the transmitted signal visible and dominant over the background noise. Unlike the pulses depicted in figure .1, the transmitted signal does not consist of basic rectangular-like pulses with constant amplitude and duration τ. The main reason is due to electromagnetic laws that do not permit low-frequencies signal to be sent over the air. Therefore, there is a need to shift the signal on a carrier signal. Moreover, the system generates internal noise. The noise power decays in 1/f. Thus, system self-generated noise is inversely proportional to the frequency. This gives a second good reason to use a carrier signal to transmit the signal. A basic quadratic demodulator recovers the signal from the RF modulation. The detected signal is shifted back to the baseband domain. Using a specific receiving filter, the output produces a triangular-like signal which maximum value leads to the target range. [2][3]

3.3 PRINCIPLE OF COMPRESSION

Pulse Compression is involved in radar systems where both maximum detection range and range discriminator factor are of importance. We know that maximum detection range Rmax is proportional to the pulse duration τ and the range discriminator factor d is and is must be minimized to ensure

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multiple targets detection. One first idea could be to increase the peak power while keeping the pulse duration to a low value, thus increasing the maximum range detection. However, due to hardware constraints, this solution is not feasible. The most popular solution consists in the use of particular pulses, called compressed pulses. Compressed pulses are pulses that have the particularity to have a non-zero duration T at Transmitting point such that T>>τ. At the receiving point, their duration is set back to τ after filtering. We define

$$\rho = T/\tau \qquad \ldots\ldots..1$$

as the compression rate. Basic rectangular pulses on a carrier do not allow such results. It is necessary to add a modulation or coding scheme on the signal phase. The most popular coding scheme is the so-called chirp scheme.

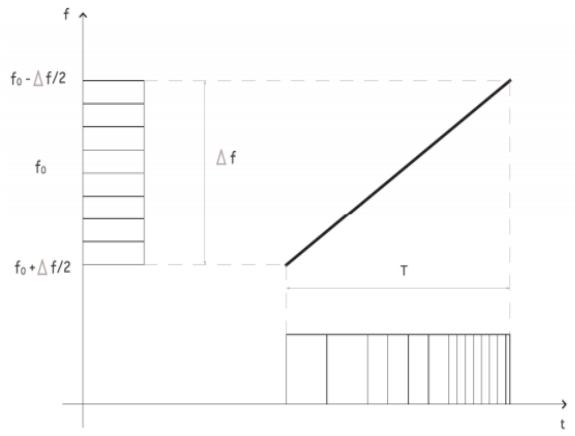

Figure: Representing the Pulse Compression Principle

4. Proposed Design for Distributed Athematic in Matched Filters

4.1 Distributed arithmetic

Distributed Arithmetic is a popular architecture for implementing FIR filters without the use of multipliers. DA realizes the sum of products computation required for FIR filters efficiently using LUTs, shifters and adders. Since these operations map efficiently onto an FPGA, DA is a favoured architecture on these devices. Distributed Arithmetic (DA) is a well-known method to save resources in multiply-and-accumulate structures (MACs) implementing DSP functions. DA trades memory for combinatory elements, resulting in ideal-to-implement custom DSPs (CDSPs) in LUT-based FPGAs. In addition to a DA implementation, the designer also can select from a bit-serial to a full-parallel implementation to trade bandwidth for resource utilization. Cascade and lattice structures present several interesting properties such as low quantification error and high stability in the filter coefficients. Moreover, you can expand lattice cells without a full redesign. The goal of this article is to implement FPGA-based direct-form, cascade, and lattice high-order FIR filters using bit-serial DA. We start by comparing the resultant topologies in both area and speed. The designs use an HDL to include pipeline techniques and scalable parameters. We also describe DA error models of the three structures. The next section reviews DA fundamentals and proposed architectures for each kind of filter. This article also presents the results of the FPGA implementation of the structures and discusses an error model for the filter structures.

4.1.1 Design the Filter

Use a sampling rate of 48 kHz, passband edge frequency of 9.6 kHz and stop frequency of 12k. Set the allowable peak-to-peak passband ripple to 1 dB and the stopband attenuation to -90 dB. Then, design the filter using

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fdesign.lowpass, and create the double-precision filter as a direct form FIR filter.

4.1.2 Quantize the Filter

Since DA implements the FIR filter by serializing the input data bits, it requires a quantized filter. Assume that 12-bit input and output word lengths are required (due to of fixed data path requirements or input ADC/output DAC widths). Quantize the filter and adjust the word lengths to the desired lengths.

4.1.3 Generate HDL Code with DA Architecture

For a filter with many taps it is best to divide the taps into a number of LUTs, with each LUT storing the sum of coefficients for only the taps associated with it. The sum of the LUT outputs is computed in a tree structure of adders.

4.1.4 Conversion of the Filter Structure

Quantize this new filter and generate HDL code on the new filter.

4.1.5 DA-Radix

The default architecture is a Radix 2 implementation, which operates on one bit of input data on each clock cycle. The number of clock cycles elapsed before an output is obtained is equal to the number of bits in the input data. Thus, DA can potentially limit the throughput. To improve the throughput of DA, you can configure DA to process multiple bits in parallel. The 'DARadix' property is provided for this purpose.

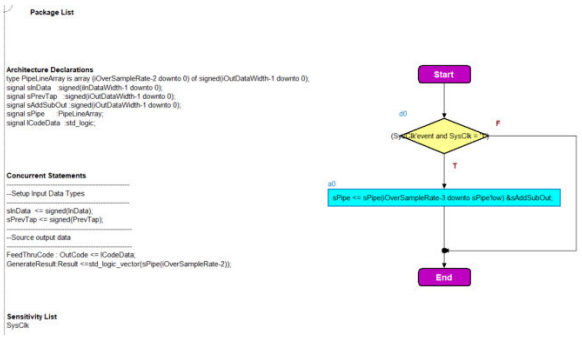
For example, you can set 'DARadix' to 2^3 to operate on 3 bits in parallel. For a 12 bit input word length, you can specify processing of 1, 2, 3, 4, 6 or 12 bits at a time by specifying corresponding 'DARadix' values of 2^1, 2^2, 2^3, 2^4, 2^6, or 2^12 respectively.

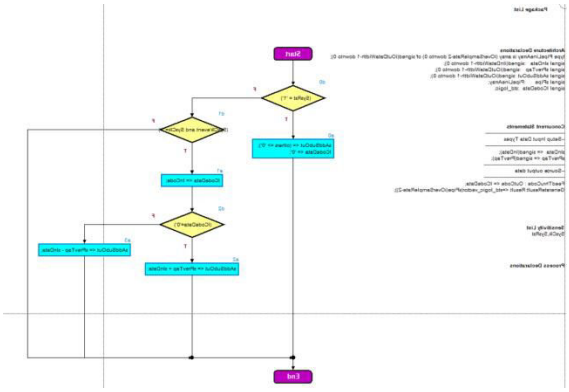
In selecting different 'DARadix' values, you trade off speed vs. area within the DA architecture.

The number of bits operated in parallel determines the factor by which the clock rate needs to be increased.

This is known as folding factor. For example, the default 'DARadix of 2^1, implying 1 bit at a time, results in a clock rate 12 times the input sample rate or a folding factor of 12. A 'DARadix' of 2^3 results in a clock rate only 4 times the input sample rate, but requires 3 identical sets of LUTs, one for each bit being processed in parallel.

4.2 Flowchart for Distributed Architecture in Higher Order Filter Design





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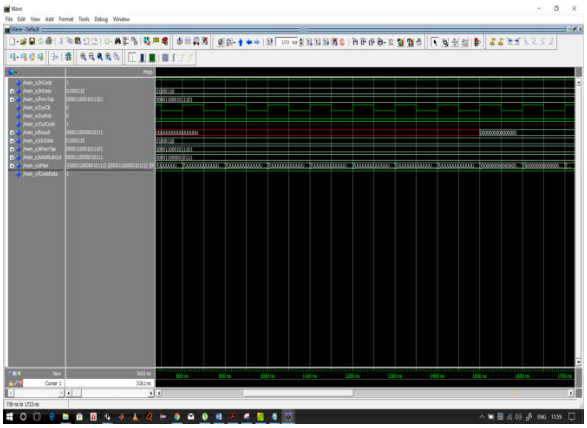
5. RESULTS AND DISCUSSION OF MATCHED FILTER USING DISTRIBUTEDARCHITECTURE:



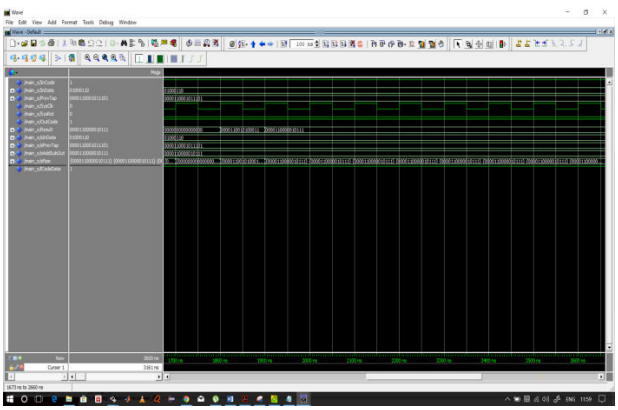
Here we could observe the design Simulation phase where each of the data is being simulated with respect to the selected or desired input. As we know that the Simulation phase requires a test vector inputs which could be analysed as shown below:

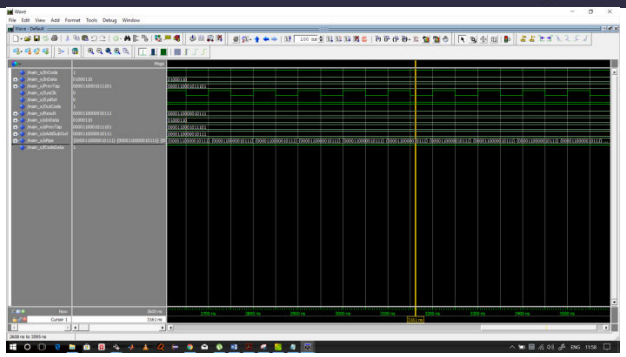
Initial Phase:

SysRst = '1';

InCode = '1'; %%%Assume for the reset condition and single run.

sPipe<= sPipe(iOverSampleRate-3 downtosPipe'low) &sAddSubOut; %%% this statement provides the matched filter condition for which we are designing specific filter with n-tap analysis reducing the accumulated power for overall design.





XILINX Results:

Power and Synthesis Results:

1. Summary

Total On-Chip Power (W)	1.376
Dynamic (W)	1.037
Device Static (W)	0.339
Effective TJA (C/W)	1.4
Max Ambient (C)	83.1
Junction Temperature (C)	26.9
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)

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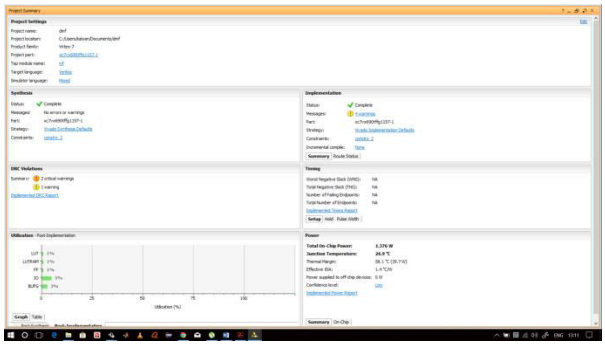
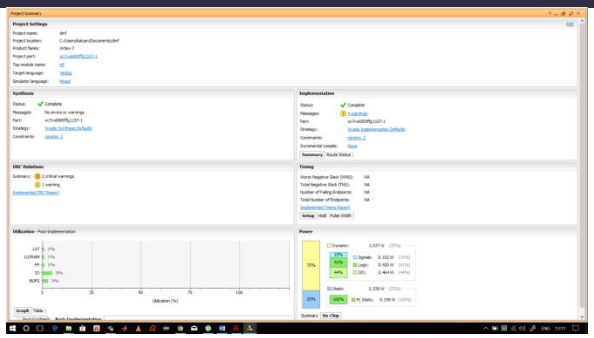
Slice Logic	0.420	9089	---	---
LUT as Logic	0.331	2048	433200	0.47
CARRY4	0.088	512	108300	0.47
BUFG	<0.001	1	32	3.13
Register	<0.001	4224	866400	0.49
Others	0.000	256	---	---
LUT as Shift Register	0.000	1024	174200	0.59
Signals	0.152	4620	---	---
I/O	0.464	27	600	4.50
Static Power	0.339			
Total	1.376			





CONCLUSION:

This paper is designed with the receiver system with matched filter is simulated in HDL design Series (Mentor Graphics). Matched filtering of the Linear Frequency Modulated (FM) waveform is done with and without spectrum weighting. The Distributed Arithmetic (DA) based higher order Matched FIR filter is implemented in VHDL which isan important step in receiving a synchronized data fornew generation cellular mobile systems. The main designfeatures of the proposed system are the configurabilityand flexibility. A simple implementation of the tap usedin the matched filter is presented. The designedcomponent is software implemented using Virtex-E andproved to work successfully.We have implemented and verified the different higher order matched filter on FPGA chip to reduce the power handling capabilities.

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