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Improved Grid Voltage Synchronization Algorithm for Distributed Generation Systems under Grid Fault Conditions

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ABSTRACT:

The real framework code necessities for the lattice association of circulated era frameworks, fundamentally wind and photovoltaic (PV) frameworks, are turning out to be exceptionally requesting. The transmission framework administrators (TSOs) are particularly concerned about the low-voltage-ride-through necessities. Arrangements based on the establishment of STATCOMs and element voltage controllers (DVRs), and in addition on cutting edge control functionalities for the existing force converters of circulated era plants, have added to improve their reaction under flawed and mutilated situations and, henceforth, to satisfy these necessities. Keeping in mind the end goal to accomplish attractive results with such frameworks, it is important to rely on exact and quick network voltage synchronization calculations, which can work under lopsided and misshaped conditions. This paper investigates the synchronization capacity of three propelled synchronization frameworks: the decoupled twofold synchronous reference outline stage bolted circle (PLL), the double second request summed up integrator PLL, and the three-stage upgraded PLL, intended to work under such conditions. Despite the fact that different frameworks taking into account recurrence bolted circles have likewise been created, PLLs have been picked because of their connection with dq0 controllers. In the accompanying, the diverse calculations will be exhibited what's more, discretized, and their execution will be tried in an trial setup controlled with a specific end goal to assess their exactness what's more, usagecomponents.

Keywords: PV, TSOs, STATCOMs, DVRs, PLL.

I. INTRODUCTION

The power share of renewable energy-based generation systems is supposed to reach 20% by 2030, where wind and photovoltaic (PV) systems are assumed to be the most outstanding examples of integration of such systems in the electrical network. The increased penetration of these technologies in the electrical network has reinforced the already existing concern among the transmission system operators (TSOs) about their influence in the grid stability; as a consequence, the grid connection standards are becoming more and more restrictive for distribution generation systems in all countries In the actual grid code requirements (GCRs), special constraints for the operationof

such plants under grid voltage fault conditions have gained a great importance. These requirements determine the fault boundaries among those through which a grid-connected generation system shall remain connected to the network, giving rise to specific voltage profiles that specify the depth and clearance time of the voltage sags that they must withstand. Such requirements are known as low voltage ride through (LVRT) and are described by a voltage versus time characteristic.

Although the LVRT requirements in the different standards are very different, as shown in

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[8], the first issue that generation systems must afford when a voltage sag occurs is the limitation of their transient response, in order to avoid its protective disconnection from the network. This is the case, for instance, of fixed speed wind turbines based on squirrel cage induction generators, where the voltage drop in the stator windings can conduct the generator to an over speed tripping, as shown in Likewise, variable speed wind power systems may lose controllability in the injection of active/reactive power due to the disconnection of the rotor side converter under such conditions. Likewise, PV systems would also be affected by the same lack of current controllability. Solutions based on the development of auxiliary systems, such as STATCOMs and dynamic voltage regulators (DVRs), have played a decisive role in enhancing the fault ride through (FRT) capability of distributed generation systems, as demonstrated in Likewise, advanced control functionalities for the power converters have also been proposed. In any case, a fast detection of the fault contributes to improving the effects of these solutions; therefore, the synchronization algorithms are crucial.

II. GRIDSYNCHRONIZATION

In an alternating current electric power system, synchronization is the process of matching the speed and frequency of a generator or other source to a running network. An AC generator cannot deliver power to an electrical grid unless it is running at the same frequency as the network. If two segments of a grid are disconnected, they cannot exchange AC power again until they are brought back into exact synchronization. A direct current (DC) generator can be connected to a power network by adjusting its open- circuit terminal voltage to match the network voltage, by either adjusting its speed or its field excitation. The exact engine speed is not critical. However, an AC generator must match both the amplitude and the timing of the network voltage, which requires both speed and excitation to be systematically controlled for synchronization. This extra complexity was one of the arguments against AC operation during the War of Currents in the 1880s. In modern grids, synchronization of generators is carried out by automatic systems. There are five conditions that must be met before the synchronization process takes place. The source (generator or sub-network) must have equal line voltage,frequency,phase sequence,phase angle, and waveform to that of the system to which it is being synchronized.[1]Waveform and phase sequence are fixed by the construction of the generator and its connections to the system. During installation of a generator, careful checks are made to ensure the generator terminals and all control wiring are correct so that the order of phases (phase sequence) matches the system. Connecting a generator with the wrongphase sequence will result in a short circuit as the system voltages are opposite to those of the generator terminal voltages.[2]

The voltage, frequency and phase angle must be controlled each time a generator is to be connected to a grid.[1]Generating units for connection to a power grid have an inherent droop speed control that allows them to share load proportional to their rating. Some generator units, especially in isolated systems, operate with isochronous frequency control, maintaining constant system frequency independent of load. Formerly, three light bulbs were connected between the generator terminals and the system terminals (or more generally, to the terminals of instrument transformers connected to generator and system). As the generator speed changes, the lights will flicker at the beatfrequency proportional to the difference between generator frequency and system frequency. When the voltage at the generator is opposite to the system voltage (either ahead or behind in phase), the lamps will be bright. When the voltage at the generator matches the system voltage, the lights will be dark. At that

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instant, the circuit breaker connecting the generator to the system may be closed and the generator will then stay in synchronism with the system.[3]An alternative technique used a similar scheme to the above except that the connections of two of the lamps were swapped either at the generator terminals or the system terminals. In this scheme, when the generator was in synchronism with the system, one lamp would be dark, but the two with the swapped connections would be of equal brightness. Synchronizing on "dark" lamps was preferred over "bright" lamps because it was easier to discern the minimum brightness. However, a lamp burnout could give a false-positive for successful synchronization.

SYNCHROSCOPE: Another manual method of synchronization relies on observing an instrument called a "synchroscope", which displays the relative frequencies of system and generator. The pointer of the synchroscope will indicate "fast" or "slow" speed of the generator with respect to the system. To minimize the transient current when the generator circuit breaker is closed, usual practice is to initiate the close as the needle slowly approaches the in-phase point. An error of a few electrical degrees between system and generator will result in a momentary inrush and abrupt speed change of the generator. Three types synchronization Systems are

A. Phase LockedLoops

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phasedetector.

B. Automobile RaceAnalogy

For a practical idea of what is going on, consider an auto race. There are many cars, and the driver of each of them wants to go around the track as fast as possible. Each lap corresponds to a complete cycle, and each car will complete dozens of laps per hour. The number of laps per hour (a speed) corresponds to an angular velocity (i.e. a frequency), but the number of laps (a distance) corresponds to a phase (and the conversion factor is the distance around the track loop).

C. ClockAnalogy

Phase can be proportional to time, so a phase difference can be a time difference. Clocks are, with varying degrees of accuracy, phase-locked (time-locked) to a master clock. Left on its own, each clock will mark time at slightly different rates. A wall clock, for example, might be fast by a few seconds per hour compared to the reference clock at NIST. Over time, that time difference would become substantial.

III. DISCRETEIMPLEMENTATION

The performance of the different structures under test is really dependent on their final digital implementation, particularly on the discretization approach made to their

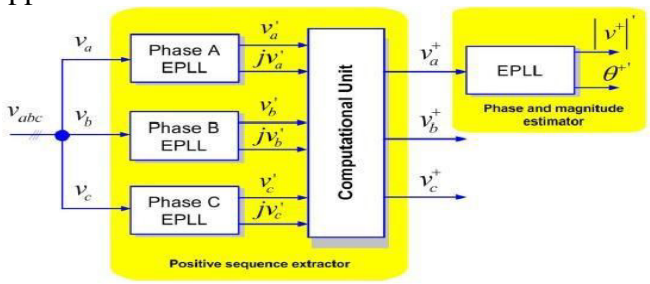

Fig.1. phEPLL Block Diagram.

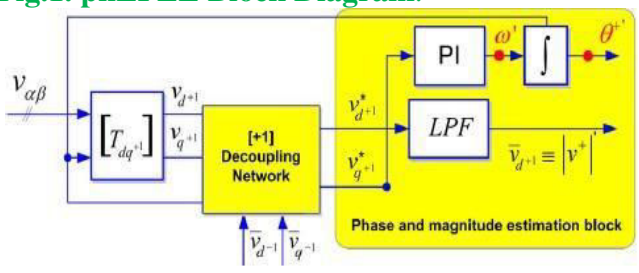

Fig.2. Phase and Magnitude Estimation Loop of the DDSRF PLL.

continuous equations. This implementation is critical

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and should be studied in detail as a straightforward implementation can give rise to additional delays in the loop that hinder the good performance of the PLL. Some methods, such as the forward Euler, the backward Euler, and the Tustin (trapezoidal) numerical integration, offer a good performance when used for discretizing other synchronization systems, as shown in and . However, Euler methods can be inadequate under certain conditions, due to the need of introducing additional sample delays. Therefore, according to the specific needs of the presented topologies, this section will describe the discrete representation of each PLL individually. In order to facilitate the comprehension of the process, the different building blocks that appear at Figs. 3–5 will be referenced. The values of the different parameters used in each case are summarized in the Appendix.

A. DDSRF-PLLDiscretization

The discrete model of this PLL can be easily obtained since the continuous representation of several parts does not change in the discrete domain. This is the case for the transformation blocks $T\alpha\beta$, $Tdq+1$, and $Tdq-1$, whose description can be found in general scope literature.

1. Positive- and Negative-Sequence Decoupling Networks

The decoupling network constitutes one of the mostimportant contributions of this synchronization method. Thediscrete equations of these blocks are shown in (1), being almost the same as in the continuous domain [41]. It is just necessary to consider one sample delay of $\theta\_$, $—vd-1$, $— vq-1$, $—vd+1$, and $—vq+1$ in order to avoid algebraic loops.

2, Phase and Magnitude Estimator Discretization

In the DDSRF PLL, the decoupling network appears embedded in the classical SRF-PLL loop (see Fig. 6). However, this does notaffect the discretization of the phase and magnitude estimator since $v* d+1$ and $v* q+1$ act as the input of this block

$$\begin{bmatrix} v_{d+1}^{*}[n+1] \\ v_{q+1}^{*}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d+1}[n+1] \\ v_{q+1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d-1}[n] \\ \bar{v}_{q-1}[n] \end{bmatrix} \quad (1)$$

$$\times \begin{bmatrix} v_{d-1}^{*}[n+1] \\ v_{q-1}^{*}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d-1}[n+1] \\ v_{q-1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d+1}[n] \\ \bar{v}_{q+1}[n] \end{bmatrix}$$

The discrete controller and the integrator can be built using a backward numerical approximation. The frequency and phase can then be represented in the z-domain (2), considering $v* q+1$ as the error to be minimized. In this equation, a feed forward of the nominal frequency is given by means ofωff

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V_{q+1}^{*}(z) + \omega_{ff}$$

$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (2)$$

Finally, sample-based representation gives rise to (3), which are the expressions to be implemented

$$\omega'[n+1] = \omega'[n] - k_p \cdot v_{q+1}^{*}[n] + (k_p + k_i \cdot T_s) \cdot v_{q+1}^{*}[n+1]$$

$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1]. \quad (3)$$

In these equations, a frequency feed forward has been introduced as an initial condition to $\omega\_$.

3. LPF Block Discretization

The amplitudes of the dqpositive- and negative-sequence components are the outputs of the decoupling networks. However, four infinite impulse response (IIR) LPFs extract the ripple from each sequence estimation in order to reinforce the performance of the PLL in case of harmonic pollution. A first-order filter with a cutoff frequency ωf, equal to half of the grid frequency, was originally proposed in hence, the same transfer function has been implemented in this paper for evaluation purposes in

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$$y[n] = \frac{1}{T_s \cdot \omega_f + 1} \cdot x[n] + \frac{T_s \cdot \omega_f}{T_s \cdot \omega_f + 1} \cdot u[n]$$
$$x[n+1] = y[n] \qquad (4)$$

B. DSOGI-PLLDiscretization

1. Dsogi-Qsg BlockDiscretization

As was previously mentioned in Section II, the DSOGI-based quadrature signal generator (QSG) of Fig. 4 consists of two independent and decoupled second-order generalized integrators (SOGIs). Therefore, each SOGI-based quadrature signal generator can be discretized individually, thus facilitating its mathematical description. In Fig. 3, the block diagram of the implemented SOGI is shown.

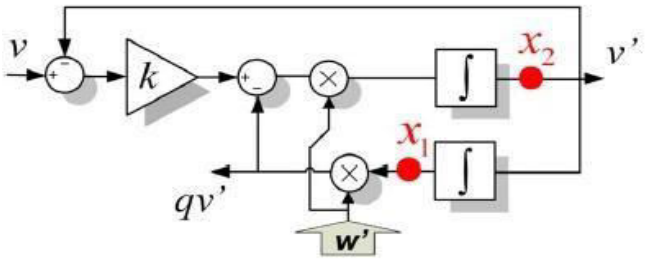

Fig.3. Quadrature Signal Generator Based on a Second Order Generalized Integrator (SOGI QSG).

This quadrature signal generator (QSG) is a linear system itself; therefore, a discrete representation can be systematically obtained if the continuous state space is previously deducted. The equations of the SOGI state space appear detailed in (5). where*v* constitutes the input while *v*_ and *qv*_ are the two inquadrature output signals

$$\left.\begin{aligned}\dot{x}_n &= A \cdot x_n + B \cdot v \\ y_n &= C \cdot x_n\end{aligned}\right\}; \quad x_n = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad y_n = \begin{bmatrix} v' \\ qv' \end{bmatrix}$$
$$A = \begin{bmatrix} 0 & 1 \\ -\omega'^2 & -k \cdot \omega' \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ k \cdot \omega' \end{bmatrix} \quad C = \begin{bmatrix} 0 & 1 \\ \omega' & 0 \end{bmatrix} \qquad (5)$$

The discretization of this system has been performed using trapezoidal integrators, as they offer a better detection of the phase, which is important when dealing with sinusoidal signals . The symbolic values of each matrix of (7) are detailed in (6), shown at the bottom of the page. In these matrices, *Ts*is the sampling time of the discrete system, ω_[*n*] is the estimated frequency magnitude, which comes from the estimation made at the SRF-PLL block at each computation step, and *k* is the SOGI gain [14]

$$x[n+1] = A' \cdot x[n] + B' \cdot v[n]$$
$$y[n] = C' \cdot x[n] + D' \cdot v[n]. \qquad (6)$$

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure presented in (8)

$$A' = \left(I + \frac{A \cdot T_s}{2}\right)\left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$B' = \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot B$$
$$C' = T_s \cdot C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$D' = C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot \frac{B \cdot T_s}{2} \qquad (7)$$

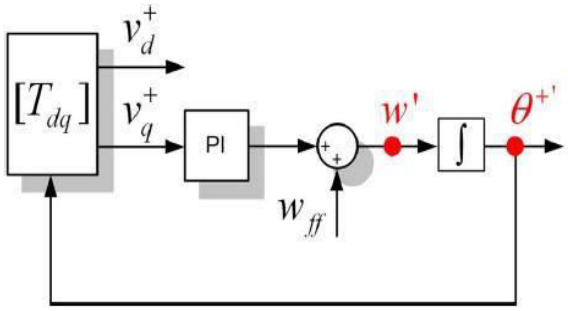

Fig.4. State Variables of the SRF-PLL Block.

where*Ts*is the sampling time. The resulting discrete system is the best option as it reduces the need of using additional delays for breaking algebraic loops that appear using other methods which do not consider the SOGI QSG as a whole.

2. SRF PllDiscretization

The frequency and phase detection is obtained by

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means of the SRF PLL shown in Fig. 8. The discretization of the controller and the integrator is performed using the backward numerical approximation. The frequency and phase can then be represented in the z-domain, as shown in (8), where *v*+ *q* constitutes the error to be minimized

$$\begin{aligned} \dot{A}'(t) &= k \cdot e(t) \cdot \cos\theta'(t) \\ \dot{\omega}'(t) &= -k_i \cdot e(t) \cdot \sin\theta'(t) \\ \dot{\theta}(t) &= \omega'(t) + \frac{k_p}{k_i} \cdot \dot{\omega}'(t) \end{aligned} \tag{8}$$

It can be noticed that the previous equations in (8) are equal to (2), as, in both cases, an SRF PLL is implemented. Likewise, the sample-based representation of (9) can be written as shown in

$$\begin{aligned} \omega'[n+1] &= \omega'[n] - k_p \cdot v^*_{q+1}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q+1}[n+1] \\ \theta^{+'}[n+1] &= \theta^{+'}[n] + T_s \cdot \omega'[n+1] \end{aligned} \tag{9}$$

C. 3phepllDiscretization

This three-phase grid synchronization system exploits the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three-phase voltages. The same EPLL structure is applied again to detect the magnitude and phase of the positive-sequence voltage component.

1. QSG Block—EpllDiscretization

The block diagram of the EPLL implemented in this paper is presented in Fig.5.

$$A' = \gamma \begin{bmatrix} 4 + 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 & 4T_s \\ -4T_s \cdot \omega'[n]^2 & 4 - 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 \end{bmatrix},$$

$$B' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ 4k \cdot \omega'[n] \end{bmatrix}$$

$$C' = \gamma \begin{bmatrix} -2T_s^2 \cdot \omega'[n]^2 & 4T_s \\ 2T_s \cdot \omega'[n] \cdot (2 + T_s \cdot k \cdot \omega'[n]) & 2T_s^2 \cdot \omega'[n] \end{bmatrix}$$

$$D' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ k \cdot T_s^2 \cdot \omega'[n]^2 \end{bmatrix}$$

$$\gamma = \frac{1}{4 + 2 \cdot T_s \cdot k \cdot \omega'[n] + T_s^2 \cdot \omega'[n]^2}$$

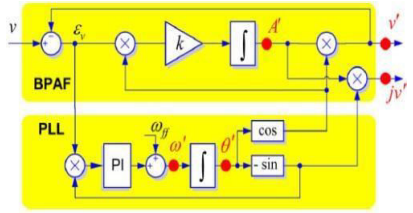

Fig.5. Quadrature Signal Generator Based on an EPLL Structure.

According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shownin

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z - 1} \cdot V^*_{q+1}(z) + \omega_{ff}$$

$$\text{The dis}\theta^{+'} = \frac{T_s \cdot z}{z - 1} \cdot W'(z) \tag{11}$$

variable representation was described in [44] using a forward Euler approximation to reach satisfactory results; therefore, the same method has been implemented here

$$\begin{aligned} e[n+1] &= u[n+1] - v'[n] \\ A'[n+1] &= A'[n] + T_s \cdot k \cdot e[n] \cdot \cos(\theta'[n]) \\ \omega'[n+1] &= \omega'[n] - T_s \cdot k_i \cdot e[n] \cdot \sin(\theta'[n]) \\ \theta'[n+1] &= \theta'[n] + T_s \cdot \omega'[n] - T_s \cdot k_p \cdot e[n] \cdot \sin(\theta'[n]) \end{aligned} \tag{12}$$

Finally, after the state variables are calculated, the EPLL output can be obtained by (13), generating the two quadraturesignals

$$qv'[n+1] = -A'[n+1] \cdot \sin(\theta'[n+1]) \tag{13}$$

This type of discretization method needs a more accurate tuning, due to the fact that the stable regions of the s-plane and z-plane are different [2]. However, its major simplicity, compared to the Tustin or backward integration, benefits from the computational speed of this block.

2. Computational BlockUnit

The description for this block is the same in both discrete and continuous domains. Nevertheless, specific equationsare used in this paper, as shown in(14).

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3. Phase and Magnitude DetectionBlock

This element is based on another EPLL, which is responsible for estimating the phase and the magnitude of the positive-sequence fundamental component. Its discretization is equal to that.

IV. Algorithm for Distributed Generation

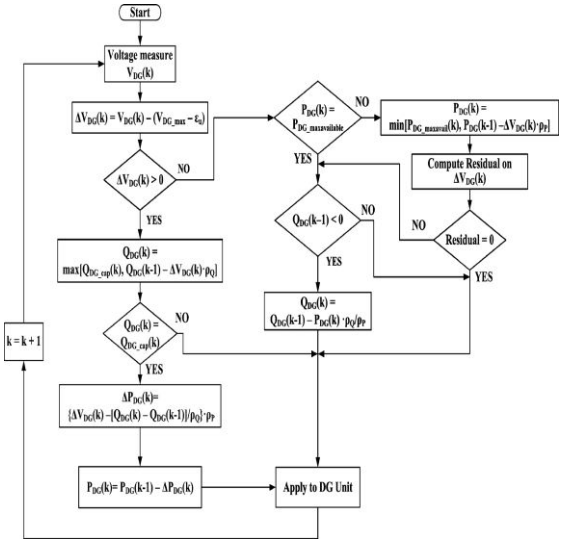

Fig.6. Grid voltage synchronization algorithm flowchart

V. SIMULATION MODEL DESIGN ANDRESULT

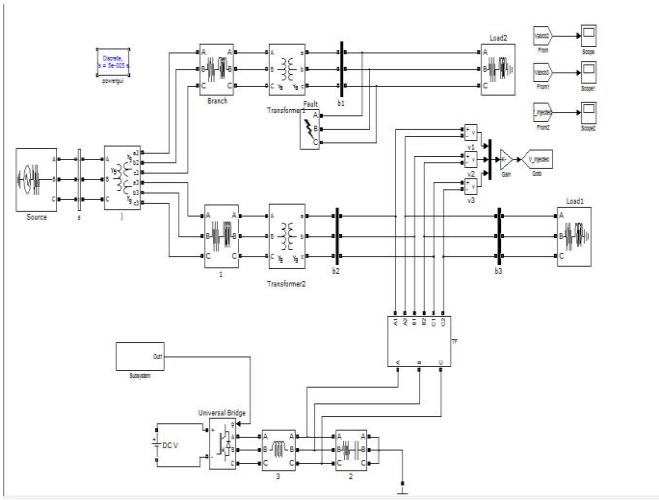

Fig.7. Simulation Model Design

A. Simulated WaveForms

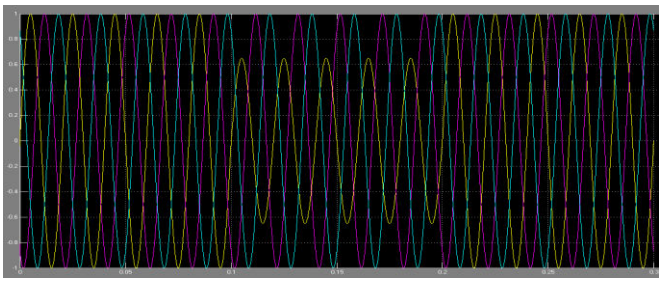

Fig.8.Bus One Voltage

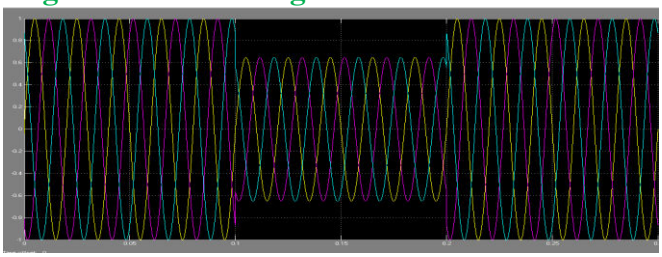

Fig.9. Source Side 3 Phase Voltages

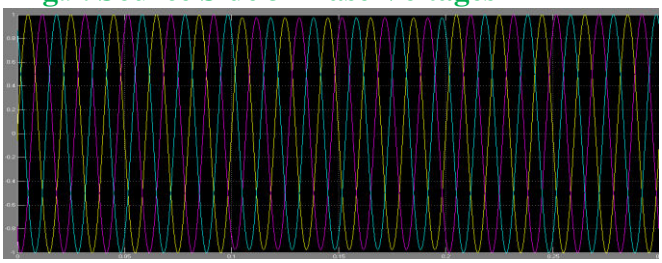

Fig.10.Three phase voltage

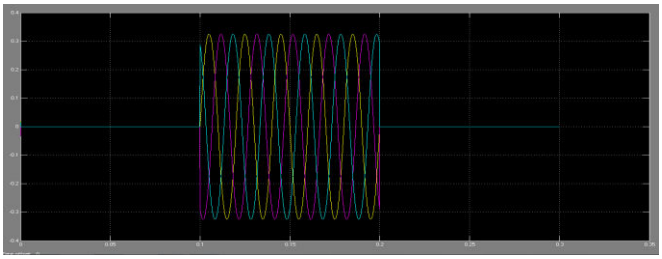

Fig.Injected voltage

CONCLUSION

This paper studied the behavior of three advanced grid synchronization systems. Their structures have been presented, and their discrete algorithms have been detailed. Moreover, their performances have been tested in an experimental setup, where these algorithms have been digitally implemented in a commercial DSP, allowing proof of their satisfactory response under balanced and distorted grid conditions. The DDSRF PLL and the DSOGI PLL

allow estimating the ISCs of a three-phase system working inthe$\alpha\beta$referenceframe,whilethe3phEPLLusesthe–*abc*‖ reference frame, thus working with three variables. As has been shown, this feature simplifies the structure of the DSOGI PLL and the DDSRF PLL, which allows reducing the computational burden, as compared to the 3phEPLL, without affecting its performance. The synchronization capability of the three PLLs under test has been shown to be fast and accurate under faulty scenarios, allowing the detection of the positive sequence of the voltage in 20–25 ms in all cases; however, the simpler structure of the DDSRF and the DSOGI affords an easier tuning of their control parameters and, therefore, a more accurate control of their transient response. The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater band pass and low-pass filtering capabilities. Although the DSOGI also gives rise to reasonably good results, due to its inherent band pass filtering structure, its response is more affected by harmonics. Although all three have been shown to be appropriate for synchronizing with the network voltage in distributed power generation applications, mainly PV and wind power, the lower computational cost of the DDSRF PLL and the DSOGI PLL, together with their robust estimation of the voltage parameters, offers a better tradeoff between the presented systems, making them particularly suitable for wind powerapplications.

I. REFERENCES

[1]A. Zervos and C. Kjaer, Pure Power: Wind Energy Scenarios for 2030. Brussels, Belgium: European Wind Energy Association (EWEA), Apr. 2008.[Online]. Available: http://www.ewea.org/index.php?id=11

[2]e-on,–Gridcode—Highandextrahighvoltage,‖ Bayreuth, Germany. Apr. 2006. [Online]. Available: http://www.pvupscale.org/IMG/pdf/ D4_2_ DE_annex_A- 3_EON_HV_grid connection_ requirements_ Enenarhs 2006de.pdf

[3]PO-12.3 Requisitos de RespuestaFrente a Huecos de Tension de lasInstalacionesEolicas, ComisiónNacional de Energía, Madrid, Spain, Oct. 2006.

[4]IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems, IEEE Std. 1547-2003, 2003. [5]The Grid Code: Revision 31, National Grid Electricity Transmission, Warwick, U.K., Oct. 2008, no. 3. [Online]. Available: http://www2. nationalgrid.com/uk/industry-information/electricity-codes/grid-code/ the-grid-code/

[6]ElkraftSystemogEltra,–Vindmullertilsluttetnetmed sprindinger under 100 kv,‖ Fredericia, Denmark, TF3.2.6, 2004. [Online]. Available: http://www.energinet.dk/ Site CollectionDocuments/Engelske%20dokumenter/El/ Grid%20 Code%203.2.5%20Wind%20Turbines%20connected %20abo ve%20100%20kV.pdf

[7]M. Tsili and S. Papathanassiou, ―A review of grid code technical requirements for wind farms,‖ IET Renew. Power Gen., vol. 3, no. 3, pp. 308–332, Sep. 2009.

[8]F. Iov, A. Hansen, P. Sorensen, and N. Cutululis, –MappingofGridFaultsandGridCodes,‖RisøNat.Lab., Roskilde, Denmark, Tech. Rep. Risoe- R-1617, 2007.

[9]A. Luna, P. Rodriguez, R. Teodorescu, and F. Blaabjerg, ―LowvoltageridethroughstrategiesforSCIGwindturbines in distributed power generation systems,‖ in Proc. IEEE PESC, Jun. 15–19, 2008, no. 1, pp.2333–2339.

[10]D.Xiang,L.Ran,P.J.Tavner,andS.Yang,–Control of a doubly fed induction generator in a wind turbine during grid fault ride-through,‖ IEEE Trans. Energy Convers., vol. 21, no. 3, pp. 652–662, Sep. 2006.