International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

UNIFIED POWER QUALITY CONDITIONER APPLIED TO THREE PHASE FOUR WIRE DISTRIBUTION SYSTEMS FOR POWER LINE CONDITIONING

***KOLLURI PRANEETHA ** CH RAJU**

*PG Scholar, Department of EEE, Vaagdevi College of Engineering (Ugc-Autonomous, Accredited By Nba)

**Assistant. Professor, Department of EEE, Vaagdevi College of Engineering(Ugc-Autonomous, Accredited By Nba)

ABSTRACT: —In this paper three different topologies of threephase four-wire Unified Power Quality Conditioner (UPQC) is compared for the mitigation of power quality problems in a four wire distribution system. The UPQC is a power conditioning device, which is a combination of shunt active power filter (APF) and series APF. The unit vector template (UVT) techniques is used to get the reference signals for series APF, where as the control strategy for shunt APF is based on combination of extended p-q theory and desired reference signals of series APF. MATLAB/Simulink based simulations are carried out, which support the functionality of the UPQC.

Index Terms-- Power Quality, UPQC, Harmonics, Load Balancing, Power Factor Correction, source neutral current mitigation.

I. INTRODUCTION IN a three-phase four-wire distribution system, poor voltage regulation, high reactive power demand and harmonics current burden, load unbalancing, excessive neutral current, voltage harmonics, voltage sag and swells are the main power quality problems. The quality degradation leads to low power-factor, low efficiency, overheating of transformers and so on. Moreover, in case of the distribution system, the overall load on the system is seldom found balanced, which cause excessive neutral currents in a threephase four-wire distribution system. Because of fundamental and high frequency contents in the neutral current, the overheating of the neutral conductor occurs [1]-[3]. With the application of sophisticated and more advanced software and hardware for the control systems, the power quality has become one of the most important issues for power electronics engineers. In order to control the power quality problems, many standards are proposed by different agencies such as IEEE-519 standard [4]. Ideally, voltage and current

waveforms are in phase, power factor of load equals unity, and the reactive power consumption is zero; this situation enables the most efficient transport of active power, leading of the cheapest distribution system. In the past, the solutions to mitigate these identified power quality problems were throughusing conventional passive filters. But their limitations such as ,fixed compensation, resonance with the source impedance and the difficulty in tuning time dependence of filter parameters have ignited the need of active and hybrid filters[5]-[7]. Under this circumstance, a new technology called custom power emerged [8], [9], which is applicable to distribution systems for enhancing the reliability and quality of the power supply. The Unified Power Quality Conditioner (UPQC) is one of the best solutions to compensate both current and voltage related problems, simultaneously [10-12]. As the UPQC is a combination of series and shunt APFs, two APFs have different functions. The series APF filter suppresses and isolates voltage-based distortions. The shunt APF cancels current-based distortions. At the same time, it compensates reactive current of the load and improves power factor. There are many control strategies reported in the literature to determine the reference values of the voltage and the current of three-phase four-wire UPQC, the most common are the pq-r theory[13],modified single-phase p-q theory[14], synchronous reference frame(SRF) theory[15], symmetrical component transformation [16],and unit vector template (UVT) technique [17],extended p-q theory[18] etc. Apart from this one cycle control (OCC) [19] (without reference calculation) is also used for the control of 3-phase, 4-wire UPQC. This paper presents a comparison of three different topologies for 3-phase, 4-wire UPQC for power quality improvements. A combination of extended p-q theory and UVT technique is proposed as a control strategy for the UPQC system. The proposed control technique is capable of extracting most of the load current and source voltage distortions successfully. The series APF is controlled to maintain voltage regulation and to eliminate supply voltage harmonics from the load terminal voltage. The shunt APF is controlled to alleviate the supply current from harmonics, negative sequence current, reactive power and load balancing. The performance of the proposed system is demonstrated through simulated waveforms and the harmonic spectra of supply currents and load voltage with and without UPQC

SYSTEM DISCRIPTION Fig. 1 shows the proposed 3-phase, 4-wire UPQC connected to a power system feeding a combination of linear

and non-linear unbalanced loads. It consists of three leg voltage controlled VSI used as a series APF and a four leg current controlled VSI used as a shunt APF. The dc link of both active filters is connected to a common dc link capacitor. The four-leg VSI based shunt active filter is capable of suppressing the harmonics in the source currents, negative sequence of load current, load balancing and power-factor correction. The second proposed topology for thee-phase four-wire UPQC is shown in Fig.2.In this topology three leg voltage controlled VSI are used for both the series and shunt APF. For neutral current compensation an additional star-delta transformer is connected on the load side. The star-delta transformer mitigates the neutral current by providing a circulating path in the delta connected secondary winding. The required rating of the star-delta transformer is calculated and the winding voltages are estimated for same current in all windings of the transformer. Fig.3 shows the third proposed configuration for the three-phase-four-wire UPQC in which, for neutral current compensation, an additional zig-zag transformer is connected near the load. The zig-zag transformer provides a path for the neutral current and split it in among the three-phases such that, the neutral current is effectively compensated. In all of the three proposed topologies of three-phase fourwire UPQC the series filter is connected between the supply and load terminals using three single phase transformers with turn's ratio of 5:1.The primary winding of these transformer are star connected and the secondary windings are connected in series with the three-phase supply. In addition to injecting the voltage, these transformers are used to filter the switching ripple content in the series active filter. A small capacity rated R-C filter is connected in parallel with the secondary winding of each series transformer to eliminate the high switching ripple content in the series active filter injected voltage. The voltage source inverters for both the APFs are implemented with IGBTs (Insulated gate Bipolar Transistors). The four-leg VSI based shunt active filter is capable of suppressing the harmonics in the source currents, negative sequence of source currents, load balancing and power-factor correction. The implemented control algorithm consists mainly of the computation of three-phase reference voltages of load voltages (v* la, v* lb and v* lc), and the reference currents for the source currents (i* sa, i * sb and i* sc). The load under consideration is a combination of linear and non-linear load. Two single-phase R-L loads are taken as unbalanced linear load, where as a three-phase diode bridge rectifier

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

with a resistive load on dc side is considered as a non-linear load. The values of the circuit parameters and load under consideration are given in Appendix

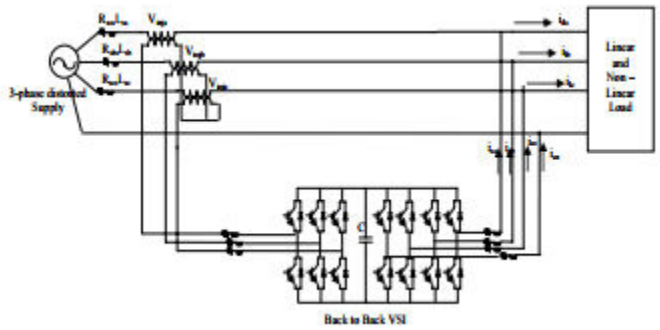


Fig.1.Three- Phase Four-wire UPQC with 4 leg Shunt APF

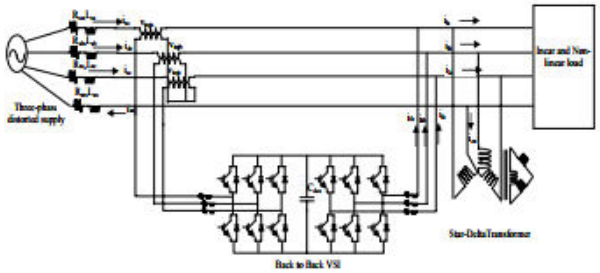


Fig.2.Three- Phase Four-wire UPQC with star-delta transformer on load side

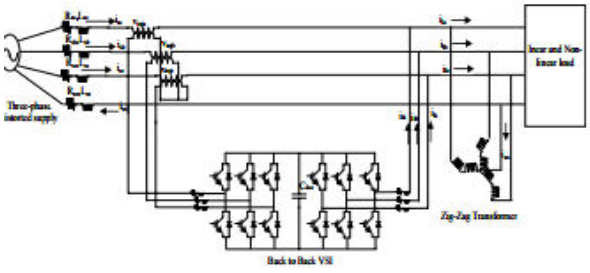


Fig.3.Three- Phase Four-wire UPQC with zig-zag transformer on load side

In order to make the input currents sinusoidal, balanced and in phase with the utility voltages, in the dual compensating strategy, the series PWM converter is controlled to operate as a sinusoidal current source. In this case, its impedance must be high enough to isolate the harmonic currents generated by the nonlinear loads. On the other hand, the parallel PWM converter also makes the output voltages sinusoidal, balanced, regulated and in phase with the utility voltages. In other words, it is controlled to operate as a sinusoidal voltage source, such that its impedance must be sufficiently low to absorb the load harmonic currents [30].

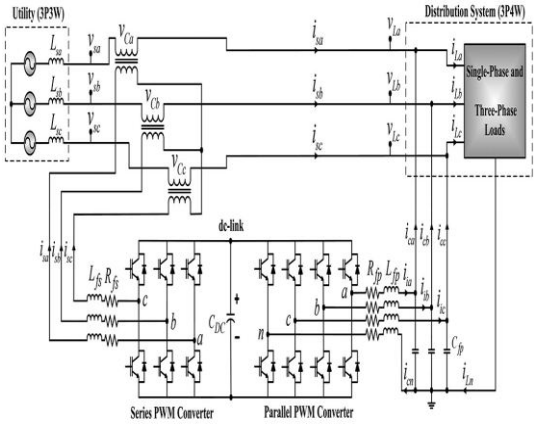


Fig.3P4W distribution system based on UPQC topology connected to 3P3W power system.

Since the series and parallel converters have high and low impedances, respectively, the load harmonic currents flow naturally through the parallel converter. Furthermore, compensation for load unbalances is ensured by

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

controlling the series converter to follow sinusoidal and balanced references so that the negative and zero sequence components are compensated. Finally, the fundamental reactive power compensation is ensured by controlling the series converter current references to be in phase with the utility voltages.

On the other hand, the utility harmonic voltages and unbalances are compensated ensuring that the controlled output voltages follow sinusoidal and balanced references such that the amplitude differences between the input and output voltages will appear across the series coupling transformers, meaning that any utility voltage disturbances are naturally compensated. This makes the dual compensating strategy more attractive than the conventional strategy, considering that the load is less affected by the occurrence of grid voltage disturbances, such as voltage sags. This is possible because, different from the conventional strategy in which the series converter controls the output voltages, in the dual compensating strategy this task is entirely assumed by the parallel converter.

Modeling of Series and Parallel Converters

The modeling of the series and parallel PWM converters are presented in this section. In addition, the voltage and current controllers implemented in the SRF (dq0 axes) are discussed.

Series Converter Modeling

The state-space system and the transfer functions of the series converter in the dq axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances and resistances are identical, as follows: Lfsa = Lfsa = Lfsa = Lfsb = Lfsc = Lf s and Rfsa =Rfsb = Rfsc = Rf s. By means of Fig. 1, the equations that represent the system are given by (3.1) and (3.2)

$$u_{sab\_PWM} = v_{L_{fsa}} + v_{R_{fsa}} + v_{C_{ab}} - v_{R_{fsb}} - v_{L_{fsb}}$$

$$u_{sbc\_PWM} = v_{L_{fsb}} + v_{R_{fsb}} + v_{C_{bc}} - v_{R_{fsc}} - v_{L_{fsc}}$$

Where usab PWM and usbc PWM are the respective PWM voltages at the 3-Leg series converter terminals.

Considering the voltages of the PWM series converter in the dq axes (usd_PWM and usq_PWM), the state-space equation is given by

$$\dot{x}_{sdq}(t) = A_{sdq}x_{sdq}(t) + B_{sdq}u_{sdq}(t) + F_{sdq}w_{sdq}(t)$$

Where

$$\dot{x}_{sdq}(t) = \begin{bmatrix} \frac{di_{sd}}{dt} \\ \frac{di_{sq}}{dt} \end{bmatrix},\ x_{sdq}(t) = \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix},\ u_{sdq} = \begin{bmatrix} u_{sd\_PWM} \\ u_{sq\_PWM} \end{bmatrix}$$

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

$$w_{\mathrm{sdq}}(t) = \begin{bmatrix} v_{\mathrm{cd}} \\ v_{\mathrm{cq}} \end{bmatrix}, \; A_{\mathrm{sdq}} = \begin{bmatrix} -\frac{R_{fs}}{L_{fs}} & \omega \\ -\omega & -\frac{R_{fs}}{L_{fs}} \end{bmatrix}$$

,

$$B_{\mathrm{sdq}} = \frac{1}{3L_{fs}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$F_{\mathrm{sdq}} = \frac{1}{3L_{fs}} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}.$$

Thereby, based on (3), the series converter average model represented as a signal flow graph is shown in the dotted area of Fig. 3.2(a). In addition, the current controller into the *dq*axes is also shown, where *Gs*(PI)*d*and *Gs*(PI)*q* represent the transfer functions of the PI current controllers; *D*sd and *D*sq are the duty cycles; *V*dc is the dc-bus voltage; and *K*PWM is the gain of the PWM modulator given by *K*PWM = 1/*P*PWM [31],where *P*PWM is the peak value of the PWM triangular carrier implemented in the digital signal processor (DSP). The current coupling between the *dq*axes, shown in the average model of Fig. 3.2(a), is eliminated by using the scheme presented in Fig. 3.2(b), where the dotted blocks represent the decoupling effects [32]implemented in the block diagram shown in Fig. 3.2(a).

Thus, based on Fig.3.2(a), the transfer functions of the closed loop system can be represented by (3.4), where $Kp_{s(d,q)}$and$Ki_{s(d,q)}$ are the proportional and integral controller gains, and$i^{*}_{s(d,q)}$ represents the continuous current references in the *dq*coordinates

$$\frac{i_{S(d,q)}(s)}{i^{*}_{S(d,q)}(s)} = \frac{X_1\left(Kp_{s(d,q)}s + Ki_{s(d,q)}\right)}{L_{fs}s^2 + \left(R_{fs} + X_1 Kp_{s(d,q)}\right)s + X_1 Ki_{s(d,q)}} \tag{3.4}$$

where X1 = K_{PWM} Vdc

Parallel Converter Modeling

The state-space system and the transfer functions of the parallel converter in the dq0 axes are obtained based on a mathematical model. The modeling is accomplished considering thatall involved inductances, resistances and capacitances are identical, as follows: Lfpa = Lfpb = Lfpc = Lfpn = Lfp, Rfpa =Rfpb = Rfpc = Rfpn = Rfp, and Cfpa = Cfpb = Cfpc = Cfp.

By means of Fig.3.1, the equations that represent the system are given by (3.5), (3.6), and (3.7) as follows:

$$u_{\mathrm{pan\_PWM}} = R_{\mathrm{fpa}} \cdot i_{\mathrm{ia}} + L_{\mathrm{fpa}} \frac{di_{\mathrm{ia}}}{dt} + v_{\mathrm{La}} + L_{\mathrm{fpn}} \frac{di_{\mathrm{cn}}}{dt} + R_{\mathrm{fpn}} \cdot i_{\mathrm{cn}} \tag{3.5}$$

$$u_{\mathrm{pbn\_PWM}} = R_{\mathrm{fpb}} \cdot i_{\mathrm{ib}} + L_{\mathrm{fpb}} \frac{di_{\mathrm{ib}}}{dt} + v_{\mathrm{Lb}} + L_{\mathrm{fpn}} \frac{di_{\mathrm{cn}}}{dt} + R_{\mathrm{fpn}} \cdot i_{\mathrm{cn}} \tag{3.6}$$

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

$$u_{\text{pcn\_PWM}} = R_{\text{fpc}} i_{\text{ic}} + L_{fcc} \frac{di_{\text{ic}}}{dt} + v_{\text{Lc}} + L_{\text{fpn}} \frac{di_{\text{cn}}}{dt} + R_{\text{fpn}} \cdot i_{\text{cn}}$$

(3.7)

where$u_{\text{pan_PWM}}$,$u_{\text{pbn\_PWM}}$, and $u_{\text{pcn\_PWM}}$ are the respective PWM voltages at the terminals *a*, *b*, and *c* of the 4-Leg parallel converter.

The capacitor currents of the output filters (i_{Cfpa},$i_{\text{Cfp b}}$ and $i_{\text{Cfp c}}$) are given by

$$i_{C_{\text{fpa}}} = C_{\text{fpa}} \frac{dv_{\text{La}}}{dt} = i_{\text{ia}} - i_{\text{ca}}$$

(3.8)

$$i_{C_{\text{fpb}}} = C_{\text{fpb}} \frac{dv_{\text{Lb}}}{dt} = i_{\text{ib}} - i_{\text{cb}}$$

(3.9)

$$i_{C_{\text{fpc}}} = C_{\text{fpc}} \frac{dv_{\text{Lc}}}{dt} = i_{\text{ic}} - i_{\text{cc}}$$

(3.10)

wherei_{ia}, i_{ib}, and i_{ic} are the currents of the inductors, and ica,icb, and icc are the output currents of the parallel converter.

Considering the PWM converter voltages of the parallel synchronous rotating frame ($u_{\text{pd\_PWM}}$, u_{pq_PWM}, and u_{p0_PWM}), the state-space equation is found as

$$\dot{x}_{\text{pdq0}}(t) = A_{\text{pdq0}} x_{\text{pdq0}}(t) + B_{\text{pdq0}} u_{\text{pdq0}}(t) + F_{\text{pdq0}} w_{\text{pdq0}}(t)$$

(3.11)

Where

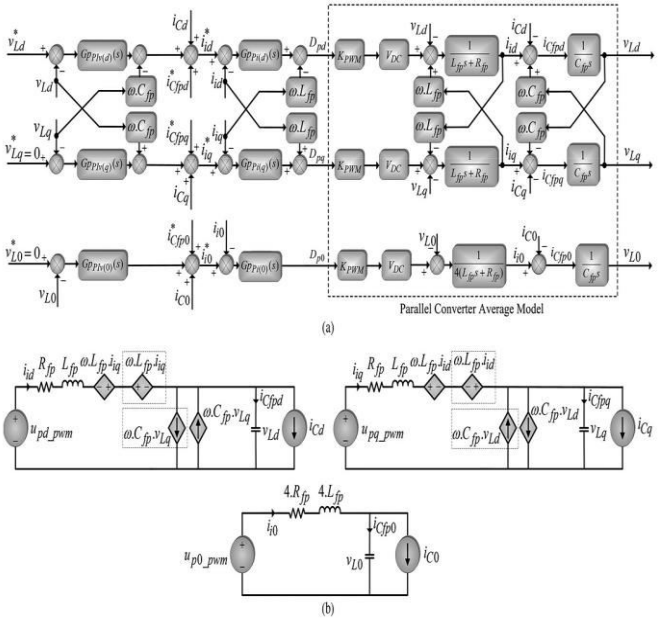
$$\dot{x}_{\text{pdq0}}(t) = \begin{bmatrix} \frac{di_{\text{id}}}{dt} & \frac{di_{\text{iq}}}{dt} & \frac{di_{\text{i0}}}{dt} & \frac{dv_{\text{Ld}}}{dt} & \frac{dv_{\text{Lq}}}{dt} & \frac{dv_{\text{L0}}}{dt} \end{bmatrix}^T$$

$$x_{\text{pdq0}}(t) = \begin{bmatrix} i_{\text{id}} & i_{\text{iq}} & i_{\text{i0}} & v_{\text{Ld}} & v_{\text{Lq}} & v_{\text{L0}} \end{bmatrix}^T$$

$$u_{\text{pdq0}} \begin{bmatrix} u_{\text{pd\_PWM}} \\ u_{\text{pq\_PWM}} \\ u_{\text{p0\_PWM}} \end{bmatrix}, \; w_{\text{pdq0}} \begin{bmatrix} i_{C_{\text{fpd}}} \\ i_{C_{\text{fpq}}} \\ i_{C_{\text{fp0}}} \end{bmatrix}$$

$$A_{\text{pdq0}} = \begin{bmatrix} -\frac{R_{\text{fp}}}{L_{\text{fp}}} & \omega & 0 & -\frac{1}{L_{\text{fp}}} & 0 & 0 \\ -\omega & -\frac{R_{\text{fp}}}{L_{\text{fp}}} & 0 & 0 & -\frac{1}{L_{\text{fp}}} & 0 \\ 0 & 0 & -\frac{R_{\text{fp}}}{L_{\text{fp}}} & 0 & 0 & -\frac{1}{4L_{\text{fp}}} \\ \frac{1}{C_{\text{fp}}} & 0 & 0 & 0 & \omega & 0 \\ 0 & \frac{1}{C_{\text{fp}}} & 0 & -\omega & 0 & 0 \\ 0 & 0 & \frac{1}{C_{\text{fp}}} & 0 & 0 & 0 \end{bmatrix}$$

$$B_{\text{pdq0}} = \begin{bmatrix} \frac{1}{L_{\text{fp}}} & 0 & 0 \\ 0 & \frac{1}{L_{\text{fp}}} & 0 \\ 0 & 0 & \frac{1}{4L_{\text{fp}}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$



International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

Fig. Parallel converter: (a) signal flow graph of the voltage controllers and average model; (b) model of the uncoupled system in SRF dq0 axes.

$$F_{\mathrm{pdq0}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -\frac{1}{C_{\mathrm{fp}}} & 0 & 0 \\ 0 & -\frac{1}{C_{\mathrm{fp}}} & 0 \\ 0 & 0 & -\frac{1}{C_{\mathrm{fp}}} \end{bmatrix}$$

Thereby, based on (11), the parallel converter average model represented as a signal flow graph is shown in the dotted area of Fig. In addition, the voltage and current controllers into the*dq*0 axes are presented, where *Gp*PI*v*(*d*), *Gp*PI*v*(*q*), and *Gp*PI*v*(0)represent the transfer functions of the PI voltage controllers(outer loops); *Gp*Pi(*d*), *Gp*Pi(*q*), and *Gp*Pi(0) are the transfer functions of the proportional current controllers (inner loops);and *D*pd, *D*pq, and *D*p0 are the duty cycles. The current and voltage coupling between the *dq*axes shown in the average model of Fig is eliminated by using the scheme presented in Fig.3.3, where the dotted blocks represent the decoupling effects, which are implemented in the block diagram shown in Fig.

Thus, based on the transfer functions of the closed-loop system can be represented by and where *Kpp*(*d,q*), *Kip*(*d,q*), and *Kip*(0) are the proportional and integral gains of the controllers (outer voltage control loop), *Kp*PI(*d,q*)and *Kp*PI(0) are the proportional gains (inner current-control loop), and $v^{*}_{L(d,q,0)}(s)$ represents the continuousvoltage references in the dq0 coordinates.

The currents of the filter capacitors icfp(d,q,0) shown inFig.3.3(a) are estimated considering the derivatives of the measured output voltages (vLa,b,c)and the respective capacitances(Cfpa,b,c) [4]

$$\frac{v_{L(d,q)}(s)}{v^{*}_{L(d,q)}(s)} = \frac{X_{1(d,q)}s^2 + X_{2(d,q)}s + X_{3(d,q)}}{Y_{1(d,q)}s^3 + Y_{2(d,q)}s^2 + Y_{3(d,q)}s + Y_{4(d,q)}} \quad (3.12)$$

$$\frac{v_{L(0)}(s)}{v^{*}_{L(0)}(s)} = \frac{X_{1(0)}s^2 + X_{2(0)}s + X_{3(0)}}{Y_{1(0)}s^3 + Y_{2(0)}s^2 + Y_{3(0)}s + Y_{4(0)}} \quad (3.13)$$

Where

$$\begin{aligned} X_{1(d,q)} &= K_{\mathrm{PWM}} V_{\mathrm{dc}} C_{\mathrm{fp}} K p_{\mathrm{PI}(d,q)} \\ X_{2(d,q)} &= K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(d,q)} K p_{p(d,q)} \\ X_{3(d,q)} &= Y_{4(d,q)} = K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(d,q)} K i_{p(d,q)} \\ Y_{1(d,q)} &= C_{\mathrm{fp}} L_{\mathrm{fp}} \\ Y_{2(d,q)} &= C_{\mathrm{fp}} (K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(d,q)} + R_{\mathrm{fp}}) \\ Y_{3(d,q)} &= K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(d,q)} K p_{p(d,q)} + 1 \\ X_{1(0)} &= K_{\mathrm{PWM}} V_{\mathrm{dc}} C_{\mathrm{fp}} K p_{\mathrm{PI}(0)} \\ X_{2(0)} &= K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(0)} K p_{p(0)} \\ X_{3(0)} &= Y_{4(0)} = K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(0)} K i_{p(0)} \\ Y_{1(0)} &= 4 C_{\mathrm{fp}} L_{\mathrm{fp}} \\ Y_{2(0)} &= C_{\mathrm{fp}} (K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(0)} + 4 R_{\mathrm{fp}}) \\ Y_{3(0)} &= K_{\mathrm{PWM}} V_{\mathrm{dc}} K p_{\mathrm{PI}(0)} K p_{p(0)} + 4. \end{aligned}$$

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

MATLAB/SIMULINK RESULTS

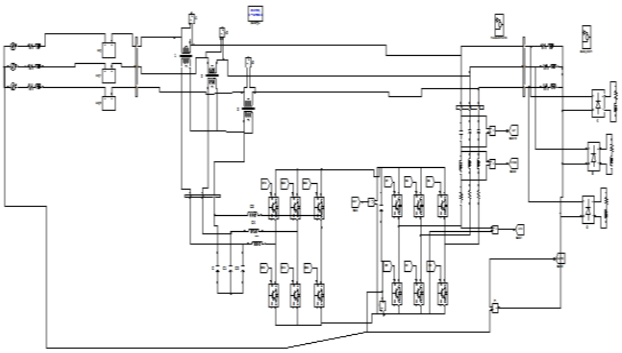


Fig.4.2 MATLAB/SIMULINK circuit of P4W distribution system based on UPQC topology connected to 3P3W power system

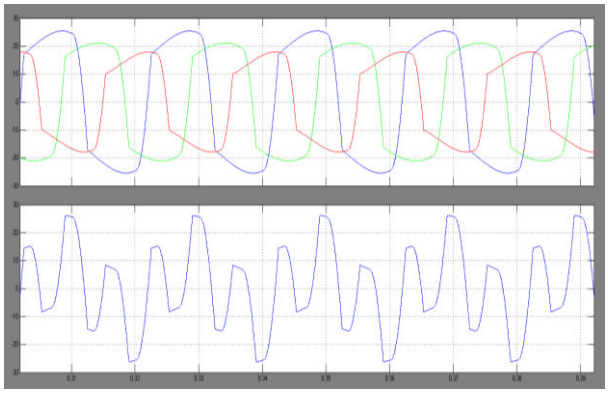


Fig.4.3 Output waveform of Load currents

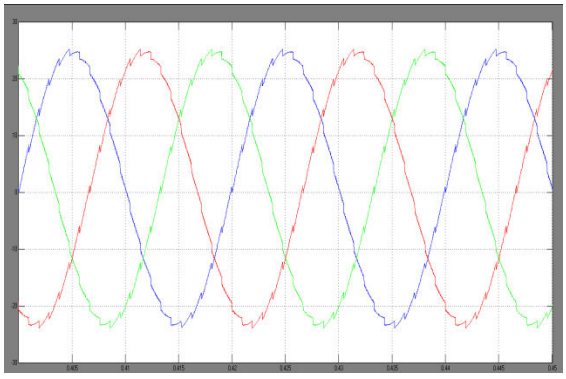


Fig.4.4 Output waveform of Compensated source currents

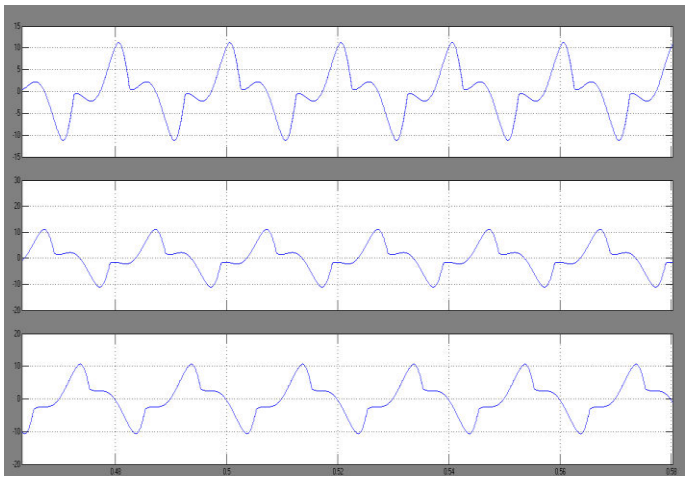


Fig.4.5 Output waveform of parallel converter currents

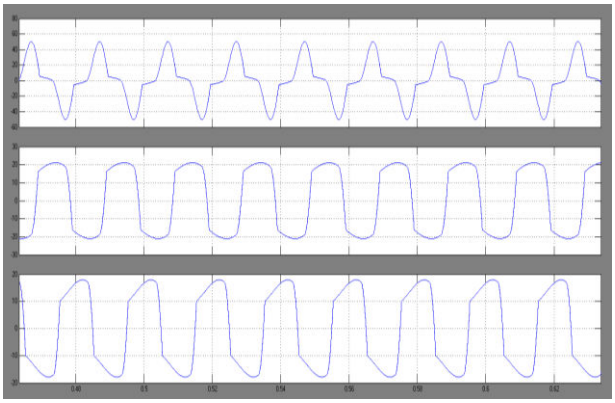


Fig.4.6 Output waveform of parallel converter Load currents

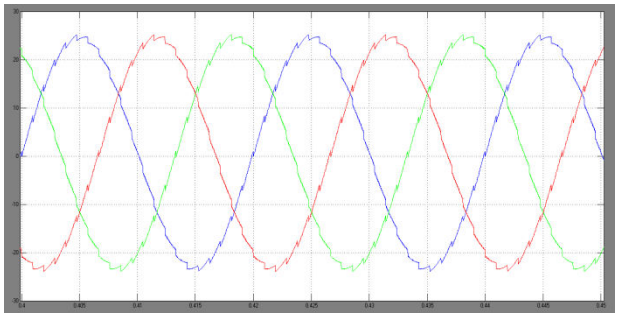


Fig.4.7 Output waveform of parallel converter Source-compensated currents

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

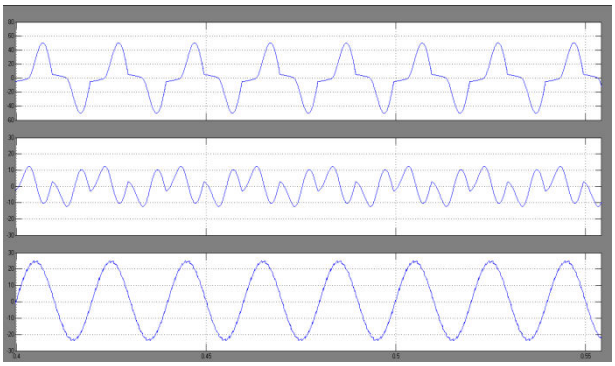


Fig.4.8 Output waveform of phase "a": load current, parallelconverter current and source current

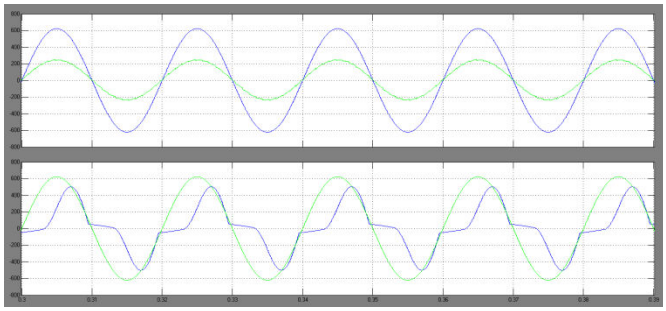


Fig.4.9 Output waveform of phase "a" load current, source current, utility voltageand load voltage

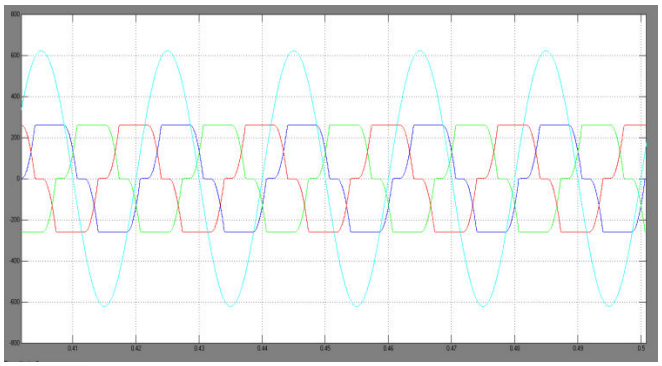


Fig.4.10 Output waveform of Load currents

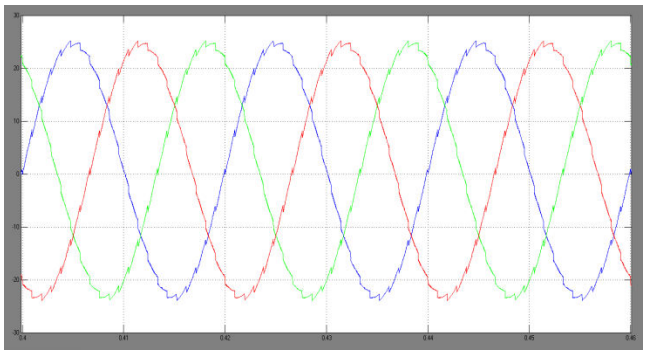


Fig.4.11 Output waveform of Source-compensated currents

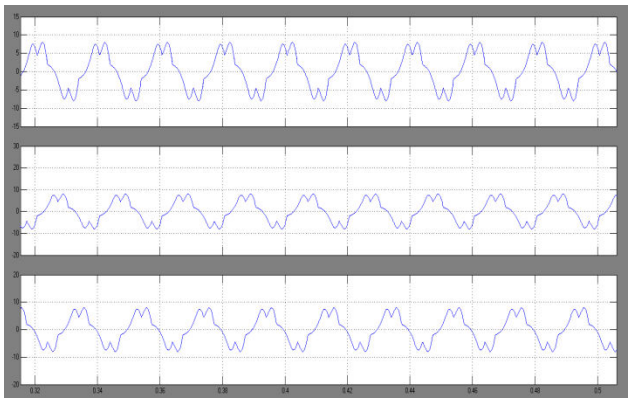


Fig.4.12 Output waveform of Parallel converter currents

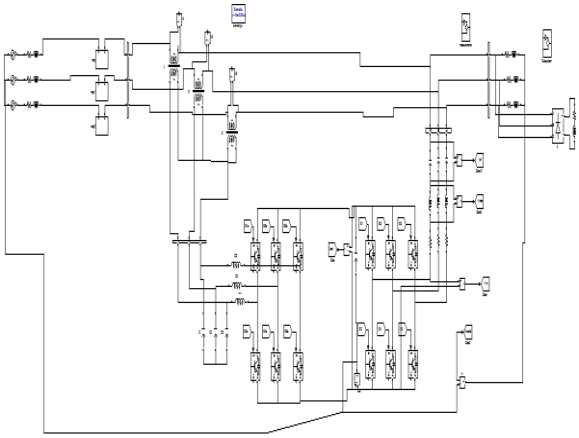


Fig.4.13 MATLAB/SIMULINK circuit of Voltages of the UPQC under utility harmonics and unbalances for the unbalanced three-phase load

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

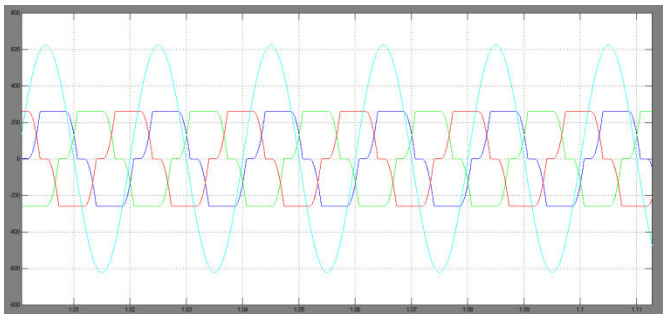


Fig.4.14 Output waveform of Utility voltages

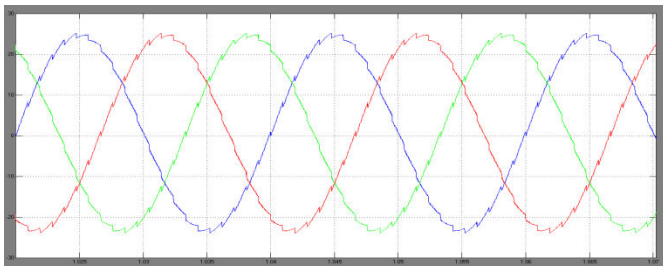


Fig.4.15 Output waveform of Load voltages

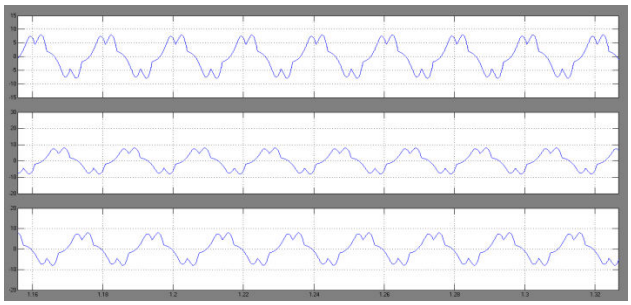


Fig.4.16 Output waveform of Series compensating voltages

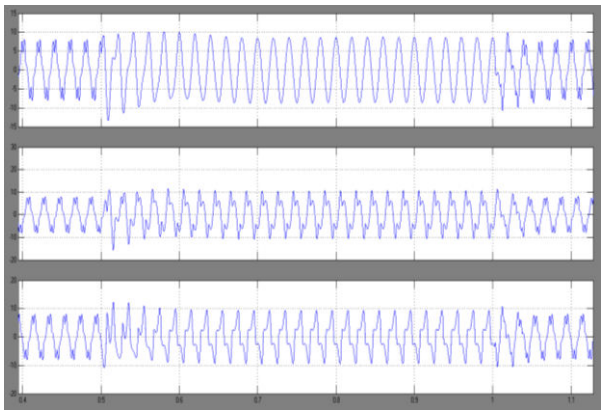


Fig.4.17 Output waveform of Utility voltage, load voltage and series compensating voltage

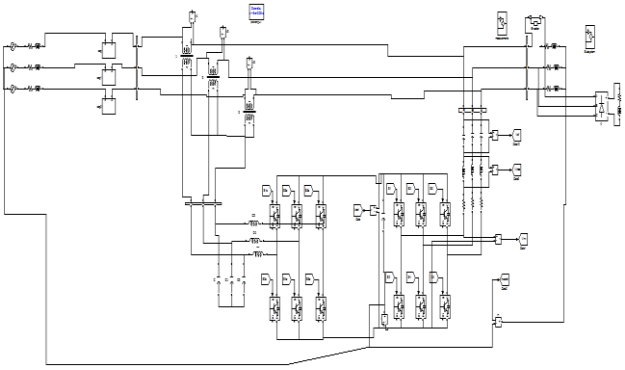


Fig.4.18 MATLAB/SIMULINK circuit of UPQC under voltage sag disturbance condition

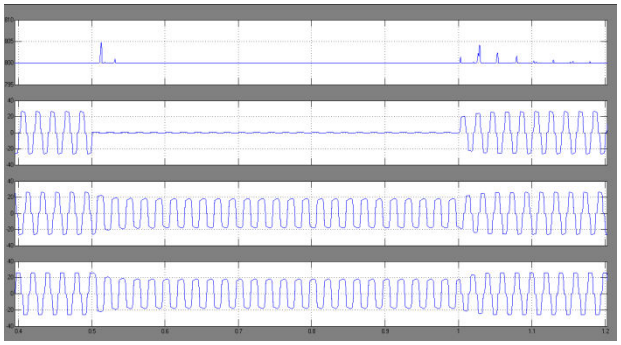


Fig.4.19 Output waveform of Dc-bus voltage, Load currents

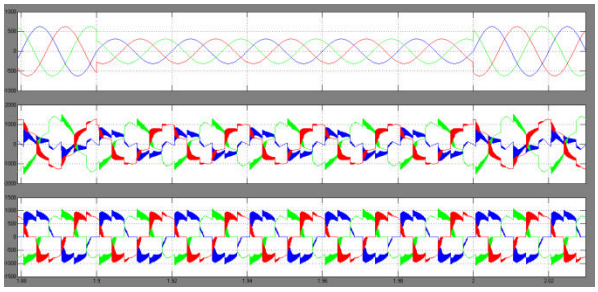


Fig.4.20 Output waveform of Source currents

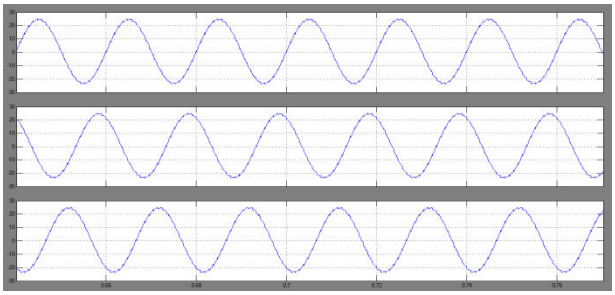
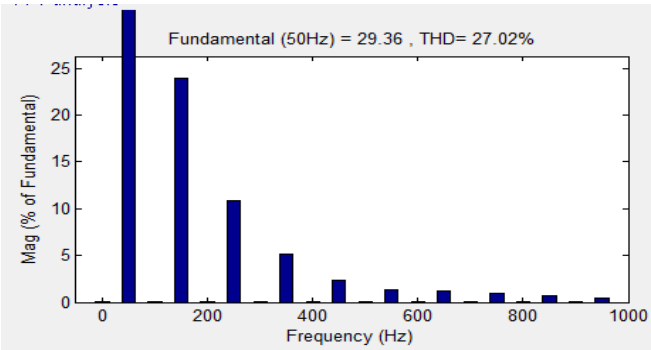
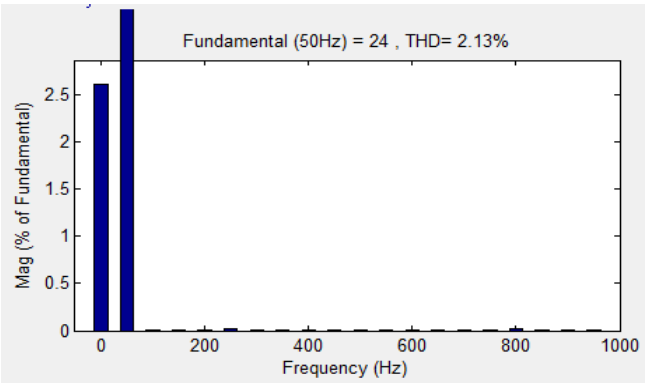


Fig.4.21 Output waveform of Source currents

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org





Currents of phase "a" for the unbalanced three-phase load1: source currenti_{sa} and load currenti_{La}

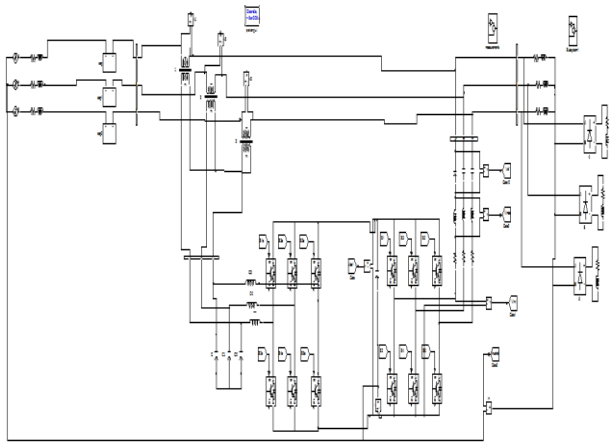
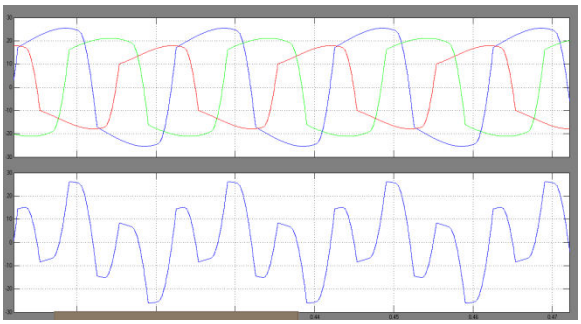
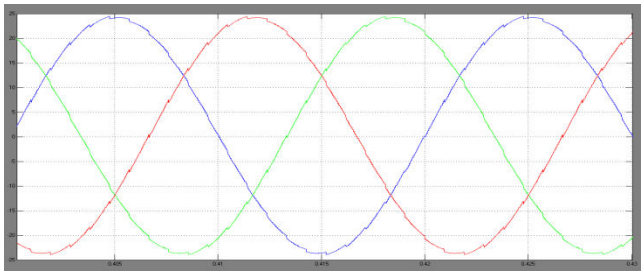


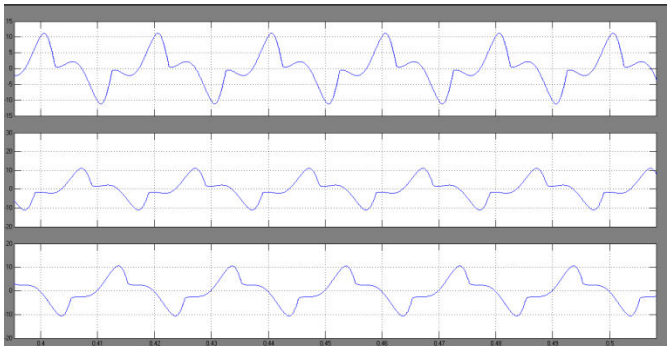
Fig.4.22. MATLAB/SIMULINK circuit of P4W distribution system based on UPQC topology connected to 3P3W power system with FUZZY logic control



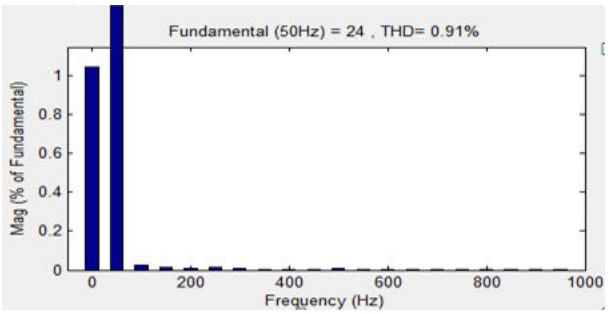
Load currents (iLa, iLb, iLc) and iLn,



Compensated source currents (isa, isb, isc)



Currents of the parallel converter (ica, icb, icc)



Source current THD

Fig.4.23 Simulation waveforms for Load currents, Source currents and Source current THD at Fuzzy Logic Controller

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org

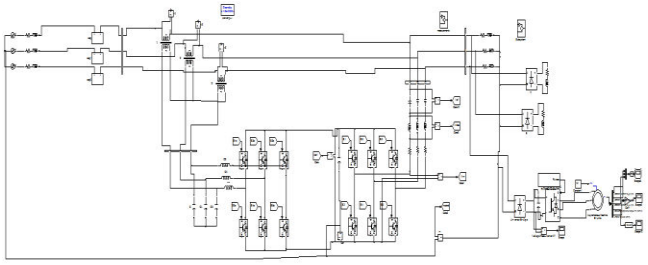
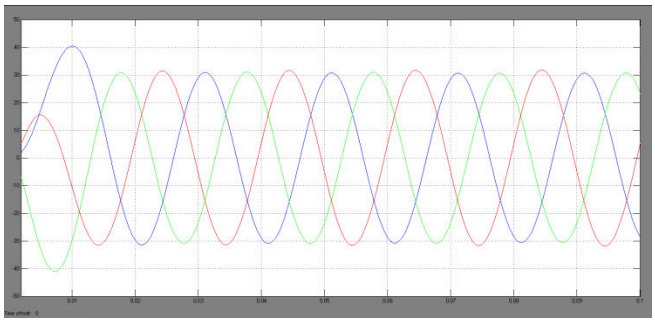
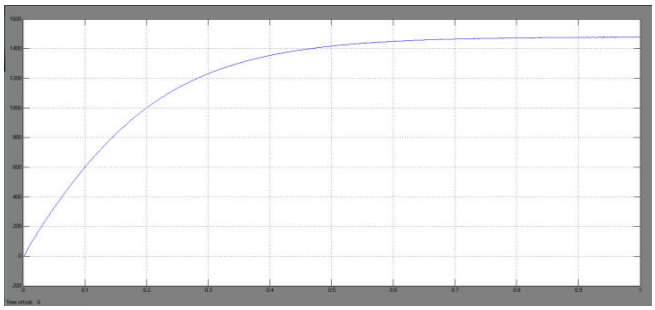


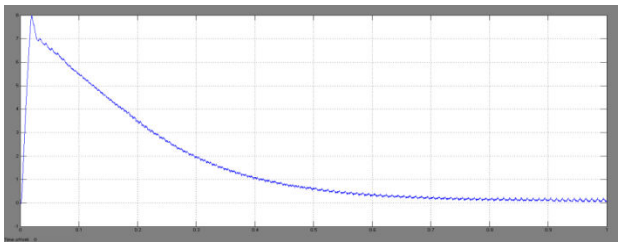
Fig.4.24 MATLAB/SIMULINK circuit of P4W distribution system based on UPQC topology connected to 3P3W with Single Phase Induction Motor Drive



Stator current



Speed



Electromagnetic Torque

Fig.4.25Simulation waveforms for Stator current, Speed and Electromagnetic Torque

CONCLUSION

This project presents a practical and versatile application based on UPQC, which can be used in 3P3W, as well as 3P4W distribution systems. It was demonstrated that the UPQC installed at a 3P3W system plant site was able to perform universal active filtering even when the installed loads required a neutral conductor for connecting one or more single-phase loads (3P4W). The series–parallel active filtering allowed balanced and sinusoidal input currents, as well as balanced, sinusoidal, and regulated output voltages.By using a dual control compensating strategy, the controlled voltage and current quantities are always sinusoidal. Therefore, it is possible to reduce the complexity of the algorithms used to calculate the compensation references. Furthermore, since voltage and current SRF-based controllers are employed, the control references become continuous, reducing the steady state errors when conventional PI controllers are used.Based on digital signal processing static and dynamic performances, as well as the effectiveness of the dual UPQC were evaluated, validating the theoretical development.

REFERENCES

[1] H. Fujita and H. Akagi, “The unified power quality conditioner: The integration of series and shunt active filters,” IEEE Trans. Power

Electron.,vol. 13, no. 2, pp. 315–322, Mar. 1998.

[2] R. J. M. Santos, J. C. Cunha, and M. Mezaroba, "A simplified control technique for a dual unified power quality conditioner," IEEE Trans. Ind.Electron., vol. 61, no. 11, pp. 5851–5860, Nov. 2014.

[3] B. W. Franc ¸a, L. F. Silva, M. AAredes, and M., Aredes, "An improved iUPQC controller to provide additional grid-voltage regulation as a STATCOM," IEEE Trans. Ind. Electron., vol. 62, no. 3, pp. 1345–1352, Mar.2015.

[4] R. A. Modesto, S. A. O. Silva, and A. A., Oliveira, "Power quality improvement using a dual unified power quality conditioner/uninterruptible power supply in three-phase four-wire systems," IET Power Electron.,vol. 8, no. 3, pp. 1595–1605, Sep. 2015.

[5] V. Khadkikar, "Enhancing electric power quality using UPQC: A comprehensive overview," IEEE Trans. Power Electron., vol. 27, no. 5,pp. 2284–2297, May 2012.

[6] V. Khadkikar, and A. Chandra, "A novel structure for three-phasefour-wire distribution system utilizing unified power quality conditioner(UPQC)," IEEE Trans. Ind. Appl., vol. 45, no. 5, pp. 1897–1902, Sep./Oct.2009.

[7] V. Khadkikar and A. Chandra, "UPQC-S: A novel concept of simultaneous voltage sag/swell and load reactive power compensations utilizing series inverter of UPQC," IEEE Trans. Power Electron., vol. 26, no. 9, pp. 2414–2425, Sep. 2011.

[8] M. Ucar, S. Ozdemir, and E. Ozdemir, "A four-leg unified series–parallel active filter system for periodic and non-periodic disturbance compensation," Electric Power Syst. Res., vol. 81, pp. 1132–1143, 2011.

[9] M. Kesler and E. Ozdemir, "Synchronous-reference-frame-based control method for UPQC under unbalanced and distorted load conditions," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 3967–3975, Sep. 2011.

[10] J. A. Munoz, J. R. Espinoza, C. R. Baier, L. A Mor ˜ an, E. E. Espinosa, ´P. E. Mel´ ın, and D. G Sbarbaro, "Design of a discrete-time linear control strategy for a multi cell UPQC," IEEE Trans. Ind. Electron., vol. 59,no. 10, pp. 3797–3807, Oct. 2012.

[11] S. B. Karanki, N. Geddada, M. K. Mishra, and B. K. Kumar, "A modified three-phase four-wire UPQC topology with reduced DC-

link voltage rating," IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3555–3566, Sep.2013.

[12] M. Ucar, and S. Ozdemir, "3-phase 4-leg unified series–parallel active filter system with ultracapacitor energy storage for unbalanced voltage sag mitigation," Electric Power Syst. Res., vol. 49, pp. 149–159, 2013.

[13] A. Teke, M. Meral, M. Cuma, M., Tumay, and C. A. Kamil, "Open unified ¨power quality conditioner with control based on enhanced phase locked loop," IET Generation Transmiss.Distrib., vol. 7, no. 3, pp. 254–264, Mar.2013.

[14] W. R. N. Santos, E. R. C. da Silva, C. B. Jacobina, E. M. Fernandes,A. C. Oliveira, R. R. Matias, D. F. G. Filho, and O. M. Almeida, "Thetransformer less single-phase universal active power filter for harmonicand reactive power compensation," IEEE Trans. Power Electron., vol. 29,no. 7, pp. 3563–3572, Jul. 2014.

[15] M. Brenna, R. Faranda, and E. Tironi, "A new proposal for power quality and custom power improvement: Open UPQC," IEEE Trans. Power Delivery, vol. 24, no. 4, pp. 2107–2116, Oct. 2009.

[16] B. B. Ambati, and V. Khadkikar, "Optimal sizing of UPQC considering VA loading and maximum utilization of power-electronic converters," IEEE Trans. Power Delivery, vol. 29, no. 3, pp. 1490–1498, Jun. 2014.

[17] I. Axente, J. N. Ganesh, M. Basu, M. F. Conlon, and K. Gaughan, "A12-kVA DSP-controlled laboratory prototype UPQC capable of mitigating unbalance in source voltage and load current," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1471–1479, Jun. 2010.

[18] B. A. Angelico, L. B. G. Campanhol, and S. A. O. Silva, "Proportional–´integral/proportional–integral–derivative tuning procedure of a single phase shunt active power filter using Bode diagram," IET Power Electron.,vol. 7, no. 10, pp. 2647–2659, Aug. 2014.

[19] J. He, Y. W. Li, F. Blaabjerg, and X. Wang, "Active harmonic filtering using current-controlled, grid-connected DG units with closed-loop power control," IEEE Trans. Power. Electron., vol. 29, no. 2, pp. 642–653, Feb.2014.

[20] F. Briz, P. Garc´ ıa, M. W. Degner, P. Garcia, and J. M. Guerrero, "Dynamic behavior of current controllers for selective harmonic compensation in three-phase active power filters," IEEE Trans. Ind. Appl., vol. 49, vol. 3,pp. 1411–1420, May/Jun. 2013.

International Journal for Innovative Engineering and Management Research
A Peer Revieved Open Access International Journal
www.ijiemr.org